**FEATURES**

- Tiny 3mm × 3mm 8-Pin DFN Package
- Maximum 16-Bit INL Error: ±1LSB over Temperature
- Low 120µA Supply Current
- Guaranteed Monotonic over Temperature
- Low 0.5nV•sec Glitch Impulse
- 2.7V to 5.5V Single Supply Operation
- Fast 1µs Settling Time to 16 Bits
- Unbuffered Voltage Output Directly Drives 60k Loads
- 50MHz SPI/QSPI/MICROWIRE Compatible Serial Interface
- Power-On Reset Clears DAC Output to Zero Scale (LTC2641) or Midscale (LTC2642)
- Schmitt-Trigger Inputs for Direct Optocoupler Interface
- Asynchronous CLR Pin
- 8-Lead MSOP and 3mm × 3mm DFN Packages (LTC2641)
- 10-Lead MSOP and 3mm × 3mm DFN Packages (LTC2642)

**APPLICATIONS**

- High Resolution Offset and Gain Adjustment
- Process Control and Industrial Automation
- Automatic Test Equipment
- Data Acquisition Systems

**TYPICAL APPLICATION**

**DESCRIPTION**

The LTC®2641/LTC2642 are families of 16-, 14- and 12-bit unbuffered voltage output DACs. These DACs operate from a single 2.7V to 5.5V supply and are guaranteed monotonic over temperature. The LTC2641A-16/LTC2642A-16 provide 16-bit performance (±1LSB INL and ±1LSB DNL) over temperature. Unbuffered DAC outputs result in low supply current of 120µA and a low offset error of ±1LSB.

Both the LTC2641 and LTC2642 feature a reference input range of 2V to VDD. VOUT swings from 0V to VREF. For bipolar operation, the LTC2642 includes matched scaling resistors for use with an external precision op amp (such as the LT1678), generating a ±VREF output swing at RFB.

The LTC2641/LTC2642 use a simple SPI/MICROWIRE compatible 3-wire serial interface which can be operated at clock rates up to 50MHz and can interface directly with optocouplers for applications requiring isolation. A power-on reset circuit clears the LTC2641’s DAC output to zero scale and the LTC2642’s DAC output to midscale when power is initially applied. A logic low on the CLR pin asynchronously clears the DAC to zero scale (LTC2641) or midscale (LTC2642). These DACs are all specified over the commercial and industrial ranges.

LTR, LT, LTC, LTM, Linear Technology and the Linear logo are registered trademarks and SoftSpan is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners.
**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

- $V_{DD}$ to GND: $-0.3V$ to $6V$
- $CS$, $SCLK$, $DIN$, $CLR$ to GND: $-0.3V$ to $(V_{DD} + 0.3V)$ or $6V$
- $REF$, $V_{OUT}$, $INV$ to GND: $-0.3V$ to $(V_{DD} + 0.3V)$ or $6V$
- $R_{FB}$ to $INV$: $-6V$ to $6V$
- $R_{FB}$ to GND: $-6V$ to $6V$
- GND to GND (S8 Package) OBSOLETE: $-0.3V$ to $0.3V$

Operating Temperature Range

- LTC2641C/LTC2642C: $0^\circ C$ to $70^\circ C$
- LTC2641/LTC2642: $-40^\circ C$ to $85^\circ C$

Maximum Junction Temperature (Note 2): $125^\circ C$

Storage Temperature Range: $-65^\circ C$ to $150^\circ C$

Lead Temperature (Soldering, 10 sec): $300^\circ C$

**PIN CONFIGURATION**

### LTC2641

- **Top View**
  - DD PACKAGE: 8-LEAD (3mm x 3mm) PLASTIC DFN
  - $T_{JMAX}$ = $125^\circ C$ (Note 2), $\theta_{JA} = 43^\circ C/W$
  - Exposed pad (pin 9) is GND, must be soldered to PCB

### LTC2641

- Top View
  - MS8 PACKAGE: 8-LEAD PLASTIC MSOP
  - $T_{JMAX}$ = $125^\circ C$ (Note 2), $\theta_{JA} = 120^\circ C/W$

### LTC2642

- **Top View**
  - DD PACKAGE: 10-LEAD (3mm x 3mm) PLASTIC DFN
  - $T_{JMAX}$ = $125^\circ C$ (Note 2), $\theta_{JA} = 43^\circ C/W$
  - Exposed pad (pin 11) is GND, must be soldered to PCB

### LTC2642

- **Top View**
  - MS PACKAGE: 8-LEAD PLASTIC SO
  - $T_{JMAX}$ = $125^\circ C$, $\theta_{JA} = 110^\circ C/W$

OBSOLETE PACKAGE

For more information [www.linear.com/LTC2641](http://www.linear.com/LTC2641)
## ORDER INFORMATION

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<td>10-Lead Plastic MSOP</td>
<td>–40°C to 85°C</td>
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</tbody>
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**OBSOLETE**

| LTC2641CS8-16#PBF | LTC2641CS8-16#TRPBF | 264116 | 8-Lead Plastic SO | 0°C to 70°C |
| LTC2641IS8-16#PBF | LTC2641IS8-16#TRPBF | 264116 | 8-Lead Plastic SO | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
## LTC2641/LTC2642

### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{DD} = 3V$ or 5V, $V_{REF} = 2.5V$, $C_L = 10pF$, $GND = 0$, $R_L = \infty$ unless otherwise specified.

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<td>±0.5</td>
<td>±1</td>
<td>±0.5</td>
<td>±1</td>
<td>±0.5</td>
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<td>2</td>
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<td>±1</td>
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<td>Bipolar Resistor Matching</td>
<td>(LTC2642) $R_{FB}/R_{INV}$</td>
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<td>1</td>
<td>kΩ</td>
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<td>±1</td>
<td>LSB</td>
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The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{DD} = 3V$ or 5V, $V_{REF} = 2.5V$, $C_L = 10pF$, $GND = 0$, $R_L = \infty$ unless otherwise specified.

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<td>$\mu s$</td>
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<td>$V_{IH}$</td>
<td>Digital Input High Voltage</td>
<td>$V_{CC} = 3.6V$ to 5.5V</td>
<td>$V_{CC} = 2.7V$ to 3.5V</td>
<td></td>
<td>●</td>
<td>2.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Digital Input Low Voltage</td>
<td>$V_{CC} = 4.5V$ to 5.5V</td>
<td>$V_{CC} = 2.7V$ to 4.5V</td>
<td></td>
<td>●</td>
<td>0.8</td>
</tr>
</tbody>
</table>

For more information www.linear.com/LTC2641
**ELECTRICAL CHARACTERISTICS**  The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{DD} = 3V$ or $5V$, $V_{REF} = 2.5V$, $C_L = 10pF$, $GND = 0$, $R_L = \infty$ unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IN}$</td>
<td>Digital Input Current</td>
<td>$V_{IN} = GND$ to $V_{DD}$</td>
<td>●</td>
<td>±1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Digital Input Capacitance</td>
<td>(Note 6)</td>
<td>●</td>
<td>3</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>$V_H$</td>
<td>Hysteresis Voltage</td>
<td></td>
<td></td>
<td>0.15</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**Power Supply**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Supply Voltage</td>
<td>Digital Inputs = $0V$ or $V_{DD}$</td>
<td>●</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Supply Current, $V_{DD}$</td>
<td>Digital Inputs = $0V$ or $V_{DD}$</td>
<td>●</td>
<td>120</td>
<td>200</td>
<td>µA</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power Dissipation</td>
<td>Digital Inputs = $0V$ or $V_{DD}$, $V_{DD} = 5V$</td>
<td></td>
<td>0.60</td>
<td></td>
<td>mW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Digital Inputs = $0V$ or $V_{DD}$, $V_{DD} = 3V$</td>
<td></td>
<td>0.36</td>
<td></td>
<td>mW</td>
</tr>
</tbody>
</table>

**TIMING CHARACTERISTICS**  The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$. $V_{DD} = 3V$ or $5V$, $V_{REF} = 2.5V$, $C_L = 10pF$, $GND = 0$, $R_L = \infty$ unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_1$</td>
<td>DIN Valid to SCLK Setup Time</td>
<td></td>
<td>●</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_2$</td>
<td>DIN Valid to SCLK Hold Time</td>
<td></td>
<td>●</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_3$</td>
<td>SCLK Pulse Width High</td>
<td></td>
<td>●</td>
<td>9</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_4$</td>
<td>SCLK Pulse Width Low</td>
<td></td>
<td>●</td>
<td>9</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_5$</td>
<td>$CS$ Pulse High Width</td>
<td></td>
<td>●</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_6$</td>
<td>LSB SCLK High to $CS$ High</td>
<td></td>
<td>●</td>
<td>8</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_7$</td>
<td>$CS$ Low to SCLK High</td>
<td></td>
<td>●</td>
<td>8</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_8$</td>
<td>$CS$ High to SCLK Positive Edge</td>
<td></td>
<td>●</td>
<td>8</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_9$</td>
<td>CLR Pulse Width Low</td>
<td></td>
<td>●</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$f_{SCLK}$</td>
<td>SCLK Frequency 50% Duty Cycle</td>
<td></td>
<td>●</td>
<td>50</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$V_{DD}$ High to $CS$ Low (Power-Up Delay)</td>
<td></td>
<td></td>
<td></td>
<td>30</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 3:** LTC2641-16/LTC2642-16 ±1LSB = ±0.0015% = ±15.3ppm of full scale. LTC2641-14/LTC2642-14 ±1LSB = ±0.006% = ±61ppm of full scale. LTC2641-12/LTC2642-12 ±1LSB = ±0.024% = ±244ppm of full scale.

**Note 4:** $R_{OUT}$ tolerance is typically ±20%.

**Note 5:** Reference input resistance is code dependent. Minimum is at \textcolor{red}{871Chex} (34,588) in unipolar mode and at \textcolor{red}{671Chex} (26,396) in bipolar mode.

**Note 6:** Guaranteed by design and not production tested.

**Note 7:** Guaranteed by gain error and offset error testing, not production tested.

For more information [www.linear.com/LTC2641](http://www.linear.com/LTC2641)
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity (INL)

Differential Nonlinearity (DNL)

INL vs Temperature

DNL vs Temperature

Bipolar Zero Error vs Temperature
TYPICAL PERFORMANCE CHARACTERISTICS

Bipolar Gain Error vs Temperature

Unbuffered Zero Scale Error vs Temperature (LTC2641-16)

Unbuffered Full-Scale Error vs Temperature (LTC2641-16)

14-Bit Integral Nonlinearity (INL) (LTC2642-14)

14-Bit Differential Nonlinearity (DNL) (LTC2642-14)

IREF vs Code (Unipolar LTC2641)

12-Bit Integral Nonlinearity (INL) (LTC2642-12)

12-Bit Differential Nonlinearity (DNL) (LTC2642-12)

IREF vs Code (Bipolar LTC2642)

For more information www.linear.com/LTC2641
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current (I_DD) vs Temperature

![Graph showing Supply Current (I_DD) vs Temperature](image1)

Supply Current (I_DD) vs Supply Voltage (V_DD)

![Graph showing Supply Current (I_DD) vs Supply Voltage (V_DD)](image2)

Supply Current (I_DD) vs Digital Input Voltage

![Graph showing Supply Current (I_DD) vs Digital Input Voltage](image3)

Supply Current (I_DD) vs VREF, V_DD = 5V

![Graph showing Supply Current (I_DD) vs VREF, V_DD = 5V](image4)

Supply Current (I_DD) vs VREF, V_DD = 3V

![Graph showing Supply Current (I_DD) vs VREF, V_DD = 3V](image5)

Midscale Glitch Impulse

![Graph showing Midscale Glitch Impulse](image6)

Full-Scale Transition

![Graph showing Full-Scale Transition](image7)

Full-Scale Settling (Zoomed In)

![Graph showing Full-Scale Settling (Zoomed In)](image8)

VOUT vs V_DD = 0V to 5.5V (POR Function) LTC2641

![Graph showing VOUT vs V_DD = 0V to 5.5V (POR Function) LTC2641](image9)
**PIN FUNCTIONS**

**LTC2641 – MSOP, DFN Packages**

**REF (Pin 1):** Reference Voltage Input. Apply an external reference at REF between 2V and VDD.

**CS (Pin 2):** Serial Interface Chip Select/Load Input. When CS is low, SCLK is enabled for shifting in data on DIN. When CS is taken high, SCLK is disabled, the 16-bit input word is latched and the DAC is updated.

**SCLK (Pin 3):** Serial Interface Clock Input. CMOS and TTL compatible.

**DIN (Pin 4):** Serial Interface Data Input. Data is applied to DIN for transfer to the device at the rising edge of SCLK.

**CLR (Pin 5):** Asynchronous Clear Input. A logic low clears the DAC to code 0.

**VOUT (Pin 6):** DAC Output Voltage. The output range is 0V to VREF.

**VDD (Pin 7):** Supply Voltage. Set between 2.7V and 5.5V.

**GND (Pin 8):** Circuit Ground.

**Exposed Pad (DFN Pin 9):** Circuit Ground. Must be soldered to PCB ground.

**LTC2642 – MSOP, DFN Packages**

**REF (Pin 1):** Reference Voltage Input. Apply an external reference at REF between 2V and VDD.

**CS (Pin 2):** Serial Interface Chip Select/Load Input. When CS is low, SCLK is enabled for shifting in data on DIN. When CS is taken high, SCLK is disabled, the 16-bit input word is latched and the DAC is updated.

**SCLK (Pin 3):** Serial Interface Clock Input. CMOS and TTL compatible.

**DIN (Pin 4):** Serial Interface Data Input. Data is applied to DIN for transfer to the device at the rising edge of SCLK.

**CLR (Pin 5):** Asynchronous Clear Input. A logic low clears the DAC to midscale.

**VOUT (Pin 6):** DAC Output Voltage. The output range is 0V to VREF.

**INV (Pin 7):** Center Tap of Internal Scaling Resistors. Connect to an external amplifier's inverting input in bipolar mode.

**RFB (Pin 8):** Feedback Resistor. Connect to an external amplifier's output in bipolar mode. The bipolar output range is \(-V_{REF}\) to \(V_{REF}\).

**VDD (Pin 9):** Supply Voltage. Set between 2.7V and 5.5V.

**GND (Pin 10):** Circuit Ground.

**Exposed Pad (DFN Pin 11):** Circuit Ground. Must be soldered to PCB ground.

**LTC2641 – SO Package OBSOLETE**

**VOUT (Pin 1):** DAC Output Voltage. The output range is 0V to VREF.

**GND (Pin 2):** Circuit Ground.

**REF (Pin 3):** Reference Voltage Input. Apply an external reference at REF between 2V and VDD.

**CS (Pin 4):** Serial Interface Chip Select/Load Input. When CS is low, SCLK is enabled for shifting in data on DIN. When CS is taken high, SCLK is disabled, the 16-bit input word is latched and the DAC is updated.

**SCLK (Pin 5):** Serial Interface Clock Input. CMOS and TTL compatible.
LTC2641/LTC2642

**BLOCK DIAGRAMS**

**LTC2641 - MSOP, DFN**

1. **VDD**
2. **CS**
3. **SCLK**
4. **DIN**
5. **CLR**
6. **GND**
7. **REF**
8. **16-/14-/12-BIT DAC**
9. **16-BIT DATA LATCH**
10. **16-BIT SHIFT REGISTER**
11. **VOUT**

**LTC2641 - SO OBSOLETE PACKAGE**

1. **VDD**
2. **CS**
3. **SCLK**
4. **DIN**
5. **CLR**
6. **GND**
7. **REF**
8. **16-/14-/12-BIT DAC**
9. **16-BIT DATA LATCH**
10. **16-BIT SHIFT REGISTER**
11. **VOUT**

**LTC2642**

1. **VDD**
2. **CS**
3. **SCLK**
4. **DIN**
5. **CLR**
6. **GND**
7. **INV**
8. **RFB**
9. **REF**
10. **16-/14-/12-BIT DAC**
11. **16-BIT DATA LATCH**
12. **16-BIT SHIFT REGISTER**
13. **VOUT**

For more information www.linear.com/LTC2641
**OPERATION**

**General Description**

The LTC2641/LTC2642 family of 16-/14-/12-bit voltage output DACs offer full 16-bit performance with less than ±1LSB integral linearity error and less than ±1LSB differential linearity error, guaranteeing monotonic operation. They operate from a single supply ranging from 2.7V to 5.5V, consuming 120µA (typical). An external voltage reference of 2V to VDD determines the DAC’s full-scale output voltage. A 3-wire serial interface allows the LTC2641/LTC2642 to fit into a small 8-/10-pin MSOP or DFN 3mm × 3mm package.

**Digital-to-Analog Architecture**

The DAC architecture is a voltage switching mode resistor ladder using precision thin-film resistors and CMOS switches. The LTC2641/LTC2642 DAC resistor ladders are composed of a proprietary arrangement of matched DAC sections. The four MSBs are decoded to drive 15 equally weighted segments, and the remaining lower bits drive successively lower weighted sections. Major carry glitch impulse is very low at 500pV*sec, C_L = 10pF, ten times lower than previous DACs of this type.

The digital-to-analog transfer function at the VOUT pin is:

$$V_{OUT(IDEAL)} = \left( \frac{k}{2^N} \right) V_{REF}$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution, and VREF is between 2.0V and VDD (see Tables 1a, 1b and 1c).

The LTC2642 includes matched resistors that are tied to an external amplifier to provide bipolar output swing (Figure 2). The bipolar transfer function at the RFB pin is:

$$V_{OUT\_BIPOLAR(IDEAL)} = V_{REF} \left( \frac{k}{2^{N-T}} - 1 \right)$$

(see Tables 2a, 2b and 2c).

**Serial Interface**

The LTC2641/LTC2642 communicates via a standard 3-wire SPI/QSPI/MICROWIRE compatible interface. The chip select input (CS) controls and frames the loading of serial data from the data input (DIN). Following a CS
high-to-low transition, the data on DIN is loaded, MSB first, into the shift register on each rising edge of the serial clock input (SCLK). After 16 data bits have been loaded into the serial input register, a low-to-high transition on CS transfers the data to the 16-bit DAC latch, updating the DAC output (see Figures 1a, 1b, 1c). While CS remains high, the serial input shift register is disabled. If there are less than 16 low-to-high transitions on SCLK while CS remains low, the data will be corrupted, and must be reloaded. Also, if there are more than 16 low-to-high transitions on SCLK while CS remains low, only the last 16 data bits loaded from DIN will be transferred to the DAC latch. For the 14-bit DACs, (LTC2641-14/LTC2642-14), the MSB remains in the same (left-justified) position in the input 16-bit data word. Therefore, two “don’t-care” bits must be loaded after the LSB, to make up the required 16 data bits (Figure 1b). Similarly, for the 12-bit family members (LTC2641-12/LTC2642-12) four “don’t-care” bits must follow the LSB (Figure 1c).

Power-On Reset

The LTC2641/LTC2642 include a power-on reset circuit to ensure that the DAC output comes up in a known state. When VDD is first applied, the power-on reset circuit sets the output of the LTC2641 to zero-scale (code 0). The LTC2642 powers up to midscale (bipolar zero). Depending on the DAC number of bits, the midscale code is: 32,768 (LTC2642-16); 8,192 (LTC2642-14); or 2,048 (LTC2642-12).

Clearing the DAC

A 10ns (minimum) low pulse on the CLR pin asynchronously clears the DAC latch to code zero (LTC2641) or to midscale (LTC2642).
APPLICATIONS INFORMATION

Unipolar Configuration

Figure 2 shows a typical unipolar DAC application for the LTC2641. Tables 1a, 1b and 1c show the unipolar binary code tables for 16-bit, 14-bit and 12-bit operation.

The external amplifier provides a unity-gain buffer. The LTC2642 can also be used in unipolar configuration by tying RFB and INV to REF. This provides power-up and clear to midscale.

Figure 2. 16-Bit Unipolar Output (LTC2641-16) Unipolar \( V_{\text{OUT}} = 0 \text{V} \) to \( V_{\text{REF}} \)

---

Table 1a. 16-Bit Unipolar Binary Code Table (LTC2641-16)

<table>
<thead>
<tr>
<th>DIGITAL INPUT BINARY NUMBER IN DAC LATCH</th>
<th>ANALOG OUTPUT ( (V_{\text{OUT}}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
</tr>
<tr>
<td>1111 1111 1111 11xx</td>
<td>( V_{\text{REF}} ) (16,383/16,384)</td>
</tr>
<tr>
<td>1000 0000 0000 00xx</td>
<td>( V_{\text{REF}} ) ((8,192/16,384) = V_{\text{REF}}/2 )</td>
</tr>
<tr>
<td>0000 0000 0000 01xx</td>
<td>( V_{\text{REF}} ) (1/16,384)</td>
</tr>
<tr>
<td>0000 0000 0000 00xx</td>
<td>0V</td>
</tr>
</tbody>
</table>

Table 1b. 14-Bit Unipolar Binary Code Table (LTC2641-14)

<table>
<thead>
<tr>
<th>DIGITAL INPUT BINARY NUMBER IN DAC LATCH</th>
<th>ANALOG OUTPUT ( (V_{\text{OUT}}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
</tr>
<tr>
<td>1111 1111 1111 11xx</td>
<td>( V_{\text{REF}} ) (16,383/16,384)</td>
</tr>
<tr>
<td>1000 0000 0000 00xx</td>
<td>( V_{\text{REF}} ) ((8,192/16,384) = V_{\text{REF}}/2 )</td>
</tr>
<tr>
<td>0000 0000 0000 01xx</td>
<td>( V_{\text{REF}} ) (1/16,384)</td>
</tr>
<tr>
<td>0000 0000 0000 00xx</td>
<td>0V</td>
</tr>
</tbody>
</table>

Table 1c. 12-Bit Unipolar Binary Code Table (LTC2641-12)

<table>
<thead>
<tr>
<th>DIGITAL INPUT BINARY NUMBER IN DAC LATCH</th>
<th>ANALOG OUTPUT ( (V_{\text{OUT}}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
</tr>
<tr>
<td>1111 1111 1111 xxxxx</td>
<td>( V_{\text{REF}} ) (4,095/4,096)</td>
</tr>
<tr>
<td>1000 0000 0000 xxxxx</td>
<td>( V_{\text{REF}} ) ((2,048/4,096) = V_{\text{REF}}/2 )</td>
</tr>
<tr>
<td>0000 0000 0001 xxxxx</td>
<td>( V_{\text{REF}} ) (1/4,096)</td>
</tr>
<tr>
<td>0000 0000 0000 xxxxx</td>
<td>0V</td>
</tr>
</tbody>
</table>
Bipolar Configuration

Figure 3 shows a typical bipolar DAC application for the LTC2642. The on-chip bipolar offset/gain resistors, R_FB and R_INV, are connected to an external amplifier to produce a bipolar output swing from –V_REF to V_REF at the R_FB pin.

The amplifier circuit provides a gain of +2 from the V_OUT pin, and gain of –1 from V_REF. Tables 2a, 2b and 2c show the bipolar offset binary code tables for 16-bit, 14-bit and 12-bit operation.

Figure 3. 16-Bit Bipolar Output (LTC2642-16) V_OUT = –V_REF to V_REF

Table 2a. 16-Bit Bipolar Offset Binary Code Table (LTC2642-16)

<table>
<thead>
<tr>
<th>DIGITAL INPUT</th>
<th>ANALOG OUTPUT (V_OUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
</tr>
<tr>
<td>1111 1111 1111 1111</td>
<td>V_REF (32,767/32,768)</td>
</tr>
<tr>
<td>1000 0000 0000 0000</td>
<td>V_REF (1/32,768)</td>
</tr>
<tr>
<td>1000 0000 0000 0000</td>
<td>0V</td>
</tr>
<tr>
<td>0111 1111 1111 1111</td>
<td>–V_REF (1/32,768)</td>
</tr>
<tr>
<td>0000 0000 0000 0000</td>
<td>–V_REF</td>
</tr>
</tbody>
</table>

Table 2b. 14-Bit Bipolar Offset Binary Code Table (LTC2642-14)

<table>
<thead>
<tr>
<th>DIGITAL INPUT</th>
<th>ANALOG OUTPUT (V_OUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
</tr>
<tr>
<td>1111 1111 1111 11xx</td>
<td>V_REF (8,191/8,192)</td>
</tr>
<tr>
<td>1000 0000 0000 01xx</td>
<td>V_REF (1/8,192)</td>
</tr>
<tr>
<td>1000 0000 0000 00xx</td>
<td>0V</td>
</tr>
<tr>
<td>0111 1111 1111 11xx</td>
<td>–V_REF (1/8,192)</td>
</tr>
<tr>
<td>0000 0000 0000 00xx</td>
<td>–V_REF</td>
</tr>
</tbody>
</table>

Table 2c. 12-Bit Bipolar Offset Binary Code Table (LTC2642-12)

<table>
<thead>
<tr>
<th>DIGITAL INPUT</th>
<th>ANALOG OUTPUT (V_OUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB</td>
<td>LSB</td>
</tr>
<tr>
<td>1111 1111 1111 xxxx</td>
<td>V_REF (2.047/2.048)</td>
</tr>
<tr>
<td>1000 0000 0001 xxxx</td>
<td>V_REF (1/2.048)</td>
</tr>
<tr>
<td>1000 0000 0000 xxxx</td>
<td>0V</td>
</tr>
<tr>
<td>0111 1111 1111 xxxx</td>
<td>–V_REF (1/2048)</td>
</tr>
<tr>
<td>0000 0000 0000 xxxx</td>
<td>–V_REF</td>
</tr>
</tbody>
</table>
Unbuffered Operation and VOUT Loading

The DAC output is available directly at the VOUT pin, which swings from GND to VREF. Unbuffered operation provides the lowest possible offset, full-scale and linearity errors, the fastest settling time and minimum power consumption.

However, unbuffered operation requires that appropriate loading be maintained on the VOUT pin. The LTC2641/LTC2642 VOUT can be modeled as an ideal voltage source in series with a source resistance of ROUT, typically 6.2k (Figure 4). The DAC’s linear output impedance allows it to drive medium loads (RL > 60k) without degrading INL or DNL; only the gain error is increased. The gain error (GE) caused by a load resistance, RL, (relative to full scale) is:

\[
GE = \frac{-1}{1 + \left(\frac{R_{OUT}}{R_L}\right)}
\]

In 16-bit LSBs:

\[
GE = -\frac{65536}{1 + \left(\frac{R_{OUT}}{R_L}\right)} [\text{LSB}]
\]

ROUT has a low tempco (typically \(< ±50\text{ppm/°C})\), and is independent of DAC code. The variation of ROUT, part-to-part, is typically less than ±20%.

Note on LSB units:

For the following error descriptions, “LSB” means 16-bit LSB and 65,536 is rounded to 66k.

To convert to 14-bit LSBs (LTC2641-14/LTC2642-14) divide by 4.

To convert to 12-bit LSBs (LTC2641-12/LTC2642-12) divide by 16.

A constant current, IL, loading VOUT will produce an offset of:

\[
V_{OFFSET} = -I_L \cdot R_{OUT}
\]

For \(V_{REF} = 2.5V\), a 16-bit LSB equals \(2.5V/65,536\), or 38µV. Since \(R_{OUT}\) is 6.2k, an \(I_L\) of 6nA produces an offset of 1LSB. Therefore, to avoid degrading DAC performance, it is critical to protect the VOUT pin from any sources of leakage current.

Unbuffered VOUT Settling Time

The settling time at the VOUT pin can be closely approximated by a single-pole response where:

\[
\tau = R_{OUT} \cdot (C_{OUT} + C_L)
\]

(Figure 4). Settling to \(1/2\)LSB at 16-bits requires about 12 time constants \((\ln(2) \cdot 65,536))\). The typical settling time of 1µs corresponds to a time constant of 83ns, and a total \((C_{OUT} + C_L)\) of about 83ns/6.2k = 13pF. The internal capacitance, \(C_{OUT}\) is typically 10pF, so an external \(C_L\) of 3pF corresponds to 1µs settling to \(1/2\)LSB.

Op Amp Selection

The optimal choice for an external buffer op amp depends on whether the DAC is used in the unipolar or bipolar mode of operation, and also depends on the accuracy, speed, power dissipation and board area requirements of the application. The LTC2641/LTC2642’s combination of tiny package size, rail-to-rail single supply operation, low power dissipation, fast settling and nearly ideal accuracy specifications makes it impractical for one op amp type to fit every application.

In bipolar mode (LTC2642 only), the amplifier operates with the internal resistors to provide bipolar offset and scaling. In this case, a precision amplifier operating from dual power supplies, such as the the LT1678 provides the \(±V_{REF}\) output range (Figure 3).

In unipolar mode, the output amplifier operates as a unity gain voltage follower. For unipolar, single supply applications a precision, rail-to-rail input, single supply op amp
such as the LTC6078 is suitable, if the application does not require linear operation very near to GND, or zero scale (Figure 2). The LTC6078 typically swings to within 1mV of GND if it is not required to sink any load current. For an LSB size of 38µV, 1mV represents 26 missing codes near zero scale. Linearity will be degraded over a somewhat larger range of codes above GND. It is also unavoidable that settling time and transient performance will degrade whenever a single supply amplifier is operated very close to GND, or to the positive supply rail.

The small LSB size of a 16-bit DAC, coupled with the tight accuracy specifications on the LTC2641/LTC2642, means that the accuracy and input specifications for the external op amp are critical for overall DAC performance.

**Op Amp Specifications and Unipolar DAC Accuracy**

Most op amp accuracy specifications convert easily to DAC accuracy.

Op amp input bias current on the noninverting (+) input is equivalent to an I_L loading the DAC V_OUT pin and therefore produces a DAC zero-scale error (ZSE) (see Unbuffered Operation):

\[
ZSE = -I_B(IN+) \cdot R_{OUT} \text{ [Volts]}
\]

In 16-bit LSBs:

\[
ZSE = -I_B(IN+) \cdot 6.2k \cdot \left(\frac{66k}{V_{REF}}\right) \text{ [LSB]}
\]

Op amp input impedance, R_{IN}, is equivalent to an R_L loading the LTC2641/LTC2642 V_OUT pin, and produces a gain error of:

\[
GE = \frac{-66k}{1 + \left(\frac{6.2k}{R_{IN}}\right)} \text{ [LSB]}
\]

Op amp offset voltage, V_{OS}, corresponds directly to DAC zero code offset error, ZSE:

\[
ZSE = V_{OS} \cdot \left(\frac{66k}{V_{REF}}\right) \text{ [LSB]}
\]

Temperature effects also must be considered. Over the −40°C to 85°C industrial temperature range, an offset voltage temperature coefficient (referenced to 25°C) of 0.6µV/°C will add 1LSB of zero-scale error. Also, I_{BIAS} and the V_{OFFSET} error it causes, will typically show significant relative variation over temperature.

Op amp open-loop gain, A_VOL, contributes to DAC gain error (GE):

\[
GE = \frac{66k}{A_{VOL}} \text{ [LSB]}
\]

Op amp input common mode rejection ratio (CMRR) is an input-referred error that corresponds to a combination of gain error (GE) and INL, depending on the op amp architecture and operating conditions. A conservative estimate of total CMRR error is:

\[
\text{Error} = \left(10^{\frac{\text{CMRR}}{20}}\right) \cdot \left(\frac{V_{\text{CMRR}_\text{Range}}}{V_{\text{REF}}}\right) \cdot 66k \text{ [LSB]}
\]

where \(V_{\text{CMRR}_\text{Range}}\) is the voltage range that CMRR (in dB) is specified over. Op amp Typical Performance Characteristics graphs are useful to predict the impact of CMRR errors on DAC performance. Typically, a precision op amp will exhibit a fairly linear CMRR behavior (corresponding to DAC gain error only) over most of the common mode input range (CMR), and become nonlinear and produce significant errors near the edge of the CMR.

Rail-to-rail input op amps are a special case, because they have 2 distinct input stages, one with CMR to GND and the other with CMR to V⁺. This results in a “crossover” CM input region where operation switches between the two input stages.

The LTC6078 rail-to-rail input op amp typically exhibits remarkably low crossover linearity error, as shown in the V_{OS} vs V_{CM} Typical Performance Characteristics graphs (see the LTC6078 data sheet). Crossover occurs at CM inputs about 1V below V⁺, and an LTC6078 operating as a unipolar DAC buffer with V_{REF} = 2.5V and V⁺ = 5V will typically add only about 1LSB of GE and almost no INL error due to CMRR. Even in a full rail-to-rail application, with V_{REF} = V⁺ = 5V, a typical LTC6078 will add only about 1LSB of INL at 16-bits.
Op Amp Specifications and Bipolar DAC Accuracy

The op amp contributions to unipolar DAC error discussed above apply equally to bipolar operation. The bipolar application circuit gains up the DAC span, and all errors, by a factor of 2. Since the LSB size also doubles, the errors in LSBs are identical in unipolar and bipolar modes.

One added error in bipolar mode comes from $I_B (\text{IN}^-)$, which flows through $R_{FB}$ to generate an offset. The full bias current offset error becomes:

\[
V_{OFFSET} = (I_B (\text{IN}^-) \cdot R_{FB} - I_B (\text{IN}^+) \cdot R_{OUT} \cdot 2) \text{ [Volts]}
\]

So:

\[
V_{OFFSET} = \left( I_B (\text{IN}^-) \cdot \frac{28k}{12.4k} \cdot \frac{33k}{V_{REF}} \right) \text{ [LSB]}
\]

Settling Time with Op Amp Buffer

When using an external op amp, the output settling time will still include the single pole settling on the LTC2641/LTC2642 $V_{OUT}$ node, with time constant $R_{OUT} \cdot (C_{OUT} + C_L)$ (see Unbuffered $V_{OUT}$ Settling Time). $C_L$ will include the buffer input capacitance and PC board interconnect capacitance.

The external buffer amplifier adds another pole to the output response, with a time constant equal to $(f_{bandwidth}/2\pi)$. For example, assume that $C_L$ is maintained at the same value as above, so that the $V_{OUT}$ node time constant is $83ns = 1\mu s/12$. The output amplifier pole will also have a time constant of $83ns$ if the closed-loop bandwidth equals $(1/2\pi \cdot 83ns) = 1.9MHz$. The effective time constant of two cascaded single-pole sections is approximately the root square sum of the individual time constants, or $\sqrt{2} \cdot 83ns = 117ns$, and $1/2$ LSB settling time will be $-12 \cdot 117ns = 1.4\mu s$. This represents an ideal case, with no slew limiting and ideal op amp phase margin. In practice, it will take a considerably faster amplifier, as well as careful attention to maintaining good phase margin, to approach the unbuffered settling time of $1\mu s$.

The output settling time for bipolar applications (Figure 3) will be somewhat increased due to the feedback resistor network $R_{FB}$ and $R_{INV}$ (each 28k nominal). The parasitic capacitance, $C_P$, on the op amp (–) input node will introduce a feedback loop pole with a time constant of $(C_P \cdot 28k/2)$. A small feedback capacitor, $C_1$, should be included, to introduce a zero that will partially cancel this pole. $C_1$ should nominally be $<C_P$, typically in the range of 5pF to 10pF. This will restore the phase margin and improve coarse settling time, but a pole-zero doublet will unavoidably leave a slower settling tail, with a time constant of roughly $(C_P + C_1) \cdot 28k/2$, which will limit 16-bit settling time to be greater than $2\mu s$.

Reference and GND Input

The LTC2641/LTC2642 operates with external voltage references from 2V to $V_{DD}$, and linearity, offset and gain errors are virtually unchanged vs $V_{REF}$. Full 16-bit performance can be maintained if appropriate guidelines are followed when selecting and applying the reference. The LTC2641/LTC2642’s very low gain error tempco of 0.1ppm/°C, typical, corresponds to less than 0.5LSB variation over the –40°C to 85°C temperature range. In practice, this means that the overall gain error tempco will be determined almost entirely by the external reference tempco.

The DAC voltage-switching mode “inverted” resistor ladder architecture used in the LTC2641/LTC2642 exhibits a reference input resistance ($R_{REF}$) that is code dependent (see the Typical Performance curves $I_{REF}$ vs Input Code).

In unipolar mode, the minimum $R_{REF}$ is 14.8k (at code 871Chex, 34,588 decimal) and the maximum $R_{REF}$ is 300k at code 0000hhex (zero scale). The maximum change in $I_{REF}$ for a 2.5V reference is 160µA. Since the maximum occurs near midscale, the INL error is about half of the change on $V_{REF}$, so maintaining an INL error of $<0.1$LSB requires a reference load regulation of $(1.53ppm \cdot 2/160\mu A) = 19 [ppm/\mu A]$. This implies a reference output impedance of 48mΩ, including series wiring resistance.

To prevent output glitches from occurring when resistor ladder branches switch from GND to $V_{REF}$, the reference input must maintain low impedance at higher frequencies. A 0.1µF ceramic capacitor with short leads between REF and GND provides high frequency bypassing. A surface mount ceramic chip capacitor is preferred because it has the lowest inductance. An additional 1µF between REF and GND provides low frequency bypassing. The circuit will benefit from even higher bypass capacitance, as long
as the external reference remains stable with the added capacitive loading.

Digital Inputs and Interface Logic
All of the digital inputs include Schmitt-trigger buffers to accept slow transition interfaces. This means that optocouplers can interface directly to the LTC2641/LTC2642 without additional external logic. Digital input hysteresis is typically 150mV.

The digital inputs are compatible with TTL/CMOS-logic levels. However, rail-to-rail (CMOS) logic swings are preferred, because operating the logic inputs away from the supply rails generates additional I DD and GND current, (see Typical Performance Characteristic graph Supply Current vs Logic Input Voltage).

Digital feedthrough is only 0.2nV•s typical, but it is always preferred to keep all logic inputs static except when loading a new code into the DAC.

Board Layout for Precision
Even a small amount of board leakage can degrade accuracy. The 6nA leakage current into V OUT needed to generate 1LSB offset error corresponds to 833MΩ leakage resistance from a 5V supply.

The V OUT node is relatively sensitive to capacitive noise coupling, so minimum trace length, appropriate shielding and clean board layout are imperative here.

Temperature differences at the DAC, op amp or reference pins can easily generate tens of microvolts of thermocouple voltages. Analog signal traces should be short, close together and away from heat dissipating components. Air currents across the board can also generate thermocouples.

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane.

A “star ground” area should be established by attaching the LTC2641/LTC2642 GND pin, V REF GND and the DAC V OUT GND reference terminal to the same area on the GND plane. Care should be taken to ensure that no large GND return current paths flow through the “star GND” area. In particular, the resistance from the LTC2641 GND pin to the point where the V REF input source connects to the ground plane should be as low as possible. Excessive resistance here will be multiplied by the code dependent I REF current to produce an INL error similar to the error produced by V REF source resistance. For the LTC2641 in the S8 package both GND pins, Pin 2 and Pin 7 should be tied to the same GND plane.

Sources of ground return current in the analog area include op amp power supply bypass capacitors and the GND connection for single supply amps. A useful technique for minimizing errors is to use a separate board layer for power ground return connections, and reserve one ground plane layer for low current “signal” GND connections. The “signal”, or “star” GND plane must connected to the “power” GND plane at a single point, which should be located near the LTC2641/LTC2642 GND pin.

If separate analog and digital ground areas exist it is necessary to connect them at a single location, which should be fairly close to the DAC for digital signal integrity. In some systems, large GND return currents can flow between the digital and analog GNDs, especially if different PC boards are involved. In such cases the digital and analog ground connection point should not be made right at the “star” GND area, so the highly sensitive analog signals are not corrupted. If forced to choose, always place analog ground quality ahead of digital signal ground. (A few mV of noise...
APPLICATIONS INFORMATION

on the digital inputs is imperceptible, thanks to the digital input hysteresis)

Just by maintaining separate areas on the GND plane where analog and digital return currents naturally flow, good results are generally achieved. Only after this has been done, it is sometimes useful to interrupt the ground plane with strategically placed “slots”, to prevent the digital ground currents from fringing into the analog portion of the plane. When doing this, the gap in the plane should be only as long as it needs to be to serve its purpose.

Caution: if a GND plane gap is improperly placed, so that it interrupts a significant GND return path, or if a signal traces crosses over the gap, then adding the gap may greatly degrade performance! In this case, the GND and signal return currents are forced to flow the long way around the gap, and then are typically channeled directly into the most sensitive area of the analog GND plane.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADEd AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

For more information www.linear.com/LTC2641
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

For more information www.linear.com/LTC2641
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

OBsolete package
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661 Rev F)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
## REVISION HISTORY

(Revision history begins at Rev C)

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