



ESDALC6V1xxM6

4 and 5 line low capacitance TRANSIL™ array for ESD protection

Main applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Features

- 4 unidirectional TRANSIL diodes (ESDALC6V1M6)
- 5 unidirectional TRANSIL diodes (ESDALC6V1-5M6)
- Breakdown Voltage $V_{BR} = 6.1 \text{ V min}$
- Low diode capacitance (12 pF typ at 0 V)
- Low leakage current $< 70 \text{ nA}$
- Very small PCB area: 1.45 mm^2
- 500 microns pitch
- Leadfree package

Description

The ESDALC6V1xxM6 is monolithic arrays designed to protect up to 4 or 5 lines against ESD transients.

The device is ideal for applications where both reduced print circuit board space and power absorption capability are required.

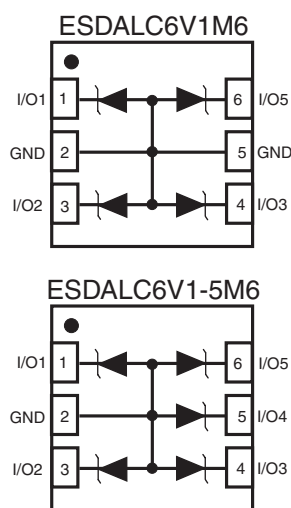
Benefits

- High ESD protection level
- High integration
- Suitable for high density boards



Micro QFN Package

Functional diagram



Order Code

Part number	Marking
ESDALC6V1M6	G
ESDALC6V1-5M6	H

Complies with the following standards:

IEC61000-4-2

15 kV (air discharge)

8 kV (contact discharge)

MIL STD 883E- Method 3015-7: class3

25 kV (human body model)

TM: TRANSIL is a trademark of STMicroelectronics

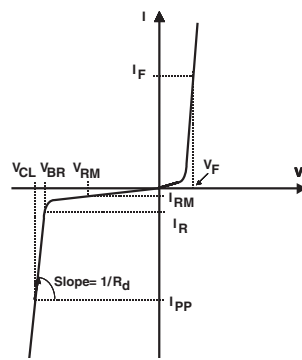
1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge – IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	± 15 ± 8	kV
P_{PP}	Peak pulse power dissipation (8/20 μ s) ⁽¹⁾	T_j initial = T_{amb} 30	W
I_{pp}	Repetitive peak pulse current typical value (8/20 μ s)	3	A
T_j	Junction temperature	125	°C
T_{stg}	Storage temperature range	-55 + 150	°C
T_L	Maximum lead temperature for soldering during 10 s	260	°C
T_{OP}	Operating temperature range	-40 + 125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	
V_{RM}	Stand-off voltage	
V_{BR}	Breakdown voltage	
V_{CL}	Clamping voltage	
I_{RM}	Leakage current @ V_{RM}	
I_{PP}	Peak pulse current	
αT	Voltage temperature coefficient	
V_F	Forward voltage drop	

Parameter	Test Condition	Min	Typ	Max	Unit
V_{BR}	$I_R = 1\text{ mA}$	6.1		7.2	V
I_{RM}	$V_{RM} = 3\text{ V}$			70	nA
V_F	$I_F = 10\text{ mA}$			1	V
R_d			2	3	Ω
$\alpha T^{(1)}$	$I_R = 1\text{ mA}$,			5	$10^{-4}/\text{°C}$
C	$V_R = 0\text{ V DC}$, $F = 1\text{ MHz}$, $V_{osc} = 30\text{ mV}_{RMS}$		12	15	pF

1. $\Delta V_{BR} = \alpha T * (T_{amb} - 25\text{ °C}) * V_{BR}(25\text{ °C})$

Figure 1. Relative variation of peak pulse power versus initial junction temperature

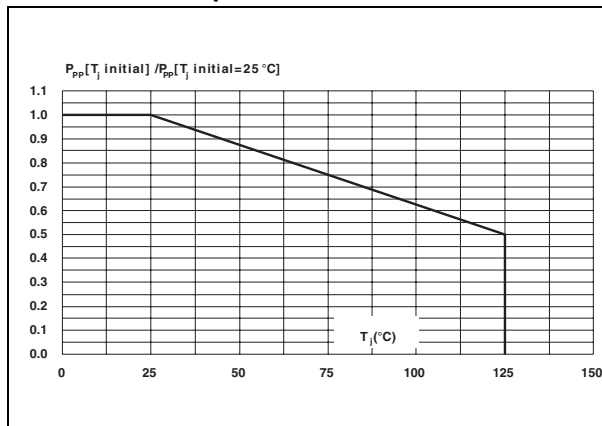


Figure 2. Peak pulse power versus exponential pulse duration

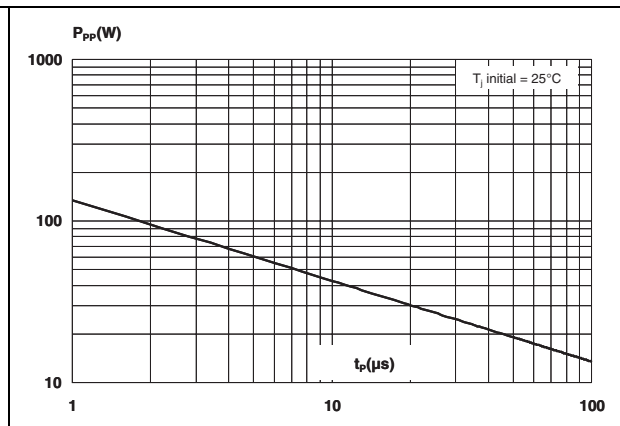


Figure 3. Clamping voltage versus peak pulse current (typical values, rectangular waveform)

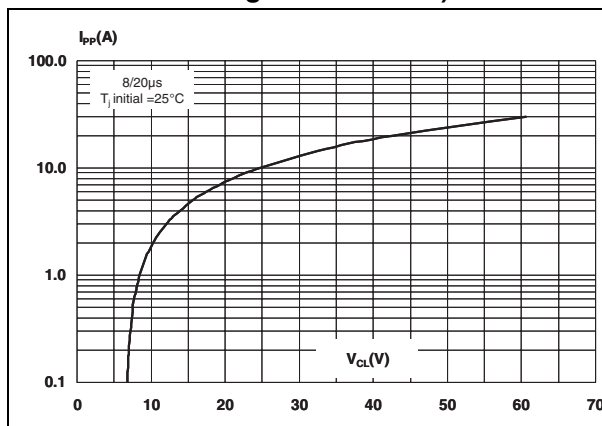


Figure 4. Forward voltage drop versus peak forward current (typical values)

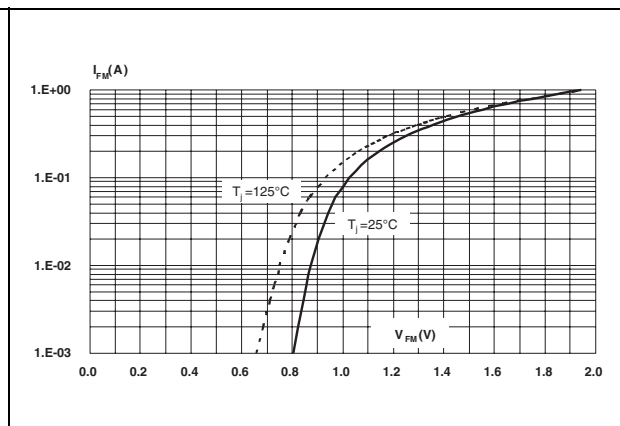


Figure 5. Junction capacitance versus reverse voltage applied (typical values)

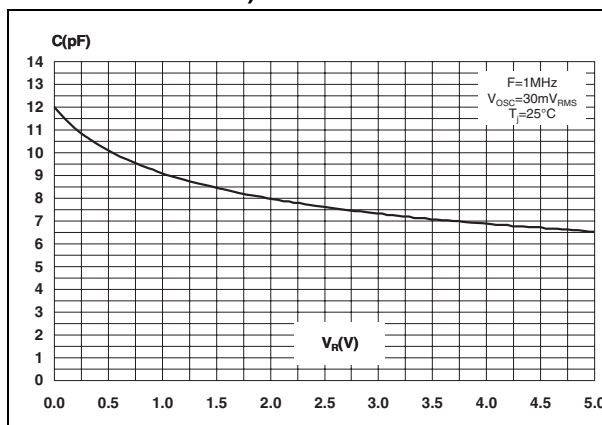


Figure 6. Relative variation of leakage current versus junction temperature (typical values)

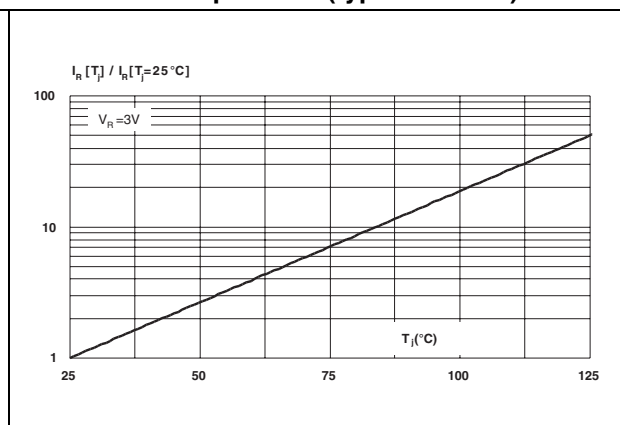


Figure 7. S21 attenuation measurement results of each channel

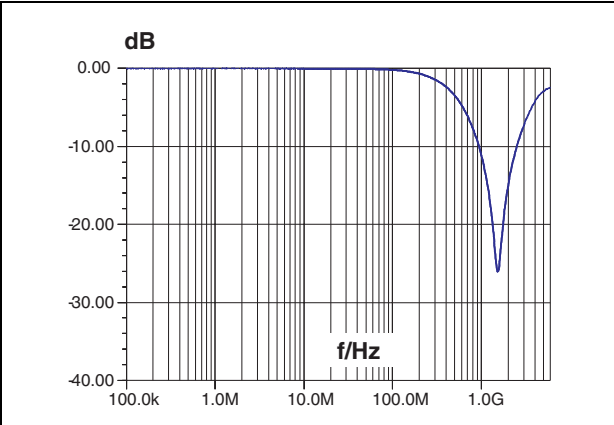


Figure 8. Analog crosstalk measurements between channels

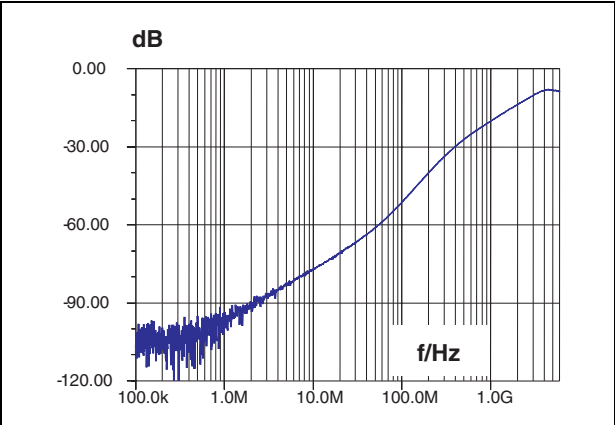


Figure 9. ESD response to IEC6100-4-2 (+15 kV air discharge) on each channel

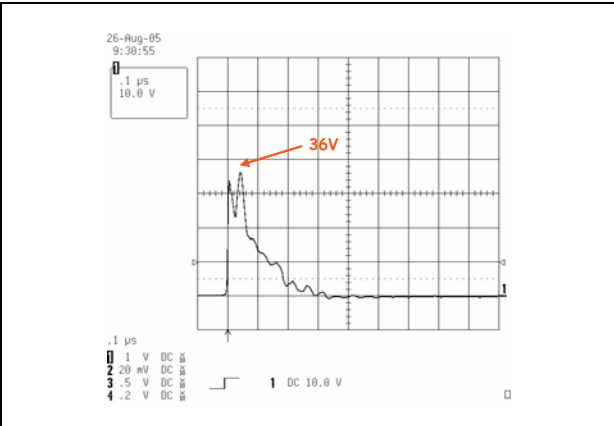
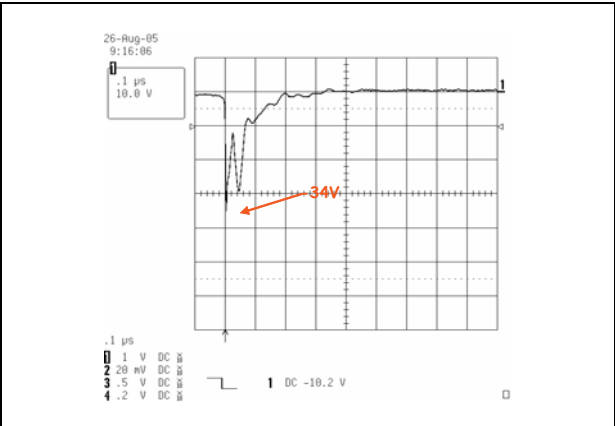


Figure 10. ESD response to IEC6100-4-2 (-15 kV air discharge) on each channel



2 Ordering information scheme

	ESDA	LC	6V1	xx	M6
ESD Array					
Low capacitance					
Breakdown voltage 6V1 = 6.1 Volts min					
Number of lines blank = 4 line -5 = 5 line protection					
Package M6 = Micro QFN 6 leads					

3 Package information

- Epoxy meets UL94, V0

Table 3. Mechanical data

REF	DIMENSIONS					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	0.20	0.22	0.24
A1	0.00	0.02	0.05	0.00	0.01	0.02
b	0.19	0.25	0.30	0.07	0.10	0.12
D	1.34	1.45	1.51	0.53	0.57	0.59
E	0.94	1.00	1.05	0.37	0.39	0.41
e	0.45	0.50	0.55	0.18	0.20	0.22
k	0.25	0.30	0.35	0.10	0.12	0.14
L	0.30	0.35	0.40	0.12	0.14	0.16

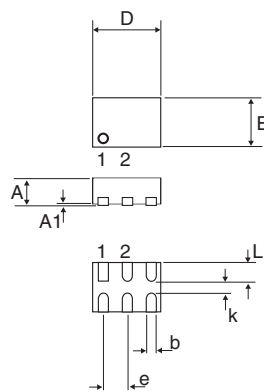


Figure 11. Footprint

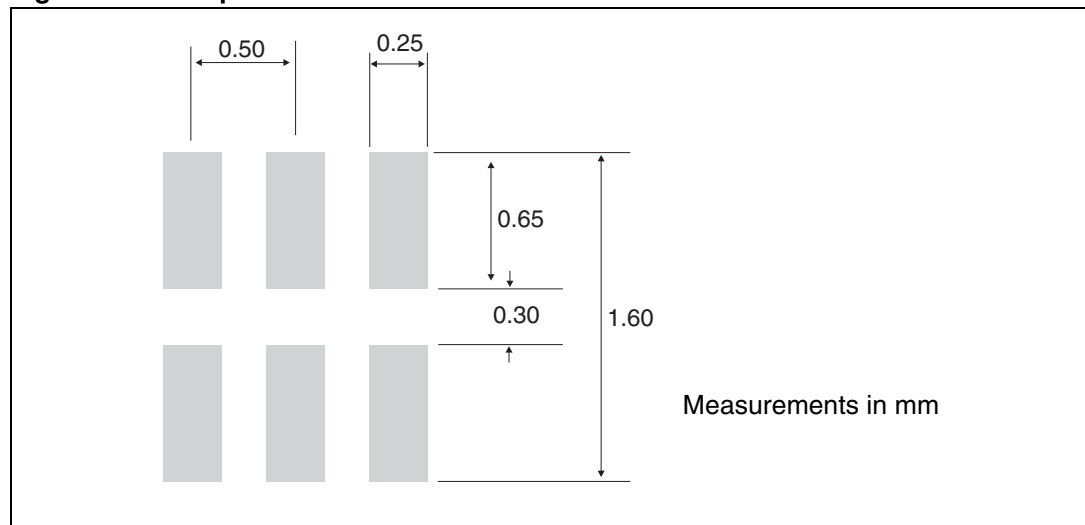
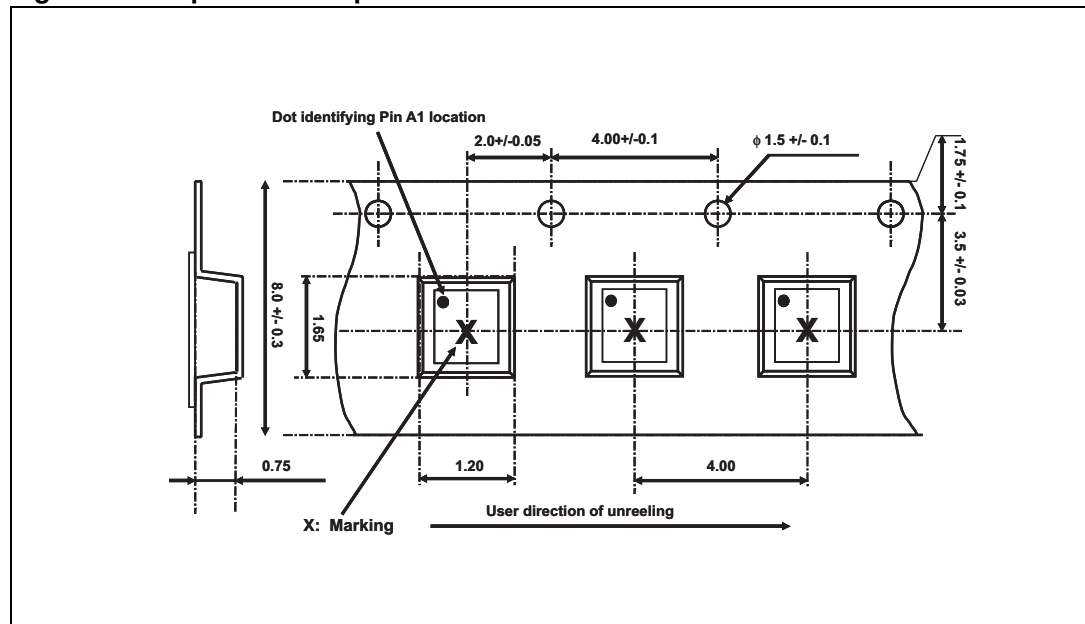


Figure 12. Tape and reel specification



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1M6	G	Micro QFN	2.2 mg	30,000	Tape and reel
ESDALC6V1-5M6	H	Micro QFN	2.2 mg	30,000	Tape and reel

5 Revision history

Date	Revision	Changes
19-Sep-2005	1	Initial release.
10-Oct-2005	2	Package title changed from DFN to QFN. No technical changes.
21-Dec-2005	3	Updated package dimensions in Table 1.
01-Fev-2007	4	Reformatted to current standard. Added note on marking rotation in section 3. Package information.

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