

3.125 Gbps LVDS Buffers with Pre-emphasis and Equalization (DS25BR100/110/120) Evaluation Kit

USER MANUAL

Part Number: DS25BR100EVK

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March 2007 Rev. 0.1

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Overview

The DS25BR100EVK is an evaluation kit designed for demonstrating performance of the 3.125 Gbps LVDS Single Channel Buffers with Transmit Pre-emphasis and Receive Equalization family (DS25BR100, DS25BR110 and DS25BR120). The evaluation kit provides all three devices on a single board and three FR4 striplines (14 (~35), 28 (~75) and 42 (~105) inches (cm) in length) for exercising devices' signal conditioning features (pre-emphasis and equalization).

The purpose of this document is to: familiarize you with the DS25BR100EVK, suggest the test setup procedures and instrumentation, and guide you through some typical measurements that demonstrate performance of the chipset in typical applications.



DS25BR100EVK Description

Figure 1 shows the top layer drawing of the PCB with the silkscreen annotations. It is a 4.5 by 4.5 inch eight-layer PCB that has a three-device layout capable of demonstrating performance and all features of the DS25BR100, DS25BR110 and DS25BR120. In addition, three microstrips allow easy evaluation of transmit pre-emphasis and receive equalization.

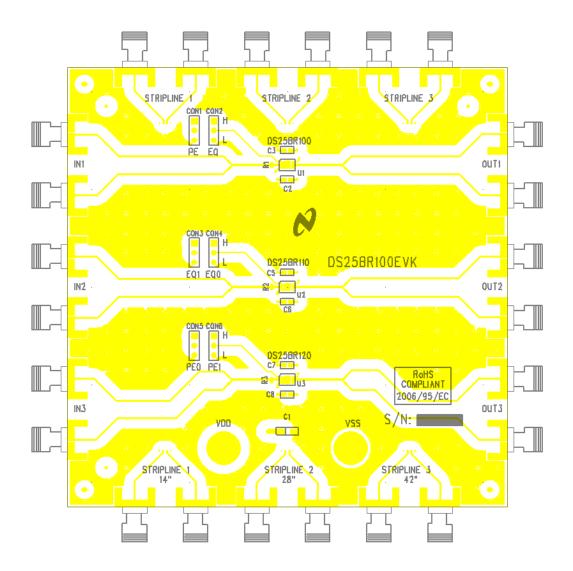


Figure 1. Driver Board

| Connector | Device | Function |
|------------|--------|-----------------------|
| CON1, CON2 | U1 | Select PE or EQ Level |
| CON3, CON4 | U2 | Select EQ Level |
| CON5, CON6 | U3 | Select PE Level |

Table 1. Driver Board Connector-Device-Function Cross Reference

DS25BR100 (U1) Evaluation

The DS25BR100 is a 3.125 Gbps LVDS buffer featuring two levels of transmit pre-emphasis (Off and Medium) and two levels of receive equalization (Low and Medium). The following is a recommended test setup procedure for the device evaluation. Figure 2 depicts a typical setup and instrumentation used for the device evaluation.

- 1. Apply the power to the device (3.3V typical) between VDD and VSS banana plug receptacles.
- 2. Connect desired STRIPLINE(s) to the input and / or output of the device using short 50-ohm coaxial cables (e.g. PE-SR402-AL from www.pasternack.com).
- 3. Connect a signal source (i.e. signal generator or an LVDS driver) to the IN1 inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations.
- 4. Select equalization level by setting the EQ pin (CON2) to L (for Low setting) or H (for Medium setting).
- 5. If a STRIPLINE is connected to the device outputs, select pre-emphasis level by setting the PE pin (CON1) to L (for Off setting) or H (for Medium setting)
- 6. Connect the OUT1 outputs to an oscilloscope and view the output signals with an oscilloscope with the bandwidth of at least 5 GHz.

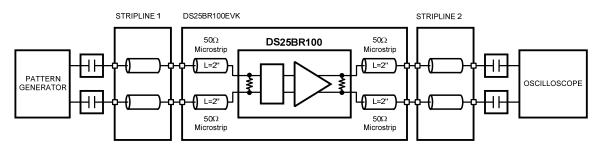


Figure 2. DS25BR100 Test Setup Example

DS25BR110 (U2) Evaluation

The DS25BR110 is a 3.125 Gbps LVDS buffer featuring four levels of receive equalization (Off, Low, Medium and High). The following is a recommended test setup procedure for the device evaluation. Figure 3 depicts a typical setup and instrumentation used for the device evaluation.

- 1. Apply the power to the device (3.3V typical) between VDD and VSS banana plug receptacles.
- 2. Connect desired STRIPLINE to the input of the device using short 50-ohm coaxial cables (e.g. PE-SR402-AL from www.pasternack.com).
- 3. Connect a signal source (i.e. signal generator or an LVDS driver) to the IN2 inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations.
- 4. Select equalization level by setting the EQ0 (CON4) and EQ1 (CON3) pins to L or H. Refer to Table 2.

| EQ1 | EQ0 | Equalization Level |
|-----|-----|--------------------|
| 0 | 0 | Off |
| 0 | 1 | Low |
| 1 | 0 | Medium |
| 1 | 1 | High |

 Table 2. Equalization Level Selection

5. Connect the OUT2 outputs to an oscilloscope and view the output signals with an oscilloscope with the bandwidth of at least 5 GHz.

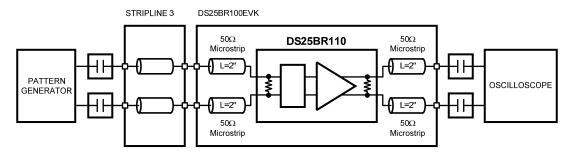


Figure 3. DS25BR110 Test Setup Example

DS25BR120 (U3) Evaluation

The DS25BR120 is a 3.125 Gbps LVDS buffer featuring four levels of transmit pre-emphasis (Off, Low, Medium and High). The following is a recommended test setup procedure for the device evaluation. Figure 4 depicts a typical setup and instrumentation used for the device evaluation.

- 1. Apply the power to the device (3.3V typical) between VDD and VSS banana plug receptacles.
- 2. Connect desired STRIPLINE to the output of the device using short 50-ohm coaxial cables (e.g. PE-SR402-AL from www.pasternack.com).
- 3. Connect a signal source (i.e. signal generator or an LVDS driver) to the IN3 inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations.
- 4. Select pre-emphasis level by setting the PE0 (CON5) and PE1 (CON6) pins to L or H. Refer to Table 3.

| PE1 | PE0 | Pre-emphasis Level |
|-----|-----|--------------------|
| 0 | 0 | Off |
| 0 | 1 | Low |
| 1 | 0 | Medium |
| 1 | 1 | High |

 Table 3. Pre-emphasis Level Selection

5. Connect the OUT3 outputs to an oscilloscope and view the output signals with an oscilloscope with the bandwidth of at least 5 GHz.

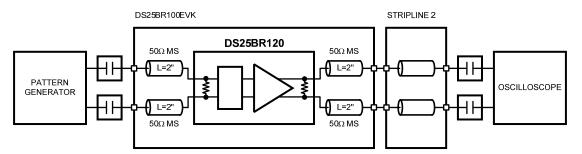
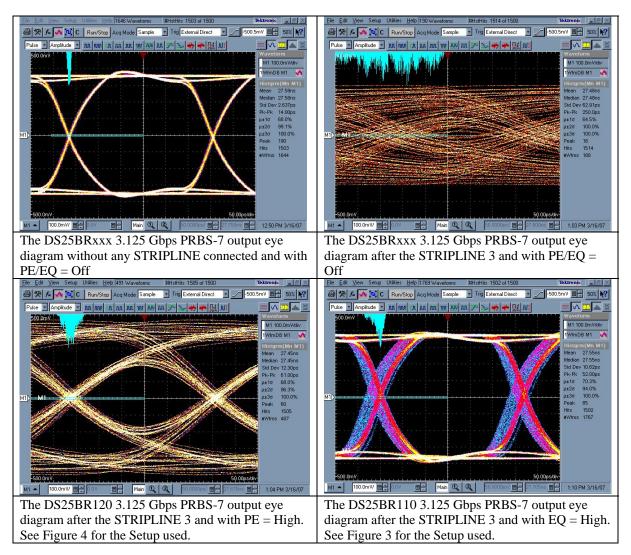


Figure 4. DS25BR120 Test Setup Example

Typical Performance

This section of the User Manual shows typical eye diagrams you can expect to see when evaluating the DS25BR100EVK.



| ENERCON - BILL OF MATERIALS | | | PCBA, DS25BR100EVK , ROHS | | | | PL Number:Rev:Rev By:Rev Date:PL Status:Z3016-012BJ3/1/2007Released | | | | | | | |
|-----------------------------|----------------------|-------------------|---------------------------|-------|----------------------------------------------------------------------------------------|-----|---------------------------------------------------------------------|-----------------------------------|----|-----------------------------------------------------------------------------------------------|----------------------|--|--|--|
| | Product: BA, DS25 | BR100EVK, ROHS | | | PCBA, DS25BR TOUEVR , RONS | | ponsib | sible Eng/Mgr: Creator: Arlene | | ox Creation | n Date: 26 / 2006 | | | |
| ltem | Part Type | Part Number/Value | Mfg | NoSub | Description | Qty | SMT | Ref D | es | Notes | Rev | | | |
| | PCB | P-05479R0 | | | DS25BR100: 4.50x4.50x.062in, 8 layer | 1 | | | | Bd: (114.30x 114.30mm) Panel: (4.50x13.70in (114.30x 347.98mm) 3 bds/panel | | | | |
| 2 | | | | _ | | | | | | a strange | | | | |
| 3 | IC | DS25BR100TSD | NAT | | | 1 | X | Ul | | Customer Supplied | 0 | | | |
| 4 | IC | DS25BR110TSD | NAT | | | 1 | х | U2 | | Customer Supplied | | | | |
| 5 | IC | DS25BR120TSD | NAT | | | 1 | X | U3 | | U3 Customer Supplied | | | | |
| 6 | | | | | | | | | | | | | | |
| 7 | | | | | | | | | | | | | | |
| 8 | CAP | 06035C103KAT | AVX | | .01µF, 50V, ±10%, 0603, Ceramic, X7R, Pb-Free | 3 | x | C2,6,8 | | | 0 | | | |
| | <alt></alt> | C0603C103K5RAC | KEMET | | .01µF, 50V, ±10%, 0603, Ceramic, X7R, Pb-Free | | | | | | | | | |
| | <alt></alt> | ECJ-1VB1H103K | PANA | | .01µF, 50V, ±10%, 0603, Ceramic, X7R, Pb-Free | | | | | | | | | |
| 9 | CAP | 0603YC104KAT | AVX | | $.1\mu\text{F},$ 16V, ±10%, 0603, Ceramic, X7R, Pb-Free | 3 | X | C3,5,7 | | | 0 | | | |
| | <alt></alt> | C0603C104K3RAC | KEMET | | $.1\mu\text{F},~25\text{V},~\pm10\%,~0603,~\text{Ceramic},~\text{X7R},~\text{Pb-Free}$ | | | | | | | | | |
| | <alt></alt> | C0603C104K4RAC | KEMET | | $.1\mu\text{F},$ 16V, ±10%, 0603, Ceramic, X7R, Pb-Free | | | | | | | | | |
| | <alt></alt> | ECJ-1VB1C104K | PANA | | .1µF, 16V, ±10%, 0603, Ceramic, X7R, Pb- Free | | | | | | | | | |
| | <alt></alt> | ECJ-1VB1E104K | PANA | | .1μF, 25V, ±10%, 0603, Ceramic, X7R, Pb- Free | | | | | | | | | |
| 10 | CAP | TAJA106K016 | AVX | | 10µF, 16V, ±10%, A-Case, Tantalum, Pb- Free | 1 | x | C1 | | | 0 | | | |
| | <alt></alt> | T491A106K016AT | KEMET | | 10μF, 16V, ±10%, A-Case, Tantalum, Pb- Free | | | | | | | | | |
| 11 | | | | | | | | | | | | | | |

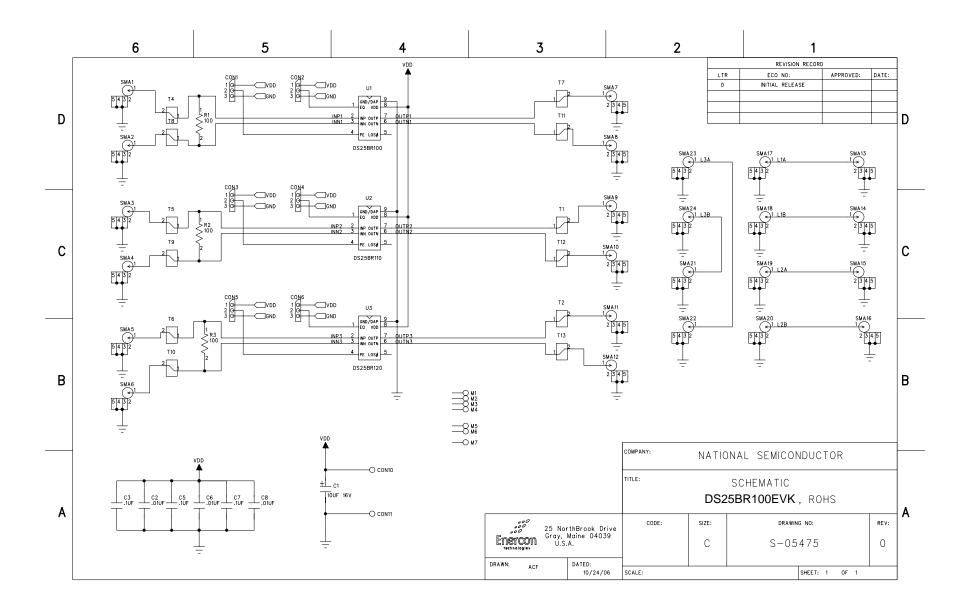
1:21:12 PM, 3/9/2007

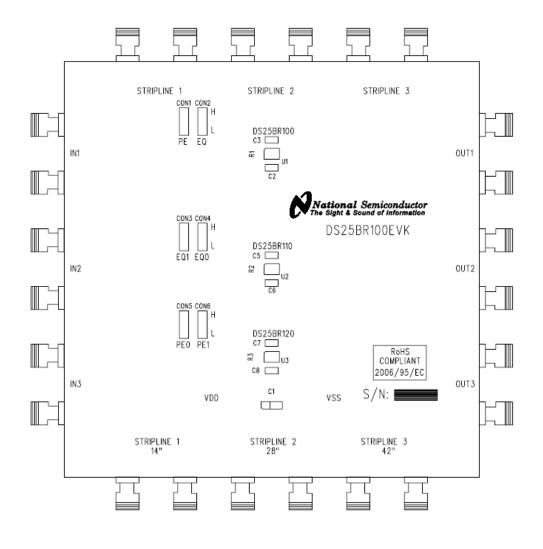
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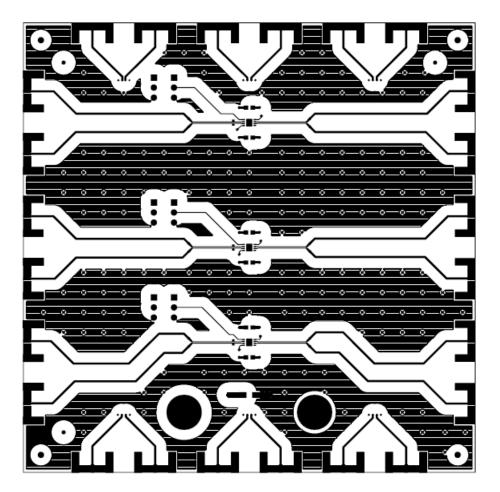
| El | VERC | ON - BILL OF MA | TERIALS | | | | lumbei)16– | :: Rev: R 01 2 B | | Rev Date 3 / 1 / 2 | | PL Status: Release | ed |
|------|----------------------|-------------------|---------|-------|------------------------------------------|---------------------------------------|-----------------------|---------------------|-------|-----------------------|---------------------------|-----------------------|-----|
| | Product: BA, DS25 | BR100EVK , rohs | | | PCBA, DS25BR100EVK , ROHS | · · · · · · · · · · · · · · · · · · · | | | | | Creation Date:Fox10/26/20 | | |
| Item | Part Type | Part Number/Value | Mfg | NoSub | Description | Qty | SMT | Re | f Des | | | Notes | Rev |
| 12 | CONN | 142-0701-851 | EMERSON | | SMA, Jack Receptacle, 50 OHM, Pb-Free | 24 | | SMA1-24 | | | | | 0 |
| 13 | CONN | 3267 | POMONA | | Banana, 1p, Female, Pb-Free | 2 | | CON10,11 | 1 | | | | 0 |
| 14 | CONN | TSW-103-07-G-S | SAMTEC | | Header, 3p, Male, .100"sp, Gold, Pb-Free | 6 CON1-6 | | CON1-6 | | | 0 | | |
| 15 | | | | | | | | | | | | | |
| 16 | STENCL | T-05481R0 | ENERCON | | STENCIL FABRICATION, DS25BR100-EVK, ROHS | 1 | | | | | | | 0 |
| 17 | | | | | | | | | | | | | |
| 18 | REF | C-05480R0 | ENERCON | | FABRICATION DWG, DS25BR100-EVK, ROHS | | | | | | | | 0 |
| 19 | REF | S-05475R0 | ENERCON | | SCHEMATIC, DS25BR100-EVK, ROHS | | | | | | | | 0 |
| 20 | REF | C-05491R0 | ENERCON | | PALLET DWG, DS25BR100-EVK, ROHS | | | | | | | | 0 |

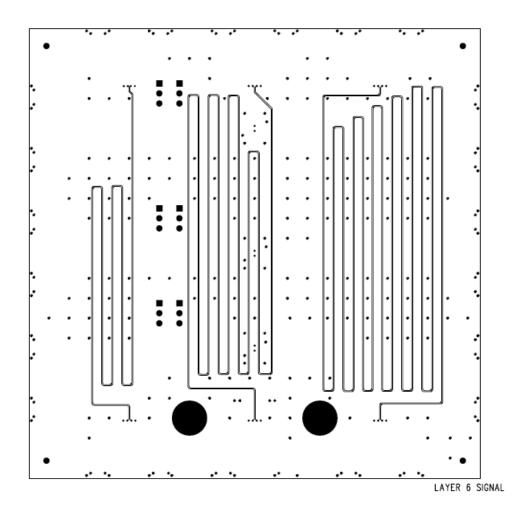
Notes:

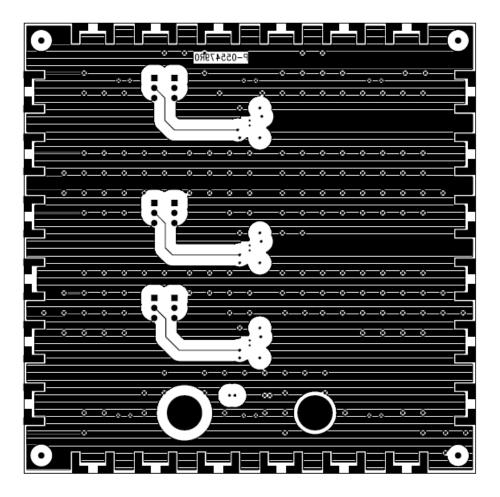
Do Not Stuff Resistors R1, R2, and R3











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