

AN-1659 LM2735X SEPIC 6-Pin WSON Demo Board

1 Introduction

This demo board converts 3V to 5.5V input to 3.3V output for up to 500mA load current using the LM2735X 1.6MHz DC-DC switching converter. This is a 2-layer board using the bottom layer as a ground plane.

A bill of materials describes the parts used on this demo board. A schematic and layout have also been included, along with measured performance characteristics. The above restrictions for the input voltage are valid only for the demo board as shipped with the demo board schematic shown in [Figure 1](#).

2 Operating Conditions

- $V_{IN} = 3V$ to $5.5V$
- $V_O = 3.3V$
- $I_O = 500mA$

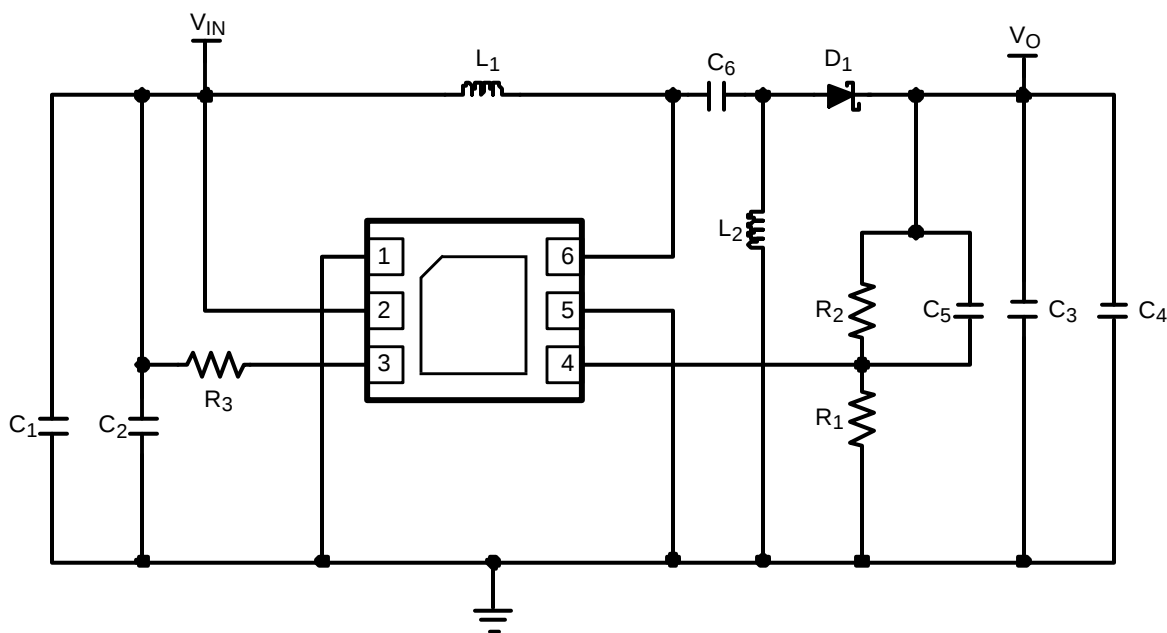


Figure 1. LM2735X 6-Pin WSON Schematic

3 Pin Description for 6-Pin WSON

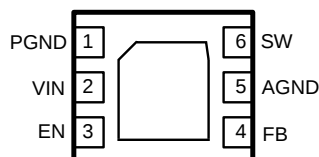


Figure 2. Pin-Out

Table 1. Pin Description

Pin	Name	Function
1	PGND	Power ground pin. Place PGND and output capacitor GND close together.
2	VIN	Supply voltage for power stage, and Input supply voltage.
3	EN	Shutdown control input. Logic high enables operation. Do not allow this pin to float or be greater than VIN + 0.3V.
4	FB	Feedback pin. Connect FB to external resistor divider to set output voltage.
5	AGND	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to pin 5
6	SW	Output switch. Connect to the inductor, output diode.
DAP	GND	Signal & Power ground. Connect to pin 1 & pin 5 on top layer. Place 4-6 via's from DAP to bottom layer GND plane.

4 Bill of Materials

Table 2. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	2.1A Boost Regulator	Texas Instruments	LM2735
C1 Input Cap	22μF, 6.3V, X5R	TDK	C2012X5R0J226M
C2 Input Cap	No Load		
C3 Output Cap	10μF, 25V, X5R	TDK	C3216X5R1E106M
C4 Output Cap	No Load		
C5 Comp Cap	2200pF	TDK	C1608X5R1H222K
C6	2.2μF 16V	TDK	C2012X5R1C225K
D1, Catch Diode	0.4V _f Schottky 1A, 20VR	ST	STPS120M
L1	6.2μH 3A	Coilcraft	MSS7341-622
L2	6.2μH 3A	Coilcraft	MSS7341-622
R1	10.2kΩ, 1%	Vishay	CRCW06031002F
R2	16.5kΩ, 1%	Vishay	CRCW06031652F
R3	100kΩ, 1%	Vishay	CRCW06031003F

5 PCB Layout

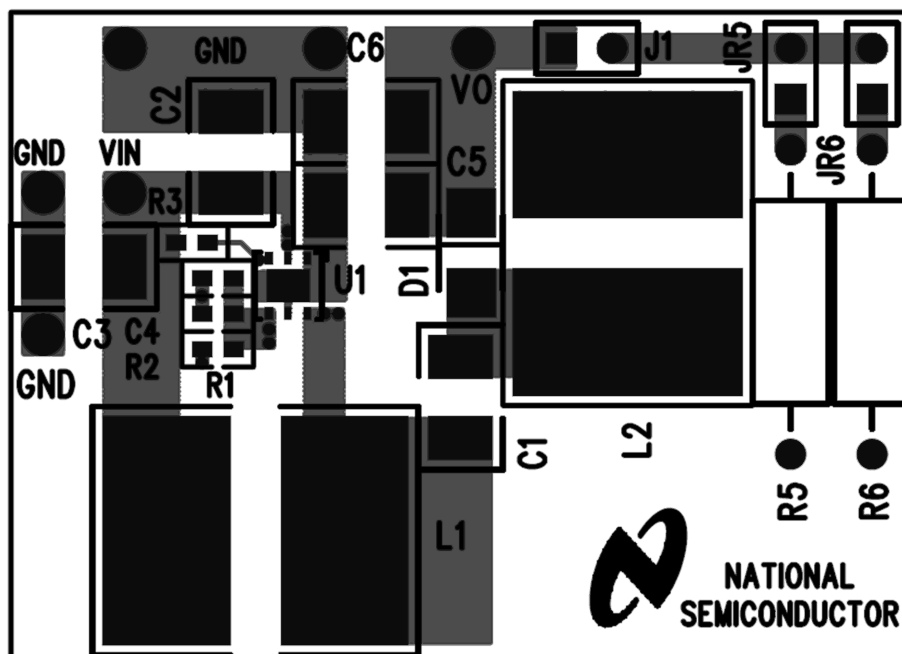


Figure 3. Top Layer

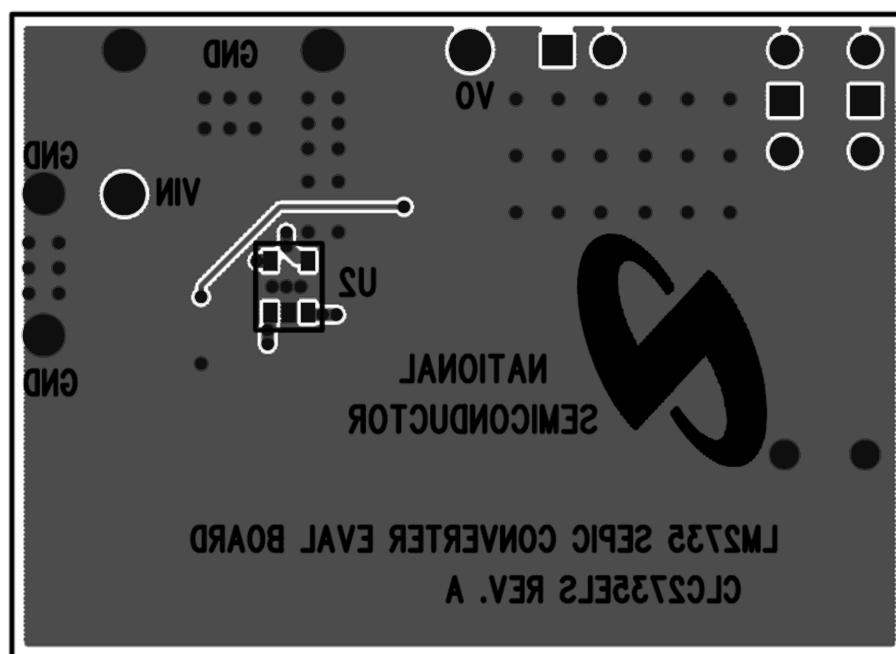


Figure 4. Bottom Layer

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