EMIF06-HSD03F3

EMI filter with integrated ESD protection for micro-SD Card™

Datasheet – production data

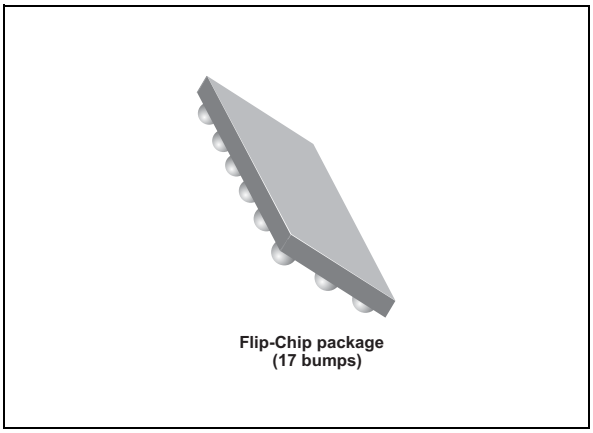


Figure 1. Pin configuration (bump side)

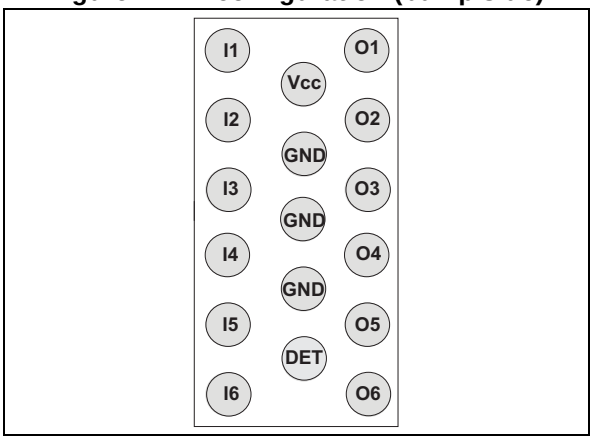
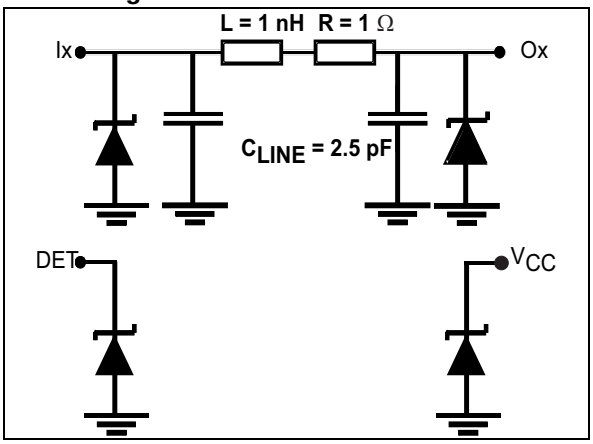


Figure 2. Functional schematic



Features

- Very low line capacitance to compensate long PCB tracks (2.5 pF typ.)
- High efficiency in ESD suppression up to 18 kV (IEC 61000-4-2)
- Very low PCB space consumption:
  - 1.1 x 2.4 mm
- Ultralow leakage current: 20 nA max.
- Very thin package: 0.605 mm
- Smart pinout for easier PCB layout
- High reduction of parasitic elements through integration and wafer level packaging
- Lead-free package

Complies with the following standards:

- IEC 61000-4-2 level 4
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

Application

- SD3.0, UHS-1 SDR104 (208 MHz)

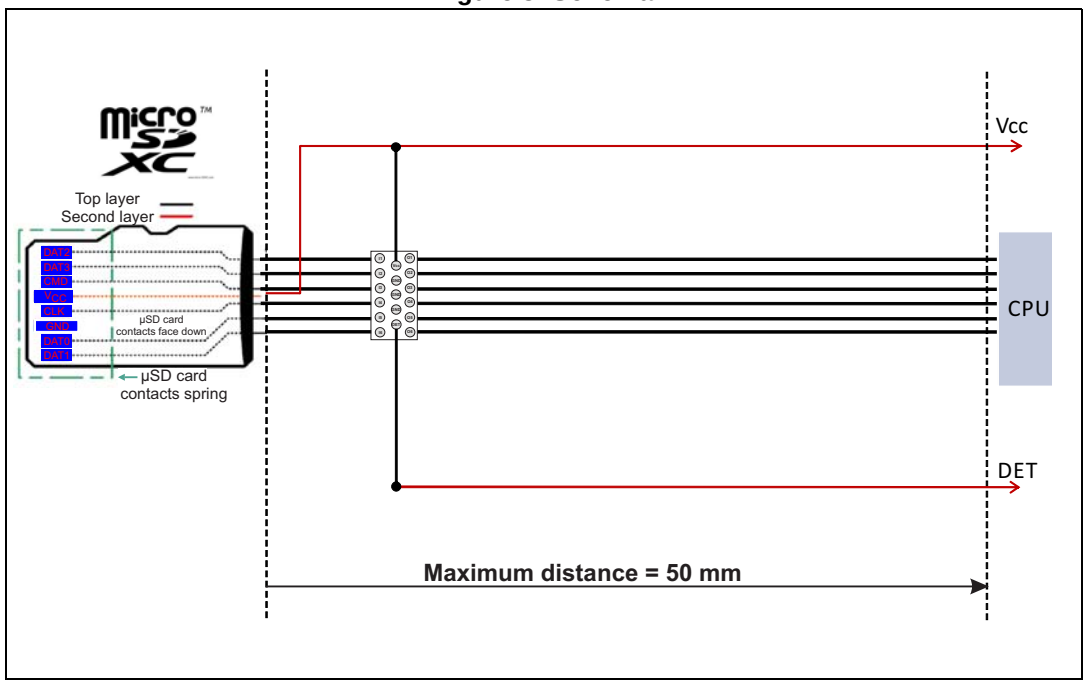
Description

The EMIF06-HSD03F3 chip is a highly integrated device designed to suppress EMI/RFI noise for interface line filtering.

The EMIF06-HSD03F3 Flip-Chip packaging means the package size is equal to the die size. That is why EMIF06-HSD03F3 is a very small device. Additionally, this filter includes ESD protection circuitry, which prevents damage to the protected device when subjected to ESD surges up 18 kV.

1 Application diagram

Figure 3. Schema



2 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, level 4 for Ix pins: Air discharge Contact discharge ESD discharge IEC 61000-4-2, level 1 for Ox pins: Air discharge Contact discharge	 18 18 10 10	kV
T_j	Maximum junction temperature	125	°C
T_{OP}	Operating temperature range	- 30 to + 85	°C
T_{stg}	Storage temperature range	- 55 to +150	°C

Figure 4. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
I_{RM}	=	Leakage current at V_{RM}
V_{RM}	=	Stand-off voltage
V_{CL}	=	Clamping voltage
I_{PP}	=	Peak pulse current
R_d	=	Dynamic resistance
C_{line}	=	Line capacitance
$R_{I/O}$	=	Series resistance between input and ouptput

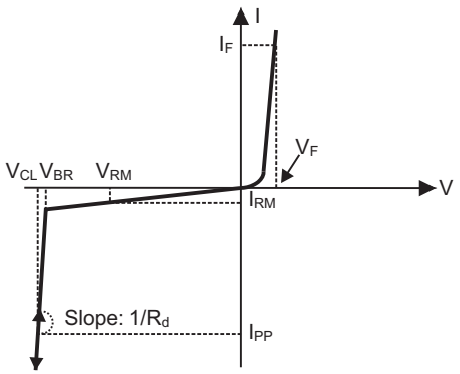


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions		Min.	Typ.	Max.	Unit
V_{BR}	Data lines, I_R = 1 mA		5		9	V
I_{RM}	V_{RM} = 3 V per line				20	nA
$R_{I/O}$				1		Ω
C_{line}	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz			2.5	3	pF
L				1		nH
Rd	Dynamics resistance, t_P = 100 ns	IO-GND (positive polarity)		650		m Ω
		GND-IO (negative polarity)		320		
V_{CC}						
V_{BR}	I_R = 1 mA		5		9	V
I_{RM}	V_{RM} = 3 V				20	nA
C_{line}	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz			40		pF
DET						
V_{BR}	I_R = 1 mA		5		9	V
I_{RM}	V_{RM} = 3 V				20	nA
C_{line}	V_{line} = 0 V, V_{osc} = 30 mV, F = 1 MHz			40		pF

Figure 5. Attenuation versus frequency I_X, O_X

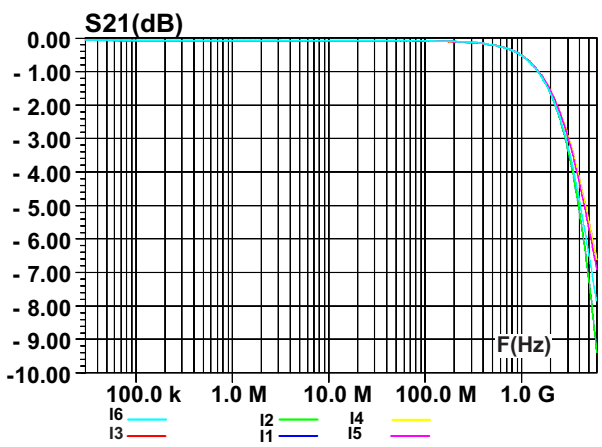


Figure 6. Attenuation versus frequency V_{CC}, DET

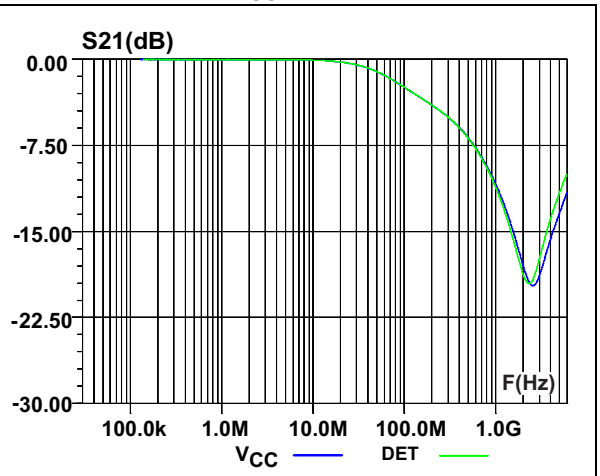


Figure 7. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

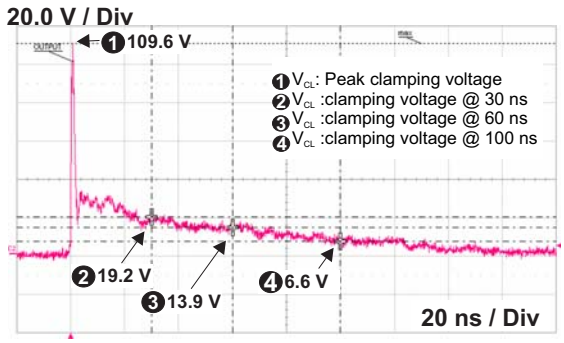


Figure 8. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

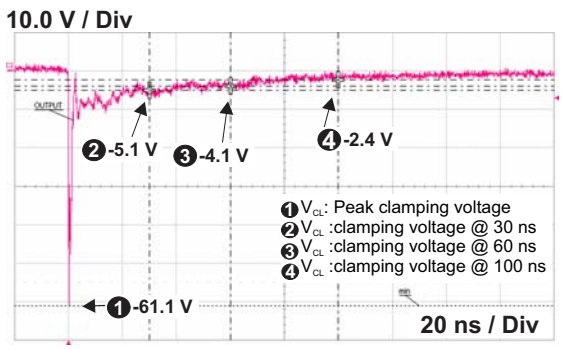


Figure 9. Digital crosstalk I1-O2

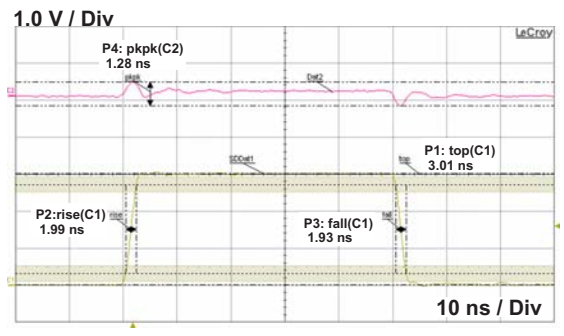


Figure 10. Analog crosstalk versus frequency

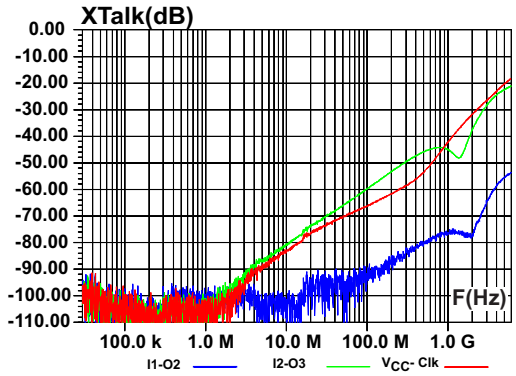
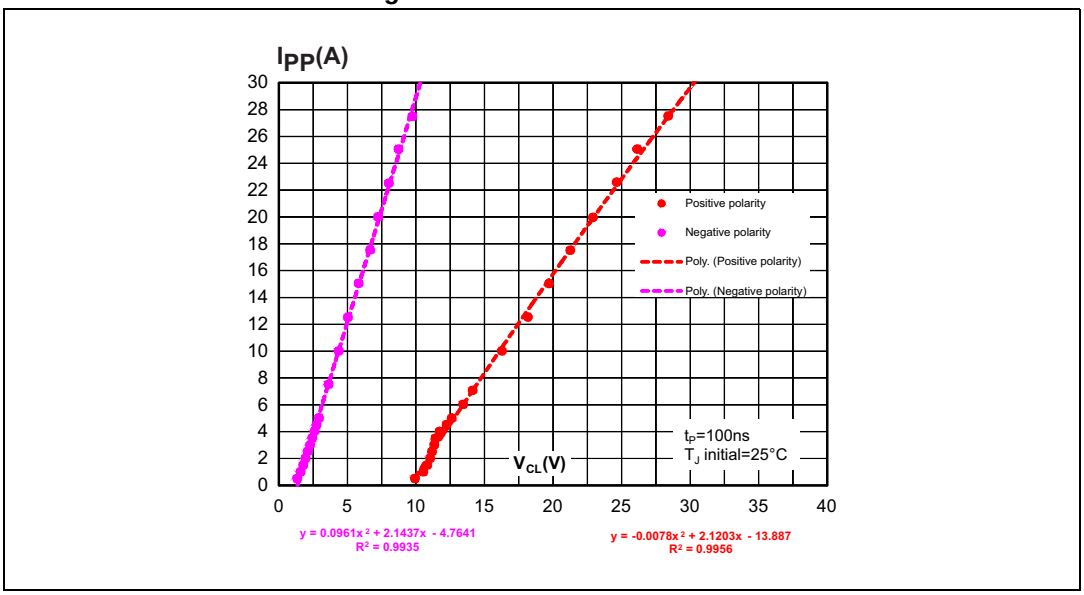


Figure 11. TLP measurement



3 Package information

- Epoxy meets UL94, V0
- Lead-free package

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Figure 12. Flip-Chip package dimensions

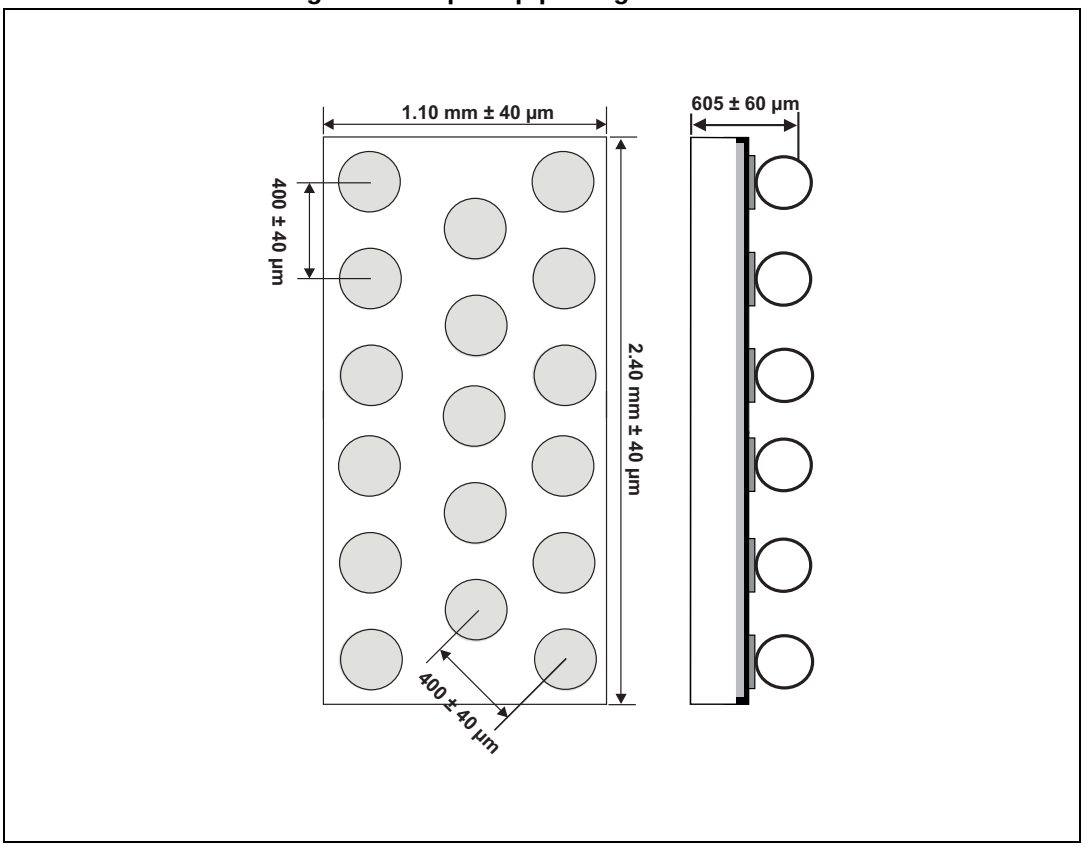


Figure 13. Footprint recommendations

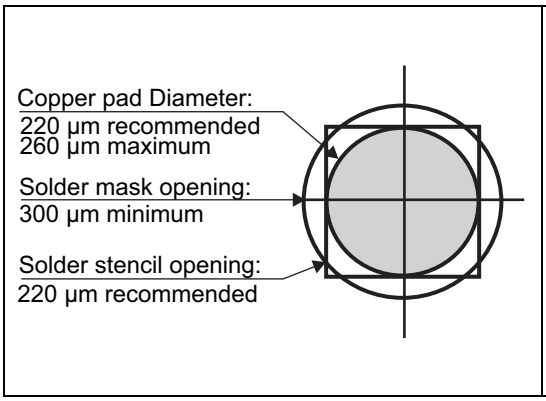


Figure 14. Marking

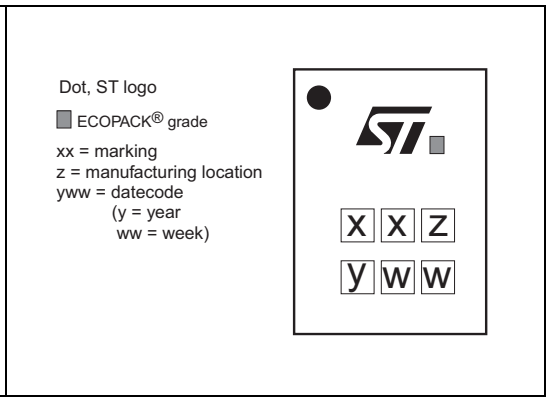
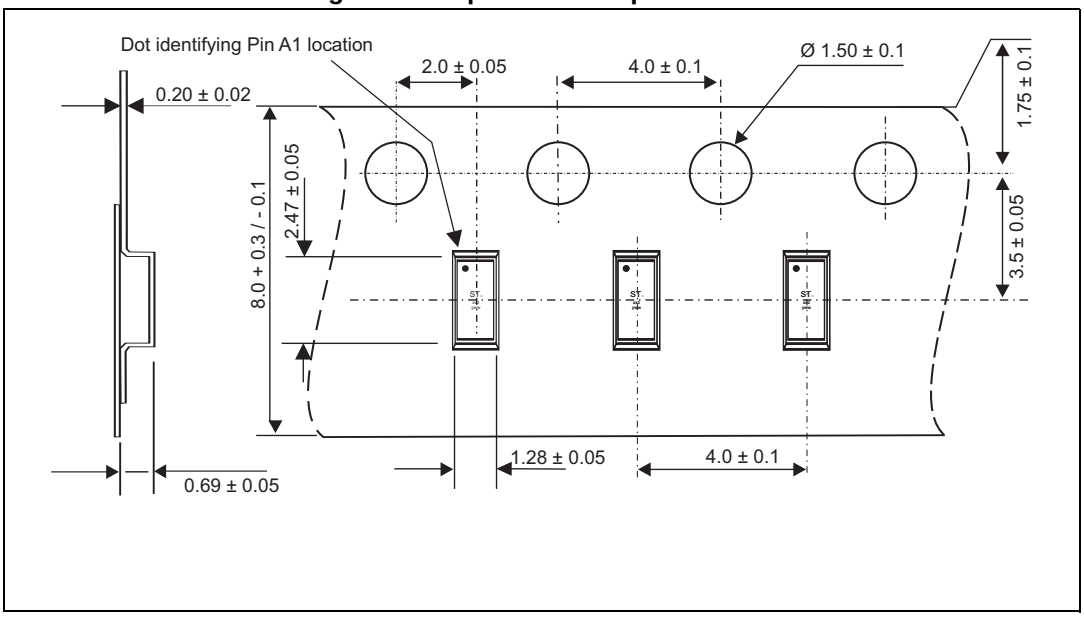


Figure 15. Tape and reel specification



Note: More information is available in the application notes:

AN2348, "IPAD™ 400 µm Flip Chip: package description and recommendations for use"

AN1751, "EMI filters: recommendations and measurements"

4 Ordering information

Figure 16. Ordering information scheme

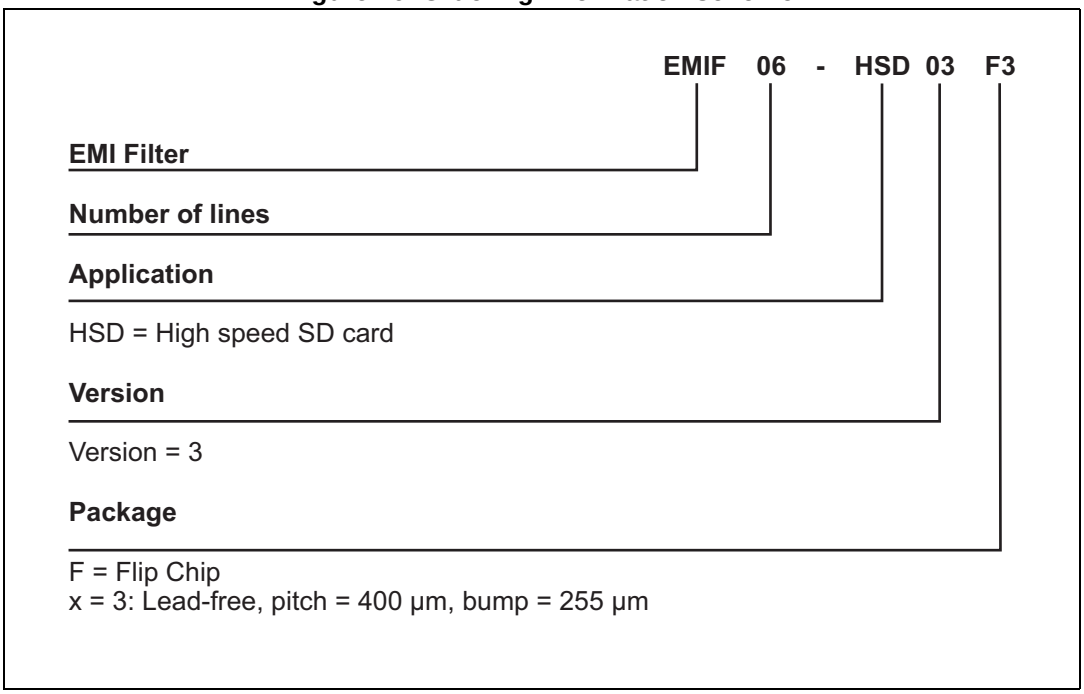


Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-HSD03F3	KK	Flip Chip	3.4 mg	5000	Tape and reel (7”)

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
19-Nov-2013	1	Initial release
10-Jan-2014	2	Reduced size of package image on coverpage, corrected typographic error in Description.

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