CSD88537ND, Dual 60 V N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD88537ND

FEATURES

- **Ultra-Low Q_g and Q_{gd}**
- **Avalanche Rated**
- **Pb Free**
- **RoHS Compliant**
- **Halogen Free**

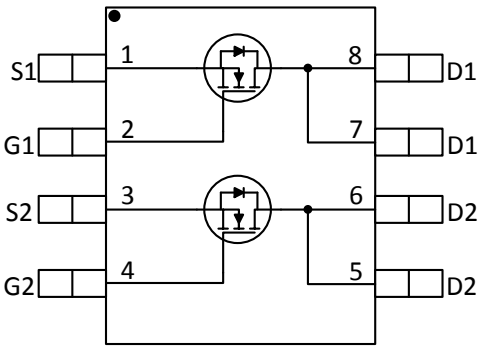
APPLICATIONS

- **Half Bridge for Motor Control**
- **Synchronous Buck Converter**

DESCRIPTION

This dual SO-8, 60 V, 12.5 mΩ NexFET™ power MOSFET is designed to serve as a half bridge in low current motor control applications.

Top View



PRODUCT SUMMARY

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	14		nC
Q_{gd}	Gate Charge Gate to Drain	2.3		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6 V	15.0	mΩ
		V_{GS} = 10 V	12.5	mΩ
$V_{GS(th)}$	Threshold Voltage	3.0		V

ORDERING INFORMATION

Device	Qty	Media	Package	Ship
CSD88537ND	2500	13-Inch Reel	SO-8 Plastic Package	Tape and Reel
CSD88537NDT	250	7-Inch Reel		

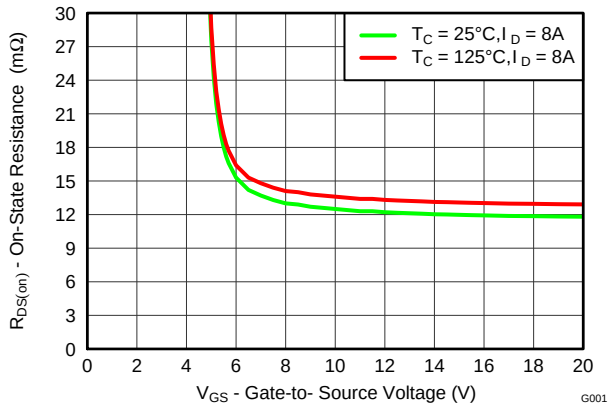
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	15	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	16	
	Continuous Drain Current (1)	8.0	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	62	A
P_D	Power Dissipation(1)	2.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 32, L = 0.1 mH, R_G = 25 Ω	51	mJ

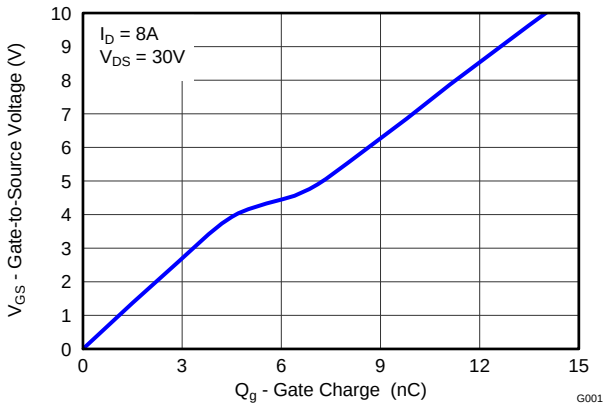
(1) Typical $R_{\theta JA}$ = 60°C/W on a 1-inch^2, 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Pulse duration ≤ 300 µs, duty cycle ≤ 2%

$R_{DS(on)}$ vs V_{GS}



GATE CHARGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.6	3.0	3.6	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6 V, I_D = 8 A		15.0	19.0	mΩ
		V_{GS} = 10 V, I_D = 8 A		12.5	15.0	mΩ
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 8 A		42		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		1080	1400	pF
C_{oss}	Output Capacitance			133	173	pF
C_{rss}	Reverse Transfer Capacitance			4.0	5.2	pF
R_G	Series Gate Resistance			5.5	11.0	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 30 V, I_D = 8 A		14	18	nC
Q_{gd}	Gate Charge Gate to Drain			2.3		nC
Q_{gs}	Gate Charge Gate to Source			4.6		nC
$Q_{g(th)}$	Gate Charge at V_{th}			3.4		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V		25		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 8 A, R_G = 0 Ω		6		ns
t_r	Rise Time			15		ns
$t_{d(off)}$	Turn Off Delay Time			5		ns
t_f	Fall Time			19		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 8 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 30 V, I_F = 8 A, di/dt = 300 A/µs		50		nC
t_{rr}	Reverse Recovery Time			30		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JL}$	Thermal Resistance Junction to Lead(1)			20	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)(2)			75	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

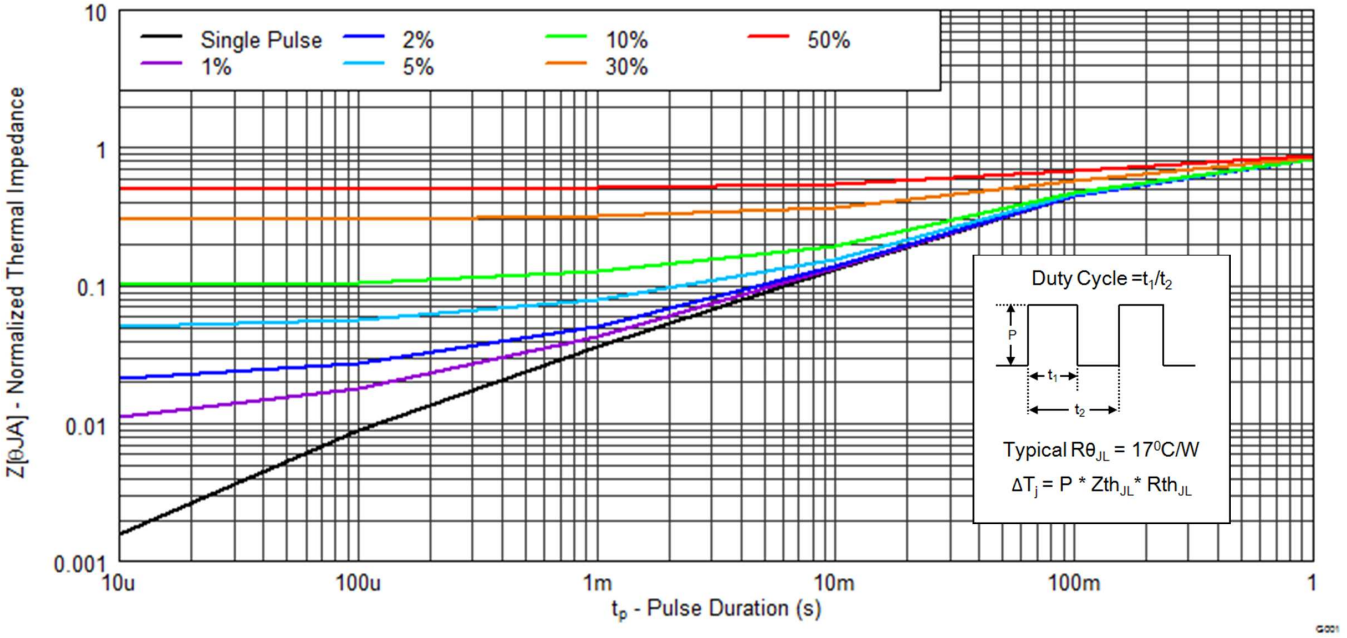


Figure 1. Transient Thermal Impedance

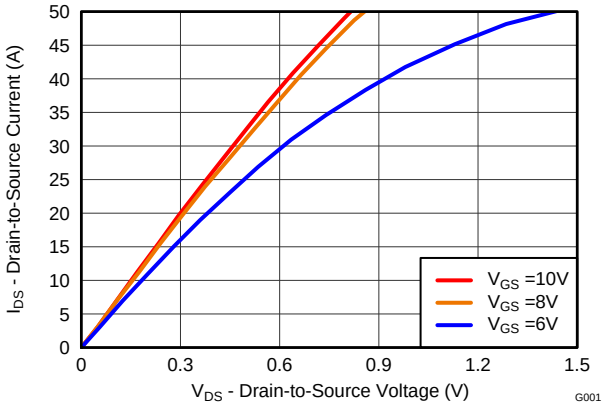


Figure 2. Saturation Characteristics

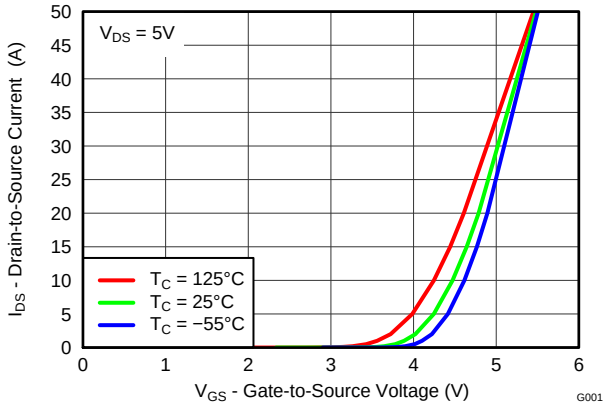


Figure 3. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

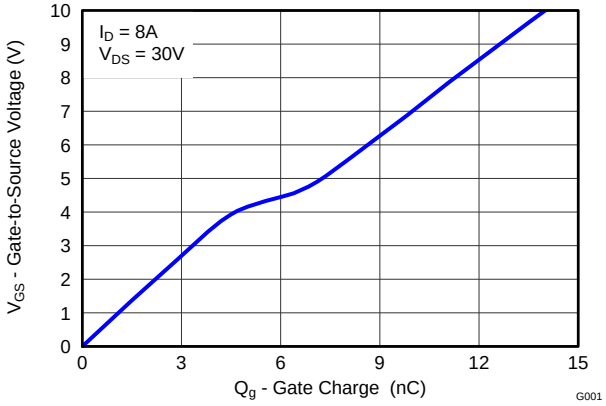


Figure 4. Gate Charge

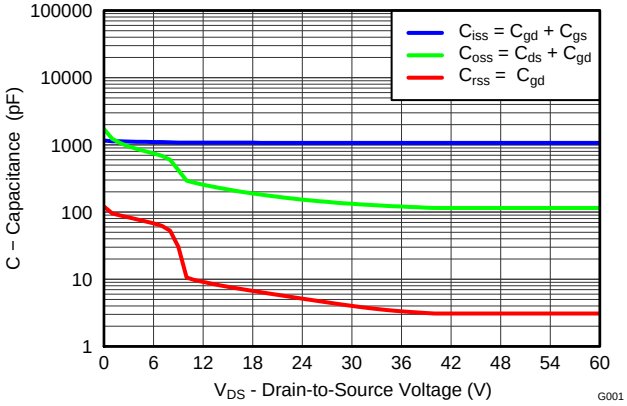


Figure 5. Capacitance

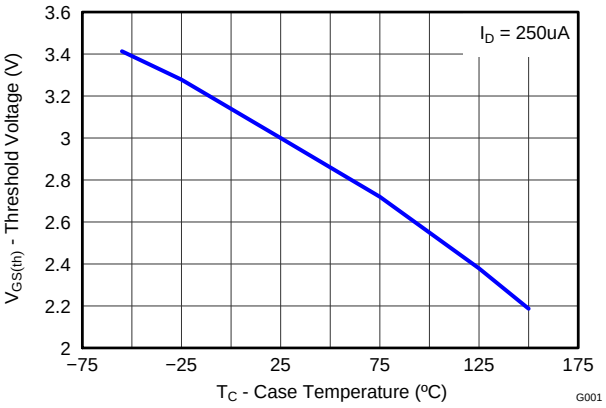


Figure 6. Threshold Voltage vs Temperature

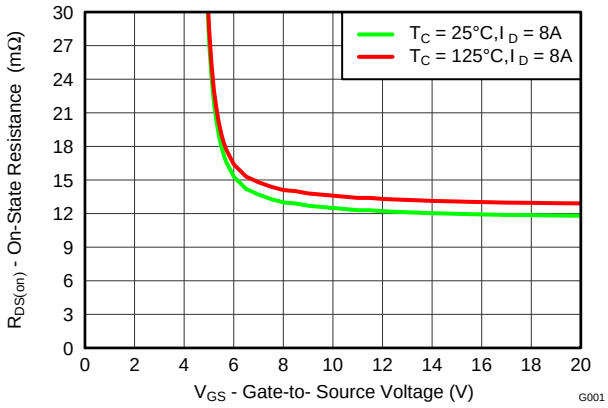


Figure 7. On-State Resistance vs Gate-to-Source Voltage

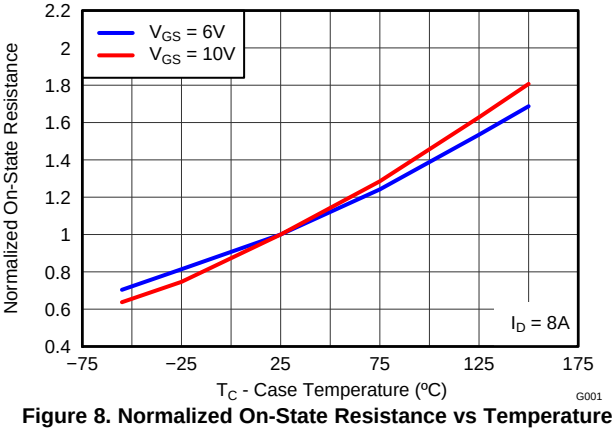


Figure 8. Normalized On-State Resistance vs Temperature

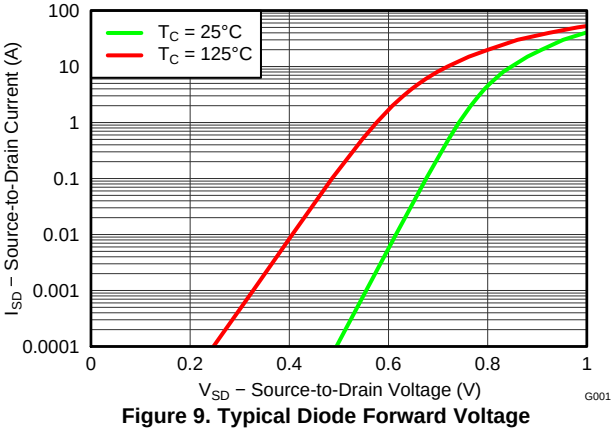


Figure 9. Typical Diode Forward Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

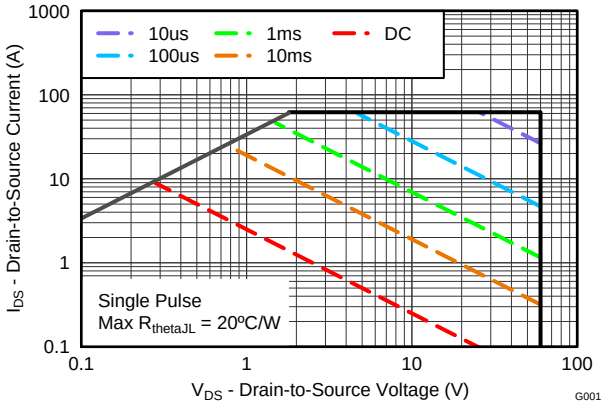


Figure 10. Maximum Safe Operating Area

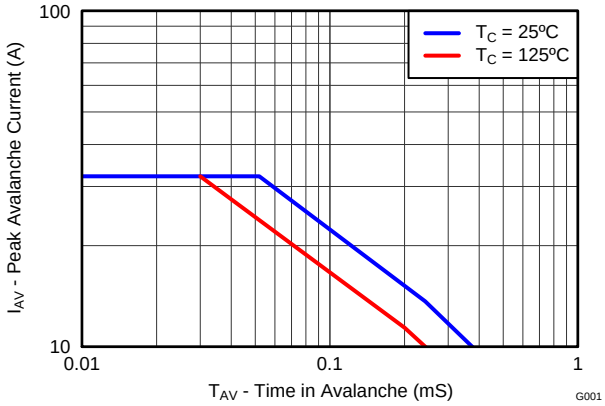


Figure 11. Single Pulse Unclamped Inductive Switching

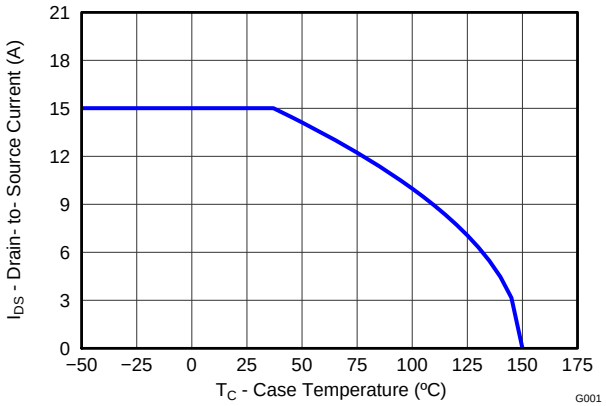
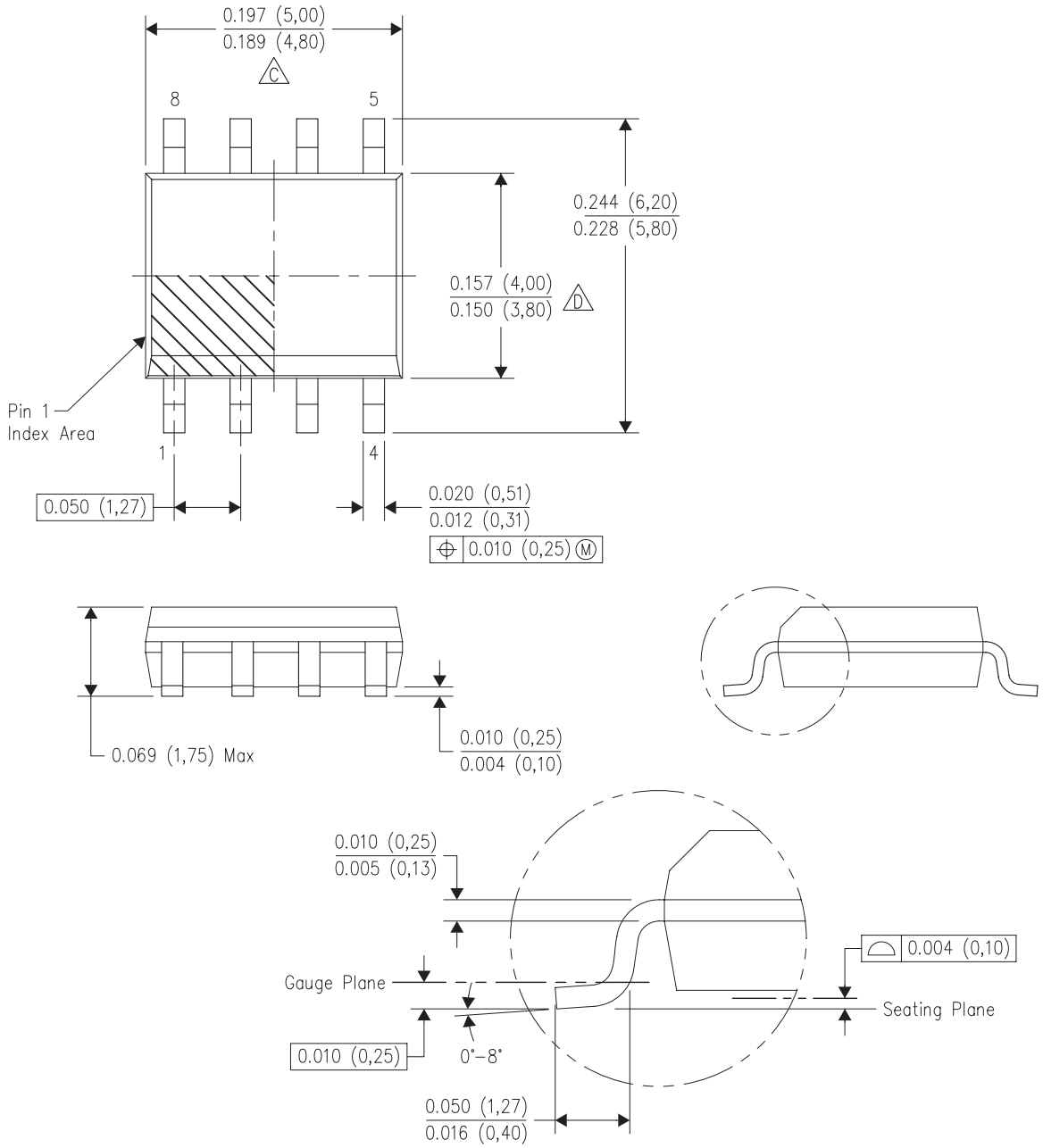


Figure 12. Maximum Drain Current vs Temperature

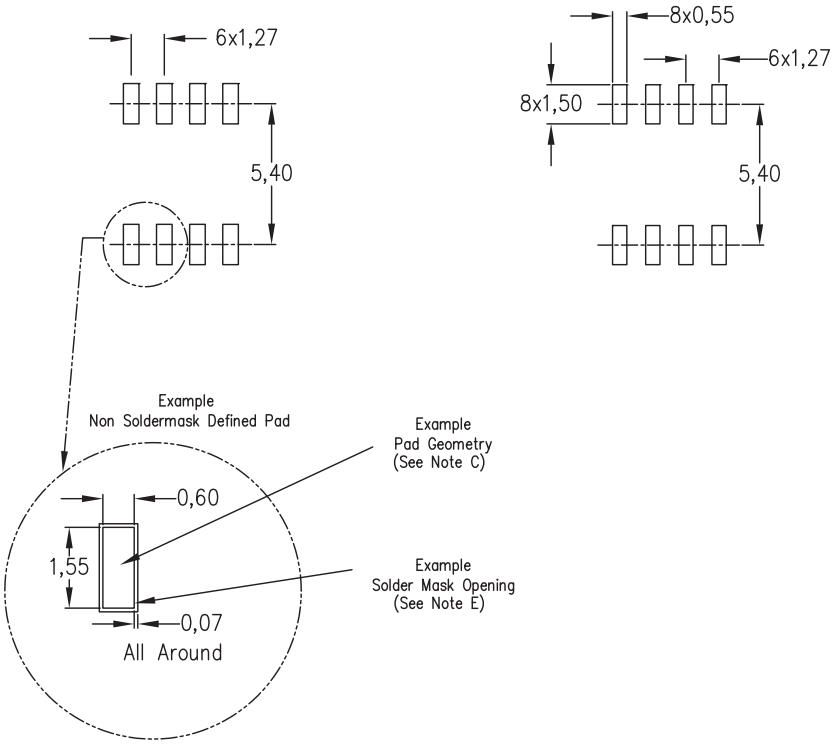
MECHANICAL DATA

SO-8 Package Dimensions



1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
4. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
5. Reference JEDEC MS-012 variation AA.

Recommended PCB Pattern and Stencil Opening



1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Publication IPC-7351 is recommended for alternate designs.
4. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
5. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88537ND	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM			Samples
CSD88537NDT	PREVIEW	SOIC	D	8	250	TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

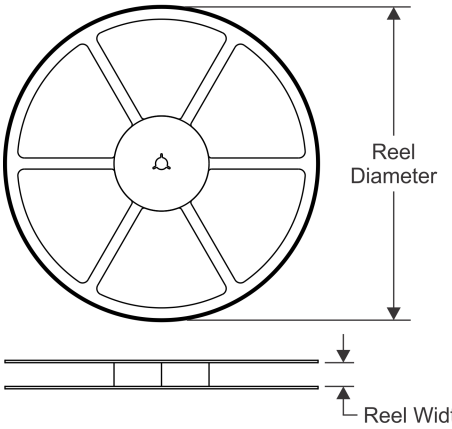
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

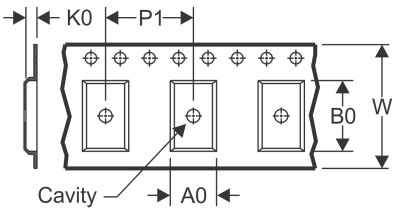
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

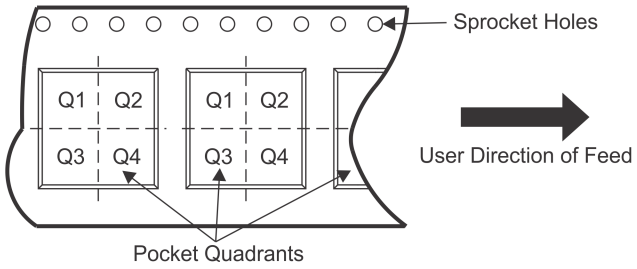


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

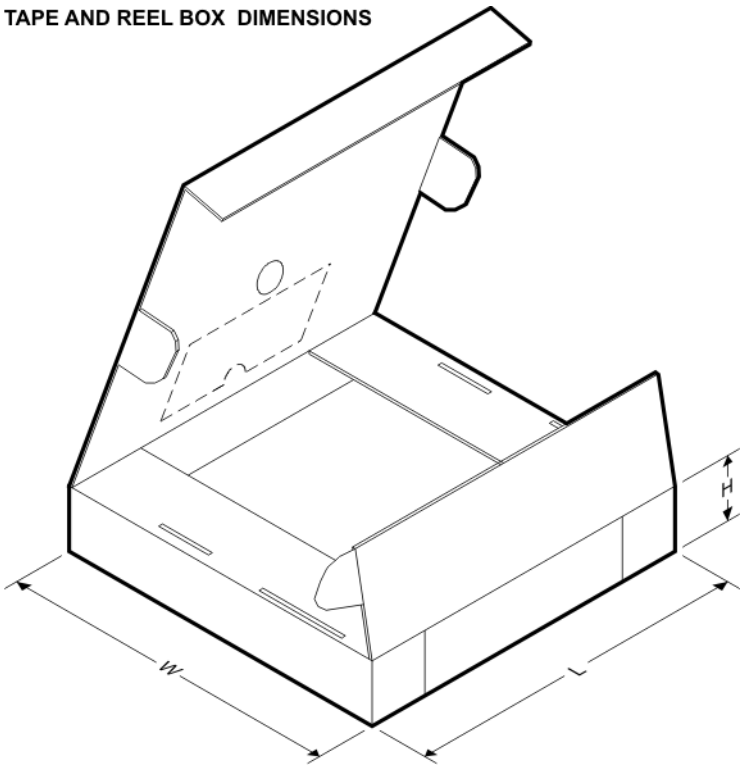
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD88537ND	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

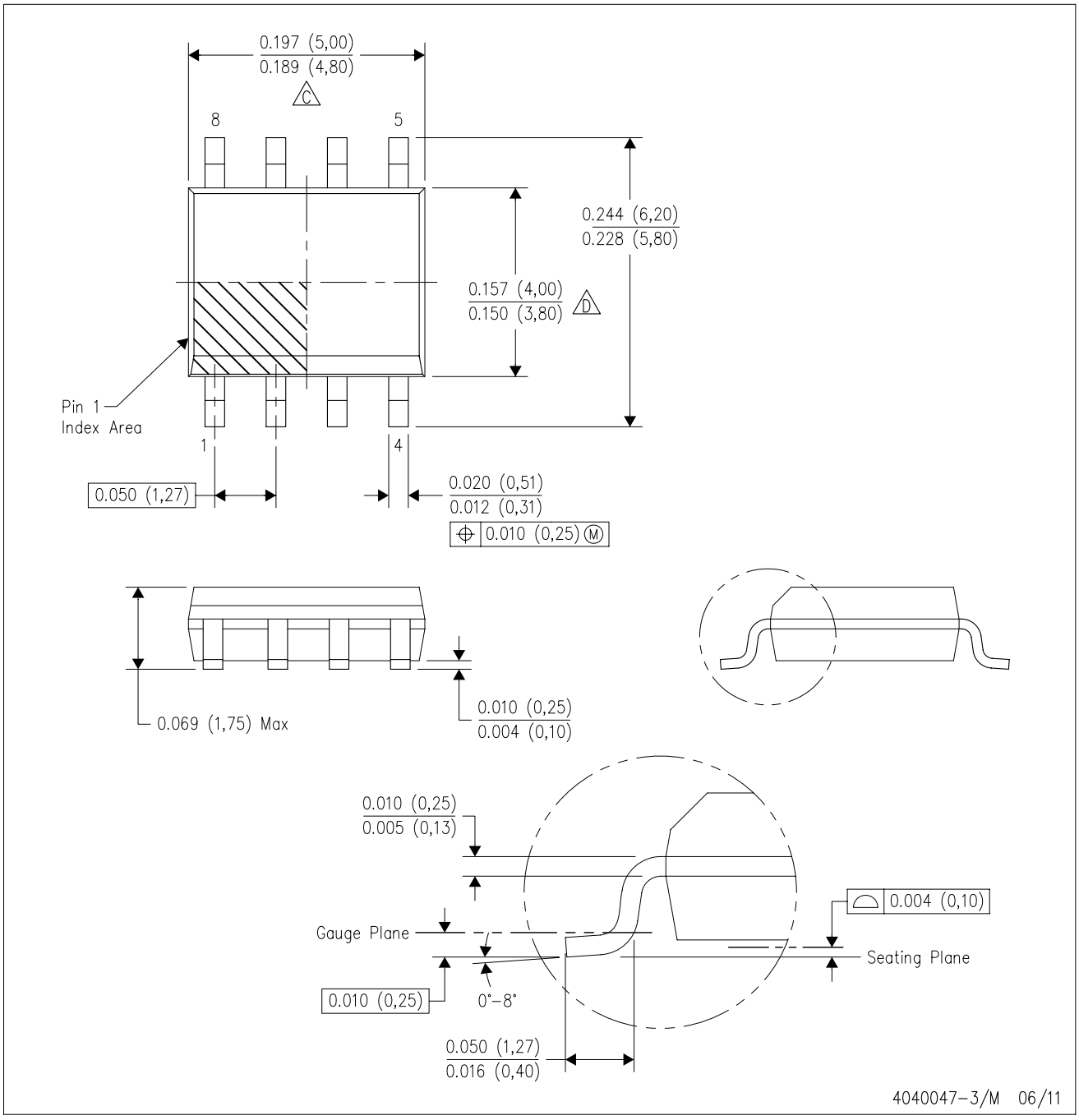
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD88537ND	SOIC	D	8	2500	336.6	336.6	41.3

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



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D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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