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# STK544UC62K-E

Thick-Film Hybrid IC

## Inverter Power H-IC for 3-phase Motor Drive

### Overview

This “Inverter Power H-IC” includes the output stage of a 3-phase inverter, pre-drive circuits, bootstrap circuits, and protection circuits in one package.

### Function

- SIP(single in-line package) of the transfer full mold structure.
- The emitter line of the each lower phase outputs to an external terminal with the option of control using 3-phase current detection with external resistors.
- Direct input of CMOS level control signals without an insulating circuit is possible.
- Protective circuits including over current and pre-drive low voltage protection are built in.
- A single power supply drive is enabled through the use of bootstrap circuits for upper IGBT gate drives.
- Built-in dead-time for shoot-thru protection.
- Internal substrate temperature is measured with an internal pulled up thermistor.

### Certification

- UL1557 (File Number: E339285).

### Specifications

**Absolute Maximum Ratings** at  $T_c = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VCC	V+ to VRU(VRV,VRW), surge<500V *1	450	V
Collector-emitter voltage	VCE	V+ to U(V,W) or U(V,W) to VRU(VRV,VRW)	600	V
Output current	Io	V+, VRU,VRV,VRW, U,V,W terminal current	±10	A
		V+, VRU,VRV,VRW, U,V,W terminal current at $T_c=100^\circ\text{C}$	±6	A
Output peak current	Iop	V+, VRU,VRV,VRW, U,V,W terminal current for a pulse width of 1ms	±20	A
Pre-driver voltage	VD1,2,3,4	VB1 to U, VB2 to V, VB3 to W, VDD to VSS *2	20	V
Input signal voltage	VIN	HIN1, 2, 3, LIN1, 2, 3 terminals	-0.3 to 7	V
ITRIP terminal voltage	VITRIP	ITRIP terminal	VSS+5	V
Maximum power dissipation	Pd	IGBT per 1 channel	22	W
Junction temperature	Tj	IGBT,FRD	150	°C
Storage temperature	Tstg		-40 to +125	°C
Operating case temperature	Tc	H-IC case temperature	-40 to +100	°C
Tightening torque		Case mounting screws *3	0.9	Nm
Withstand voltage	Vis	50Hz sine wave AC 1 minute *4	2000	VRMS

Reference voltage is “VSS” terminal voltage unless otherwise specified.

\*1: Surge voltage developed by the switching operation due to the wiring inductance between V+ and VRU(VRV,VRW) terminals.

\*2: VD1=VB1 to U, VD2=VB2 to V, VD3=VB3 to W, VD4=VDD to VSS terminal voltage.

\*3: Flatness of the heat-sink should be less than  $-50\mu\text{m}$  to  $+100\mu\text{m}$ .

\*4: Test conditions : AC2500V, 1 second.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

# STK544UC62K-E

## Electrical Characteristics at Tc = 25°C, VD1, VD2, VD3, VD4 = 15V

Electrical Characteristics at $T_C = 25^{\circ}\text{C}$ , $V_{D1}$ , $V_{D2}$ , $V_{D3}$ , $V_{D4} = 15\text{V}$							
Parameter	Symbol	Conditions	Test circuit	Ratings			Unit
				min	typ	max	
Power output section							
Collector-emitter cut-off current	ICE	VCE=600V	Fig.1	-	-	0.1	mA
Bootstrap diode reverse current	IR(BD)	VR(BD)=600V		-	-	0.1	mA
Collector to emitter saturation voltage	VCE(SAT)	Io=10A, Tj=25°C	Fig.2	-	1.4	2.3	V
		Io=5A, Tj=100°C		-	1.3	-	
Diode forward voltage	VF	Io=10A, Tj=25°C	Fig.3	-	1.3	2.2	V
		Io=5A, Tj=100°C		-	1.2	-	
Junction to case thermal resistance	$\theta_{j-c}(T)$	IGBT	-	-	4.5	5.5	°C/W
	$\theta_{j-c}(D)$	FRD		-	5.5	6.5	
Thermal resistance case to sink	Rth(c-s)	1W/mK thermal conductivity *1		-	-	0.1	
Protection section							
FAULT clearance delay time	FLTCLR	Form time fault condition clears	-	6	9	12	ms
Switching time	t ON	Io=10A	Fig.5	-	0.48	-	μs
	t OFF	Inductive load		-	0.54	-	

Reference voltage is "VSS" terminal voltage unless otherwise specified.

\*1: At 100μm thickness of the thermal grease.

## Electrical Characteristics Driver Function at Tc = 25°C

Parameter	Symbol	Test circuit	Ratings			Unit
			min	typ	max	
Supply section						
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage protection reset	V <sub>DDUV+</sub>	-	10.5	11.1	11.7	V
	V <sub>BSUV+</sub>					
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage protection set	V <sub>DDUV-</sub>	-	10.3	10.9	11.5	V
	V <sub>BSUV-</sub>					
V <sub>DD</sub> and V <sub>BS</sub> supply undervoltage hysteresis	V <sub>DDUVH</sub>	-	0.14	0.2	-	V
	V <sub>BSUVH</sub>					
Quiescent V <sub>DD</sub> supply current	I <sub>QDD</sub>	Fig.4	-	2.0	4.0	mA
Quiescent V <sub>BS</sub> supply current	I <sub>QBS</sub>		-	0.08	0.4	mA
Input section						
Logic low input voltage	V <sub>INL</sub>	-	-	-	0.8	V
Logic high input voltage	V <sub>INH</sub>	-	2.5		-	V
Logic 0 input leakage current	I <sub>IN+</sub>	-	76	118	160	μA
Logic 1 input leakage current	I <sub>IN-</sub>	-	97	150	203	μA
ITRIP threshold voltage(OUT=LO or OUT=HI)	V <sub>ITRIP</sub>	-	3.67	4.17	4.67	V
Dynamic section						
Dead time(Internal dead time injected by driver)	DT	-	220	300	380	ns
ITRIP to shutdown propagation delay	t <sub>ITRIP</sub>	-	1.0	1.2	1.4	μs
ITRIP blanking time	t <sub>ITRPBL</sub>	-	-	0.9	-	μs

Reference voltage is "VSS" terminal voltage unless otherwise specified.

## STK544UC62K-E

### Switching Characteristics at $T_c = 25^\circ\text{C}$ , VD1, VD2, VD3, VD4 = 15V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Turn-on switching loss	Eon	$I_C=5\text{A}$ , $V_+=400\text{V}$ , $V_{DD}=15\text{V}$ , $L=3.9\text{mH}$ , $T_c=25^\circ\text{C}$	-	195	-	$\mu\text{J}$
Turn-off switching loss	Eoff		-	122	-	$\mu\text{J}$
Total switching loss	Etot		-	317	-	$\mu\text{J}$
Turn-on switching loss	Eon	$I_C=5\text{A}$ , $V_+=400\text{V}$ , $V_{DD}=15\text{V}$ , $L=3.9\text{mH}$ , $T_c=100^\circ\text{C}$	-	224	-	$\mu\text{J}$
Turn-off switching loss	Eoff		-	186	-	$\mu\text{J}$
Total switching loss	Etot		-	410	-	$\mu\text{J}$
Diode reverse recovery time	trr	$I_F=5\text{A}$ , $V_+=400\text{V}$ , $V_{DD}=15\text{V}$ , $L=3.9\text{mH}$ , $T_c=100^\circ\text{C}$	-	70	-	ns
Reverse bias safe operating area	RBSOA	$I_o=20\text{A}$ , $V_{CE}=450\text{V}$	FULL SQUARE			-
Short circuit safe operating area	SCSOA	$V_{CE}=400\text{V}$	4	-	-	$\mu\text{s}$

$V_{DD}=V_{B1}=V_{B2}=V_{B3}=15\text{V}$ ,  $V_{SS}=V_{S1}=V_{S2}=V_{S3}=0\text{V}$ , outputs loaded with 1nF, all voltage are referenced to VSS; unless otherwise noted.

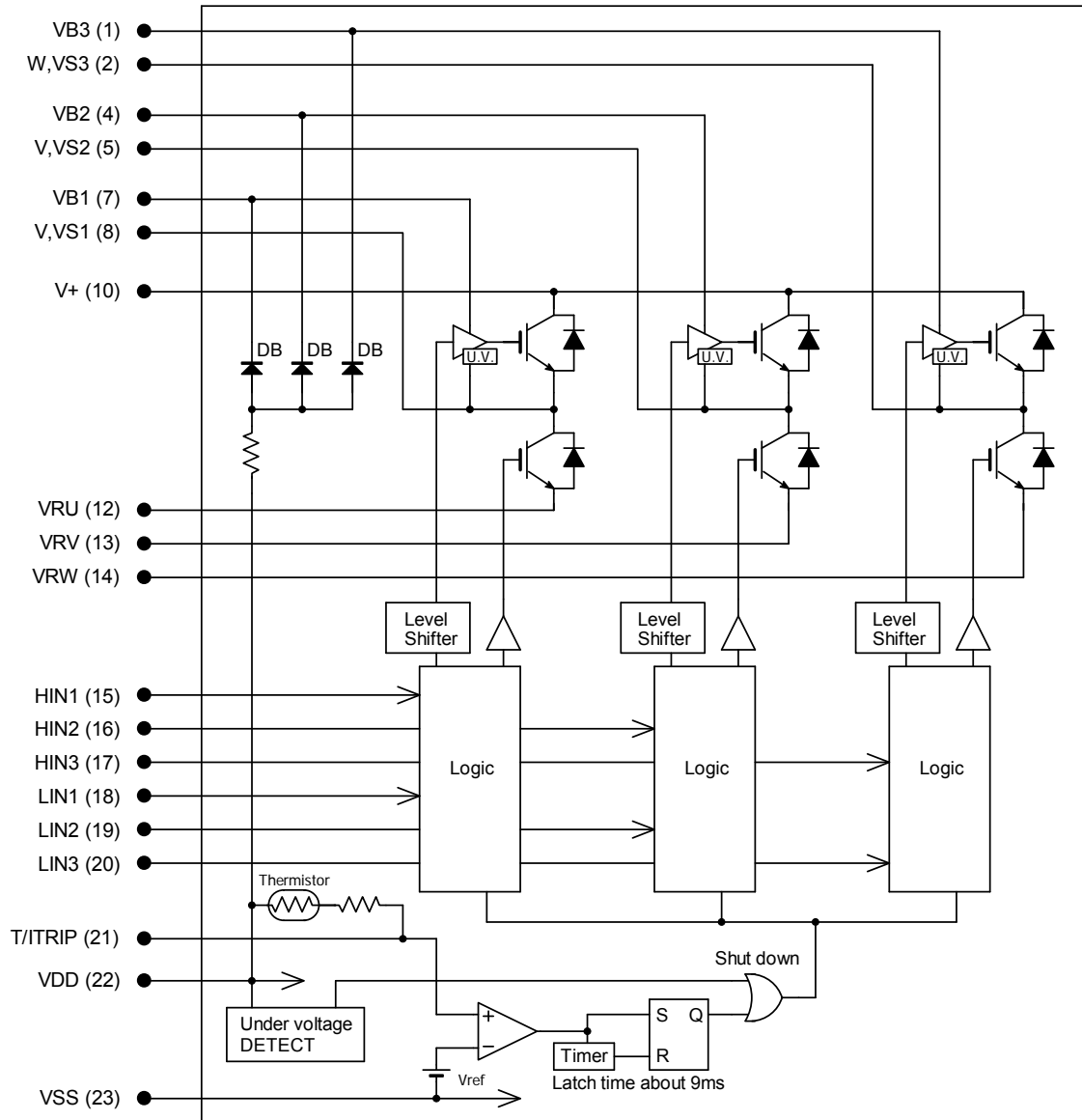
### Internal NTC-Thermistor Characteristics

Parameter		Conditions	Typ.	Unit
R25	Resistance	$T_c=25^\circ\text{C}$	$100\pm3\%$	k $\Omega$
R125	Resistance	$T_c=125^\circ\text{C}$	$2.522\pm3\%$	k $\Omega$
B	B-Constant(25-50 $^\circ\text{C}$ )	$R_2=R_1e^{[B(1/T_2-1/T_1)]}$	$4250\pm1\%$	K
Temperature range		-	-40 to +125	$^\circ\text{C}$
Typ. Dissipation constant		$T_c=25^\circ\text{C}$	1	mW/ $^\circ\text{C}$

#### Notes:

- The pre-drive power supply low voltage protection has approximately 200mV of hysteresis and operates as follows.  
Upper side : The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'high'.  
Lower side : The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.
- When assembling the H-IC on the heat sink the tightening torque range is 0.6Nm to 0.9Nm.
- The pre-drive low voltage protection protects the device when the pre-drive supply voltage falls due to an operating malfunction.

## Equivalent Block Diagram



## Module Pin-Out Description

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W, VS3	Output 3, High Side Floating Supply Offset Voltage 3
3	-	Without pin
4	VB2	High Side Floating Supply Voltage 2
5	V, VS2	Output 2, High Side Floating Supply Offset Voltage 2
6	-	Without pin
7	VB1	High Side Floating Supply Voltage 1
8	U, VS1	Output 1, High Side Floating Supply Offset Voltage 1
9	-	Without pin
10	V+	Positive Bus Input Voltage
11	-	Without pin
-	-	-

Pin	Name	Description
12	VRU	Low Side Emitter Connection – Phase 1
13	VRV	Low Side Emitter Connection – Phase 2
14	VRW	Low Side Emitter Connection – Phase 3
15	HIN1	Logic Input High Side Gate Driver – Phase 1
16	HIN2	Logic Input High Side Gate Driver – Phase 2
17	HIN3	Logic Input High Side Gate Driver – Phase 3
18	LIN1	Logic Input Low Side Gate Driver – Phase 1
19	LIN2	Logic Input Low Side Gate Driver – Phase 2
20	LIN3	Logic Input Low Side Gate Driver – Phase 3
21	T/Itrip	Temperature Monitor and Shut-down Pin
22	VDD	+15V Main Supply
23	VSS	Negative Main Supply

Test Circuit

The tested phase U+ shows the upper side of the U phase and U- shows the lower side of the U phase.

ICE / IR(BD)

	U+	V+	W+	U-	V-	W-
M	10	10	10	8	5	2
N	8	5	2	12	13	14

	U(BD)	V(BD)	W(BD)
M	7	4	1
N	23	23	23

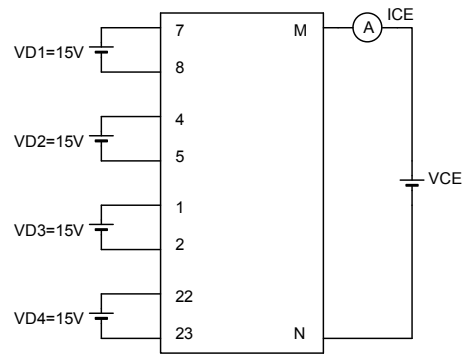


Fig. 1

VCE(SAT) (test by pulse)

	U+	V+	W+	U-	V-	W-
M	10	10	10	8	5	2
N	8	5	2	12	13	14
m	15	16	17	18	19	20

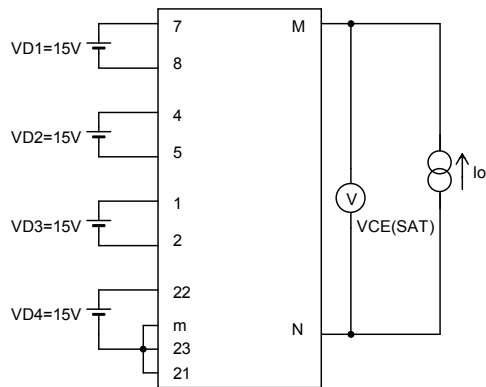


Fig. 2

VF (test by pulse)

	U+	V+	W+	U-	V-	W-
M	10	10	10	8	5	2
N	8	5	2	12	13	14

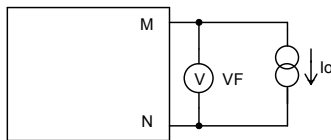


Fig. 3

ID

	VD1	VD2	VD3	VD4
M	7	4	1	22
N	8	5	2	23

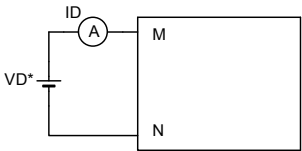


Fig. 4

■Switching time (The circuit is a representative example of the lower side U phase.)

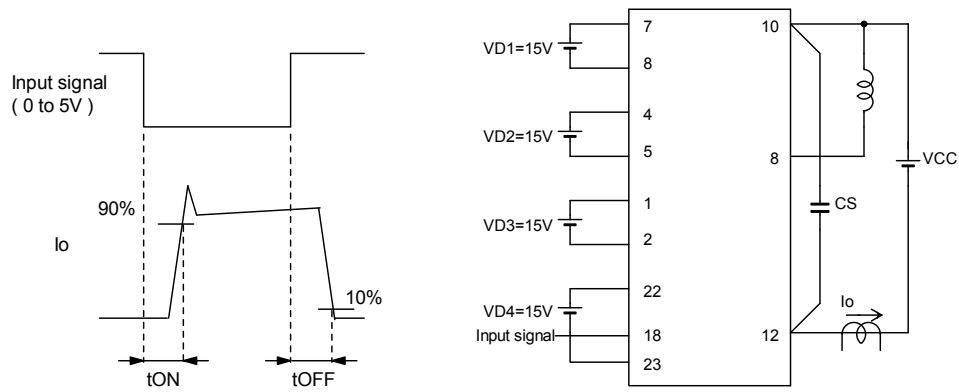


Fig. 5

■RB-SOA (The circuit is a representative example of the lower side U phase.)

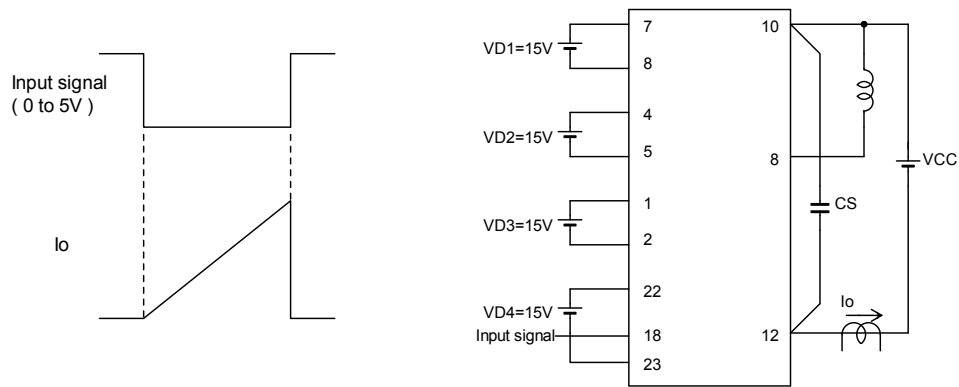


Fig. 6

# Input / Output Timing Diagram

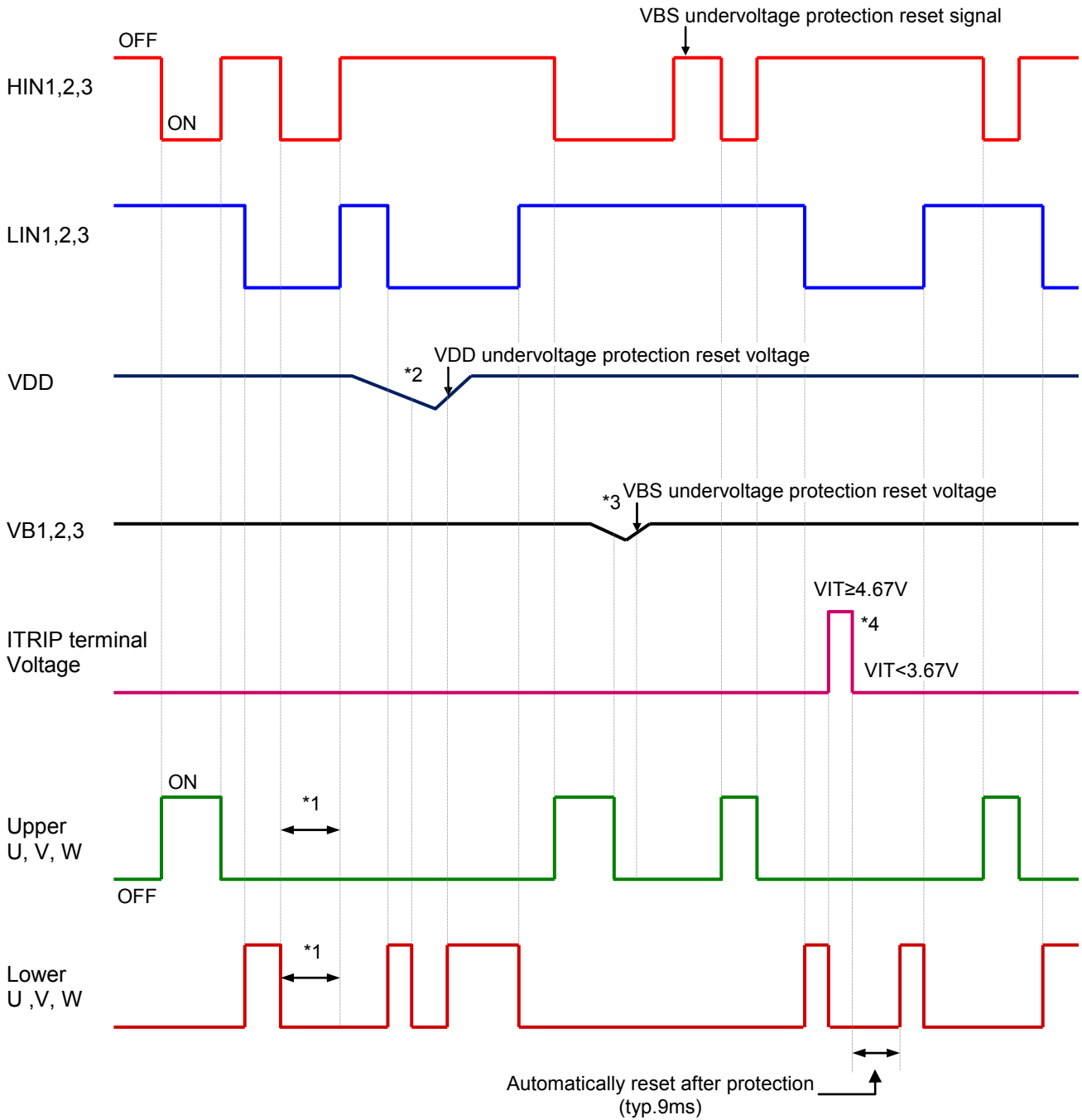
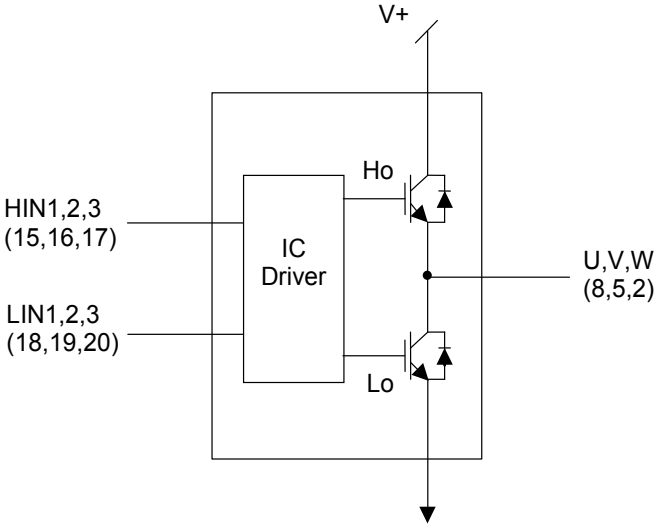


Fig. 7

## Notes:

- \*1 shows the prevention of shoot-thru via control logic, however, more dead time must be added to account for switching delay externally.
- \*2 when VDD decreases all gate output signals will go low and cut off all 6 IGBT outputs. When VDD rises the operation will resume immediately.
- \*3 when the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
- \*4 when VITRIP exceeds threshold all IGBT's are turned off and normal operation resumes 9ms (typ) after over current condition is removed.

Logic level table

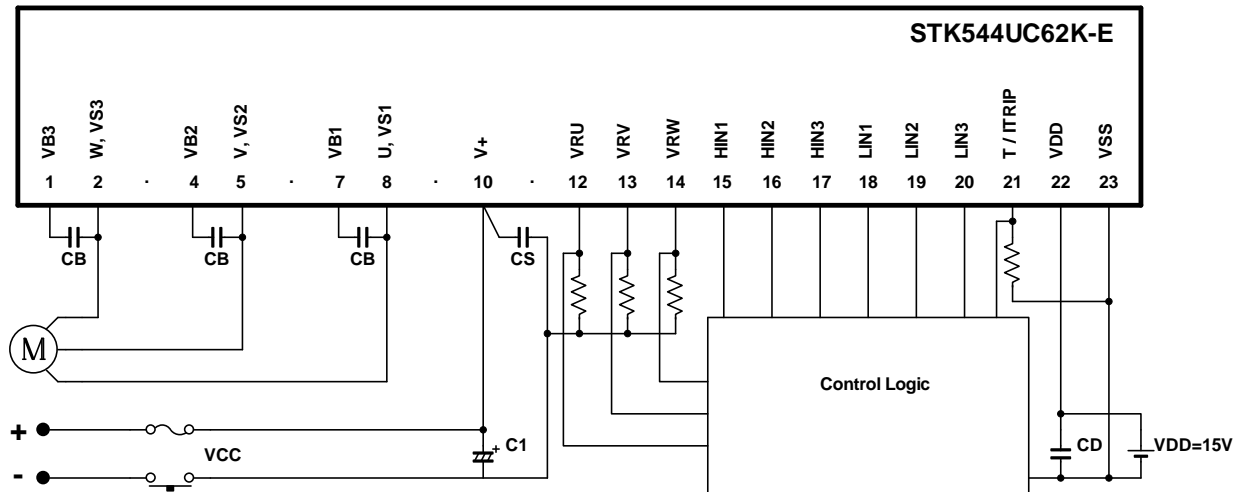


Itrip	HIN1,2,3	LIN1,2,3	U,V,W
0	0	1	V+
0	1	0	0
0	1	1	X
1	X	X	X

Fig. 8



## Sample Application Circuit



## Recommended Operating Conditions at Tc = 25°C

Item	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	VCC	Between V+ to VRU(VRV,VRW)	0	280	450	V
Pre-driver supply voltage	VD1,2,3	Between VB1 to U,VB2 to V,VB3 to W	12.5	15	17.5	V
	VD4	Between VDD to VSS *1	13.5	15	16.5	
ON-state input voltage	VIN(ON)	HIN1,HIN2,HIN3,LIN1,LIN2,LIN3 terminal	0	-	0.3	V
OFF-state input voltage	VIN(OFF)		3.0	-	5.0	
PWM frequency	fPWM	-	1	-	20	kHz
Dead time	DT	Turn-off to turn-on (External)	0.5	-	-	μs
Mounting torque	-	'M3' type screw	0.6	-	0.9	Nm

\*1 Pre-drive power supply (VD4=15±1.5V) must have the capacity of Io=20mA(DC), 0.5A(Peak).

## Usage Precaution

1. This H-IC includes internal bootstrap diode and resistor. By adding a capacitor CB, a single high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47μF, however, this value needs to be verified prior to production. When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of CS is in the range of 0.1 to 10μF.
3. VRU, VRV, and VRW terminals are direct outputs of the emitter line of the each lower phase IGBT and can be used to monitor each phase's or collective current with external resistors. IF current is not monitored, each resistor should be short-circuited.
4. Disconnection of terminals U, V, or W during normal motor operation will cause damage to H-IC, use caution with this connection.
5. Zener diode with 10V is connected with the inside of the signal input terminal. When inputting voltage which exceeds 5V, connect resistor between the side of the power and the signal input terminal, for the input current of the signal input terminal become equal to or less than 0.5mA. This resistor is effective with the noise absorption of the signal terminal, too.
6. A fuse on VCC is recommended.
7. Inside the H-IC, a thermistor used as the temperature monitor is connected between VDD terminal and T/ITRIP terminal, therefore, an external pull down resistor connected between the T/ITRIP terminal and VSS terminal should be used. The temperature monitor example application is as follows, please refer the Fig.10, Fig.11, and Fig.12 below.
8. All data shown implements an example of the application circuit but does not guarantee a design for the mass production.

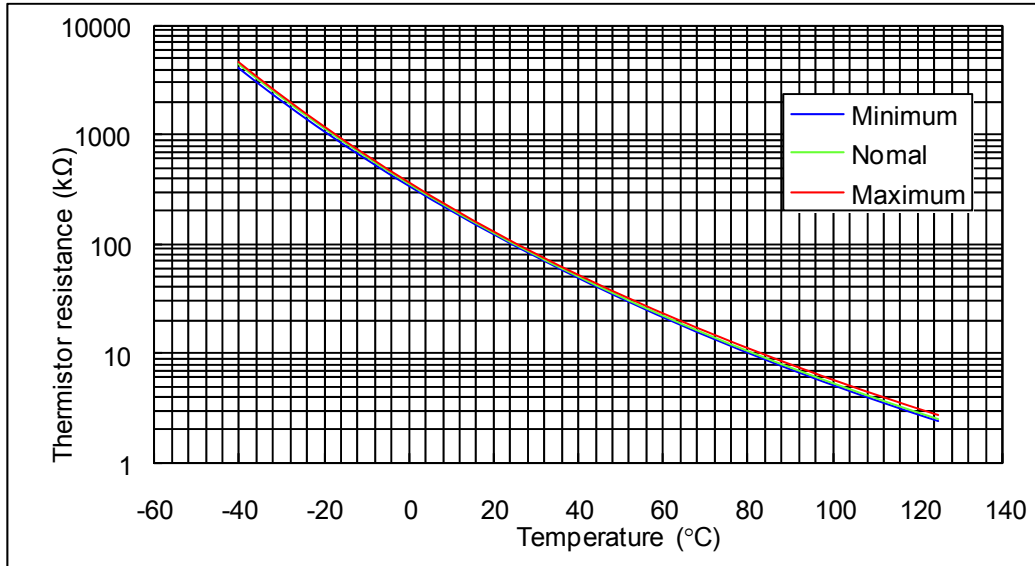


Fig. 10 Variation of thermistor resistance with temperature

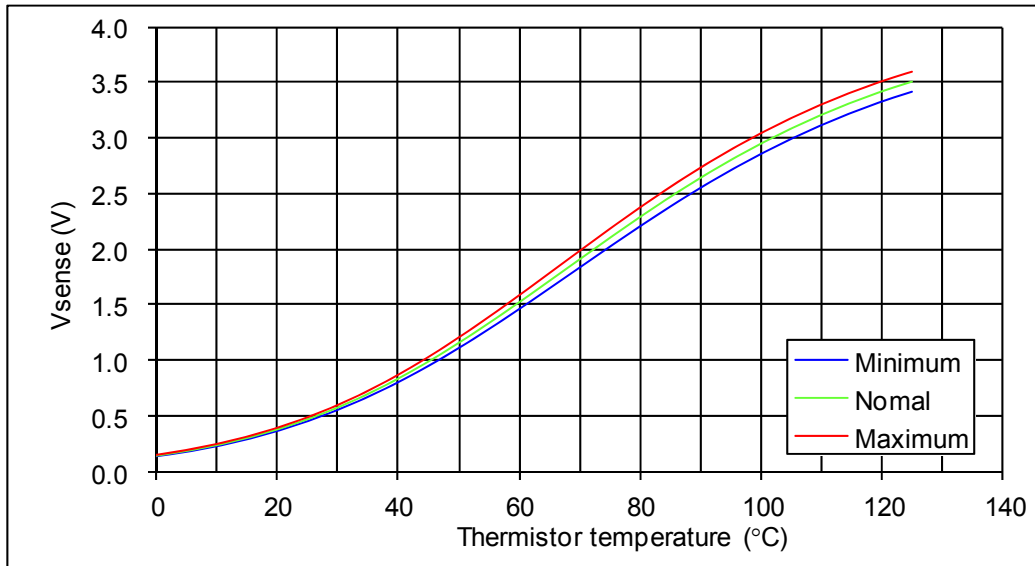


Fig. 11 Variation of temperature sense voltage with thermistor temperature by using external bias resistance of  $4.3\text{k}\Omega \pm 1\%$  and  $V_{DD}=15\text{V}$

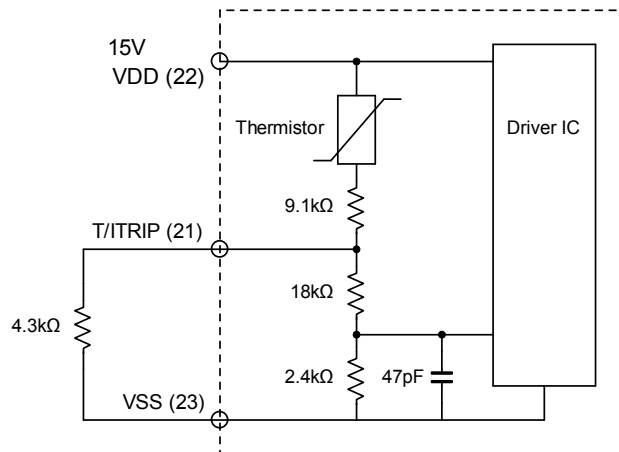


Fig. 12 Sample application circuit for temperature monitoring

## The characteristic of PWM switching frequency

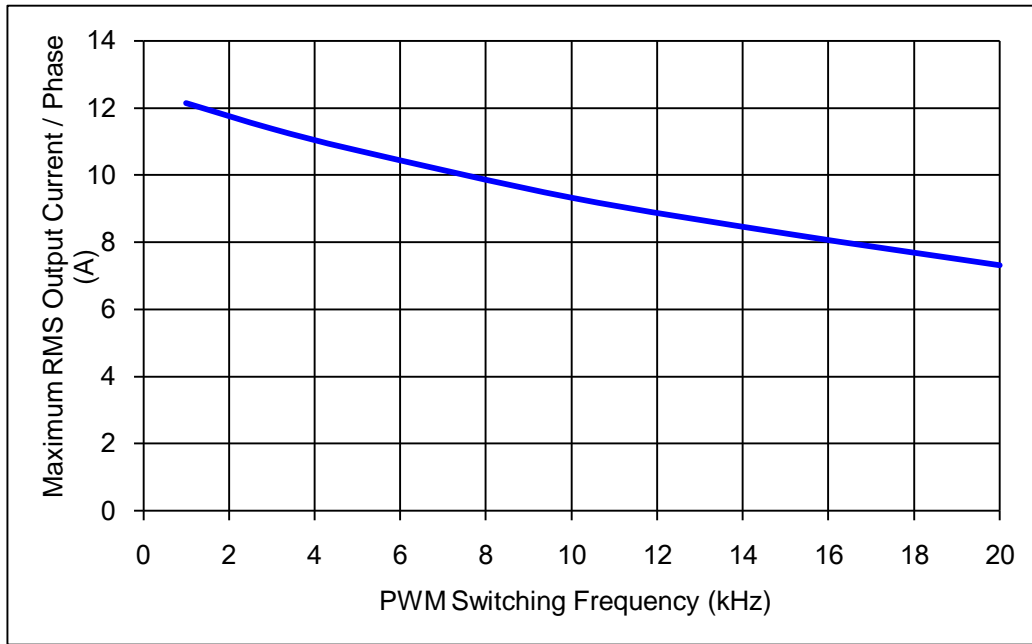


Fig. 13 Maximum sinusoidal phase current as function of switching frequency  
at  $T_c=100^{\circ}\text{C}$ ,  $V_{CC}=400\text{V}$

## Switching waveform

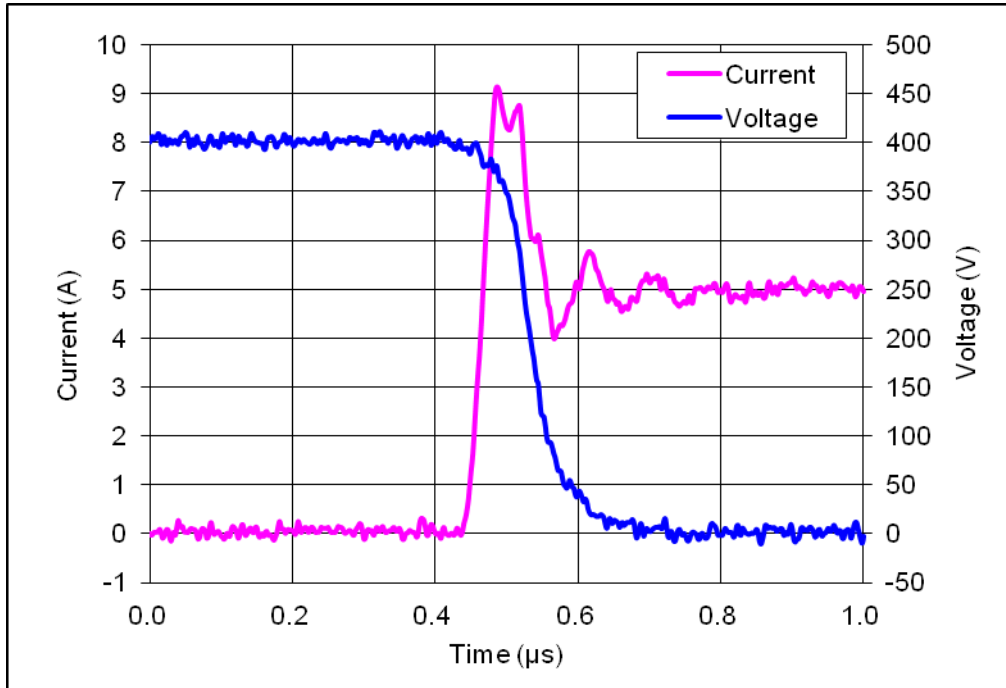


Fig. 14 IGBT Turn-on. Typical turn-on waveform at  $T_c=100^{\circ}\text{C}$ ,  $V_{CC}=400\text{V}$

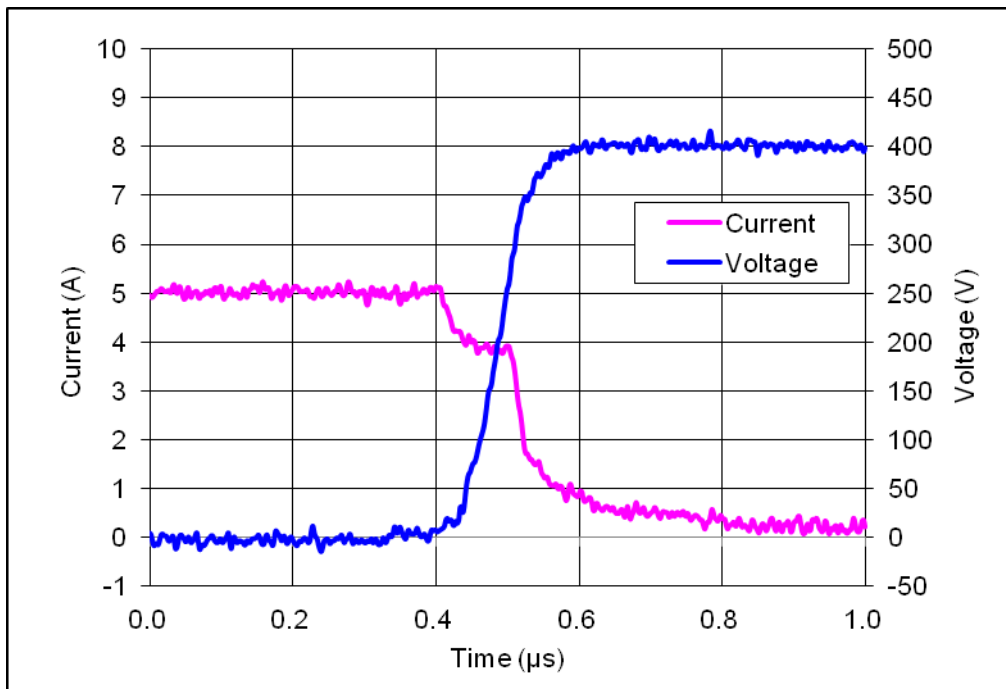


Fig. 15 IGBT Turn-off. Typical turn-off waveform at  $T_c=100^{\circ}\text{C}$ ,  $V_{CC}=400\text{V}$

## CB capacitor value calculation for bootstrap circuit

### Calculate conditions

Parameter	Symbol	Value	Unit
Upper side power supply.	VBS	15	V
Total gate charge of output power IGBT at 15V.	QG	89	nC
Upper limit power supply low voltage protection.	UVLO	12	V
Upper side power dissipation.	IDMAX	95	μA
ON time required for CB voltage to fall from 15V to UVLO	TONMAX	-	S

### Capacitance calculation formula

Thus, the following formula are true

$$VBS \times CB - QG - IDMAX \times TONMAX = UVLO \times CB$$

therefore,

$$CB = (QG + IDMAX \times TONMAX) / (VBS - UVLO)$$

The relationship between TONMAX and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47μF, however, this value needs to be verified prior to production.

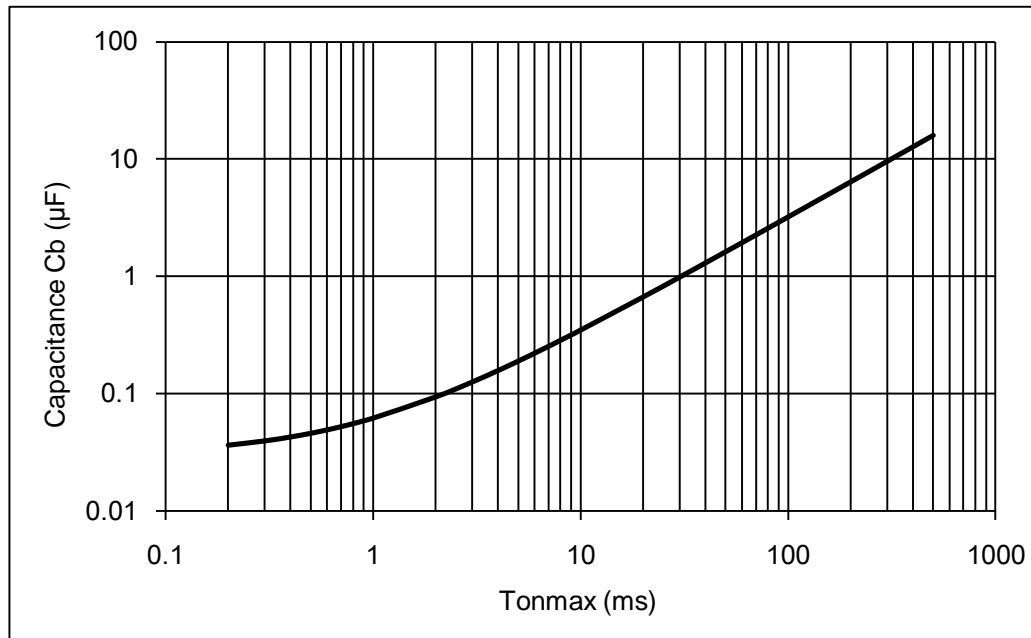


Fig. 16 TONMAX vs CB characteristic

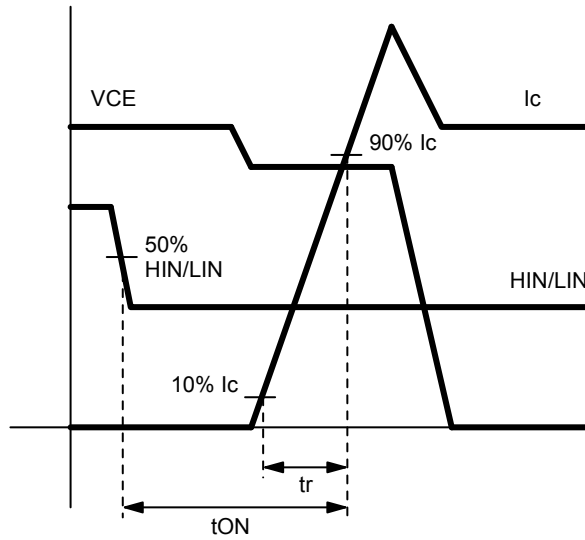


Fig. 17a Input to output propagation turn-on delay time

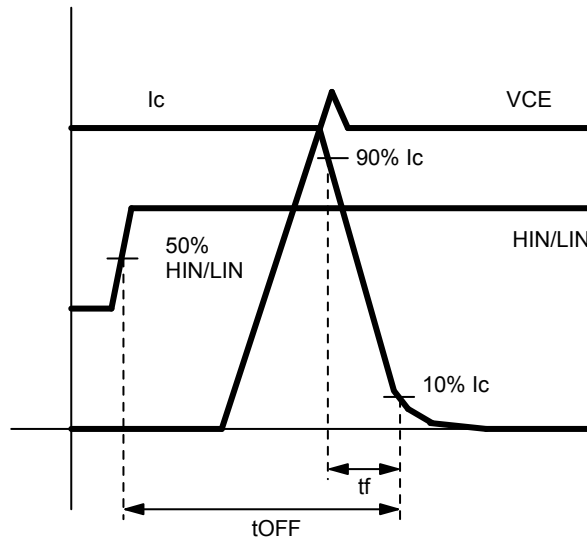


Fig. 17b Input to output propagation turn-off delay time

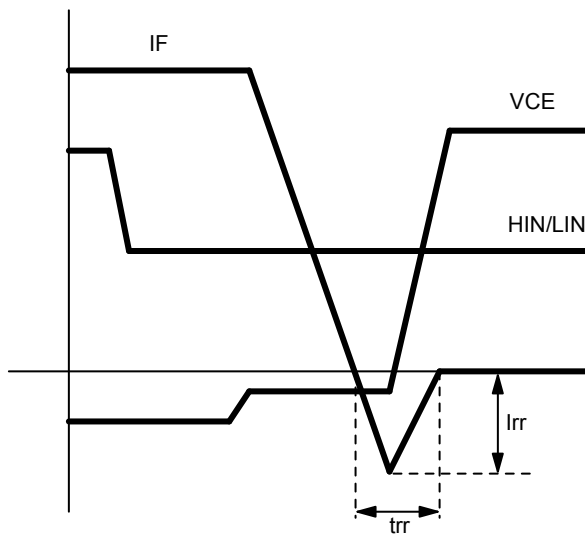
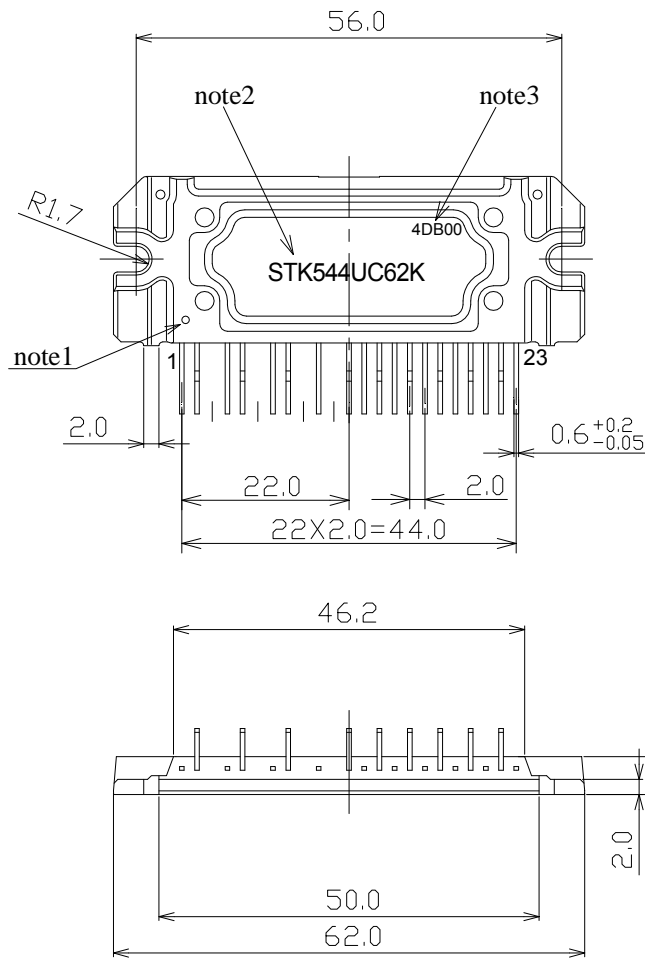


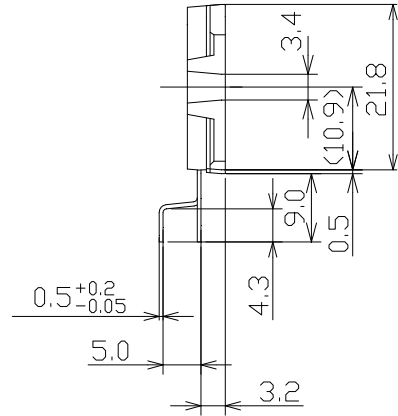
Fig. 17c Diode reverse recovery

# Package Dimensions

(unit : mm)



missing pin ; 3,6,9,11



note1: Mark for No.1 pin identification.

note2: The form of a character in this drawing differs from that of HIC.

note3: This indicates the lot code.  
The form of a character in this drawing differs from that of HIC.

## ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK544UC62K-E	SIP23 (Pb-Free)	8 / Fan-Fold

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