

PEMD2; PIMD2; PUMD2

NPN/PNP resistor-equipped transistors;
R1 = 22 k Ω , R2 = 22 k Ω

Rev. 8 — 14 November 2013

Product data sheet

1. Product profile

1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

| Type number | Package | | PNP/PNP complement | NPN/NPN complement | Package configuration |
|-------------|---------|-------|--------------------|--------------------|---------------------------|
| | NXP | JEITA | | | |
| PEMD2 | SOT666 | - | PEMB1 | PEMH1 | ultra small and flat lead |
| PIMD2 | SOT457 | SC-74 | - | - | small |
| PUMD2 | SOT363 | SC-88 | PUMB1 | PUMH1 | very small |

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

Table 2. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|------------|------|-----|------|------------|
| Per transistor; for the PNP transistor with negative polarity | | | | | | |
| V _{CEO} | collector-emitter voltage | open base | - | - | 50 | V |
| I _O | output current | | - | - | 100 | mA |
| R1 | bias resistor 1 (input) | | 15.4 | 22 | 28.6 | k Ω |
| R2/R1 | bias resistor ratio | | 0.8 | 1 | 1.2 | |



2. Pinning information

Table 3. Pinning

| Pin | Description | Simplified outline | Graphic symbol |
|---------------------------------------|------------------------|--------------------|------------------|
| PEMD2 (SOT666); PUMD2 (SOT363) | | | |
| 1 | GND (emitter) TR1 | <p>001aab555</p> | <p>006aaa143</p> |
| 2 | input (base) TR1 | | |
| 3 | output (collector) TR2 | | |
| 4 | GND (emitter) TR2 | | |
| 5 | input (base) TR2 | | |
| 6 | output (collector) TR1 | | |
| PIMD2 (SOT457) | | | |
| 1 | GND (emitter) TR2 | | <p>006aab23ε</p> |
| 2 | input (base) TR2 | | |
| 3 | output (collector) TR1 | | |
| 4 | GND (emitter) TR1 | | |
| 5 | input (base) TR1 | | |
| 6 | output (collector) TR2 | | |

3. Ordering information

Table 4. Ordering information

| Type number | Package | | Version |
|-------------|---------|--|---------|
| | Name | Description | |
| PEMD2 | - | plastic surface-mounted package; 6 leads | SOT666 |
| PIMD2 | SC-74 | plastic surface-mounted package (TSOP6); 6 leads | SOT457 |
| PUMD2 | SC-88 | plastic surface-mounted package; 6 leads | SOT363 |

4. Marking

Table 5. Marking codes

| Type number | Marking code ^[1] |
|-------------|-----------------------------|
| PEMD2 | D4 |
| PIMD2 | M5 |
| PUMD2 | D*2 |

[1] * = placeholder for manufacturing site code

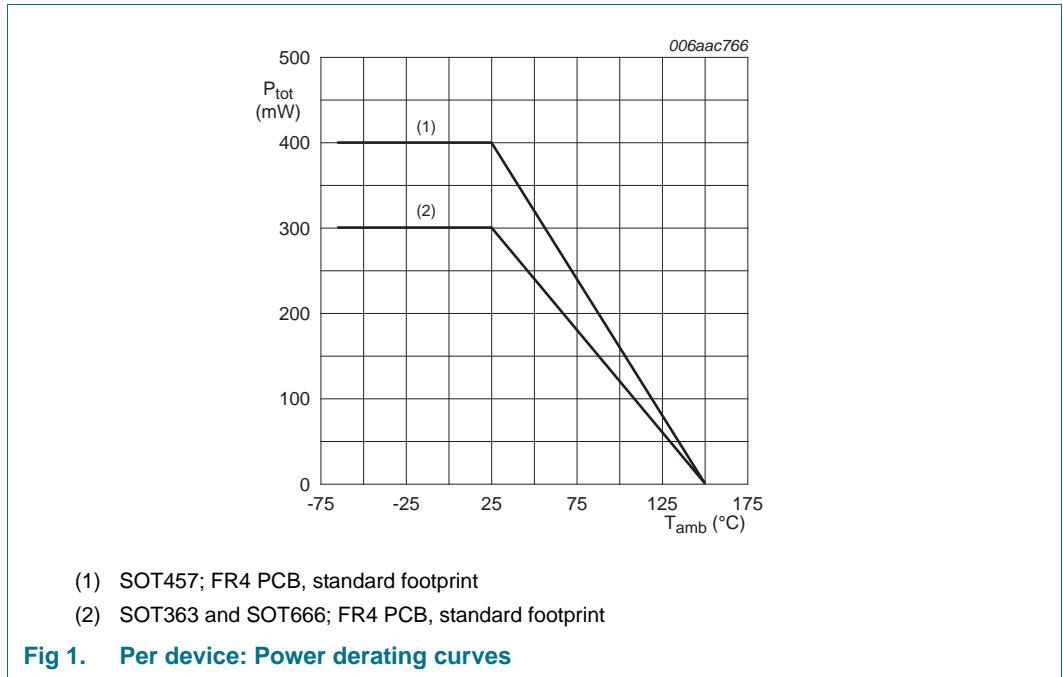
5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|--|---------------------------|--|--------------------------|------|------|----|
| Per transistor; for the PNP transistor with negative polarity | | | | | | |
| V _{CBO} | collector-base voltage | open emitter | - | 50 | V | |
| V _{CEO} | collector-emitter voltage | open base | - | 50 | V | |
| V _{EBO} | emitter-base voltage | open collector | - | 10 | V | |
| V _I | input voltage TR1 | | | | | |
| | | positive | - | +40 | V | |
| | | negative | - | -10 | V | |
| | input voltage TR2 | | | | | |
| | | positive | | +10 | | |
| | negative | | -40 | | | |
| I _O | output current | | - | 100 | mA | |
| I _{CM} | peak collector current | single pulse; t _p ≤ 1 ms | - | 100 | mA | |
| P _{tot} | total power dissipation | | T _{amb} ≤ 25 °C | | | |
| | | PEMD2 (SOT666) | [1] | - | 200 | mW |
| | | PIMD2 (SOT457) | [1] | | 250 | mW |
| | | PUMD2 (SOT363) | [1] | - | 200 | mW |
| Per device | | | | | | |
| P _{tot} | total power dissipation | | T _{amb} ≤ 25 °C | | | |
| | | PEMD2 (SOT666) | [1] | - | 300 | mW |
| | | PIMD2 (SOT457) | [1] | | 400 | mW |
| | | PUMD2 (SOT363) | [1] | - | 300 | mW |
| T _j | junction temperature | | - | 150 | °C | |
| T _{amb} | ambient temperature | | -55 | +150 | °C | |
| T _{stg} | storage temperature | | -65 | +150 | °C | |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

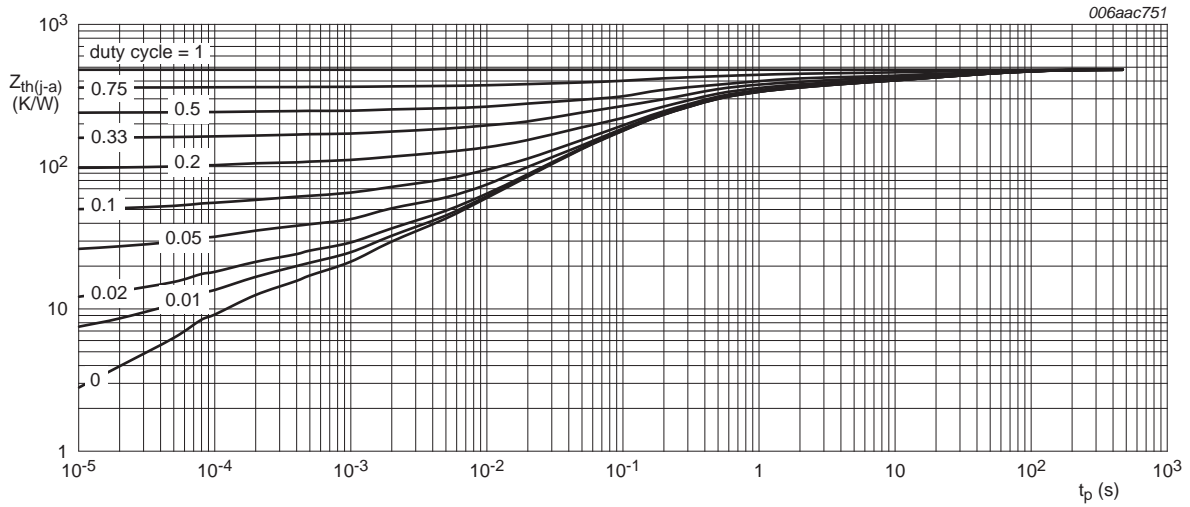


6. Thermal characteristics

Table 7. Thermal characteristics

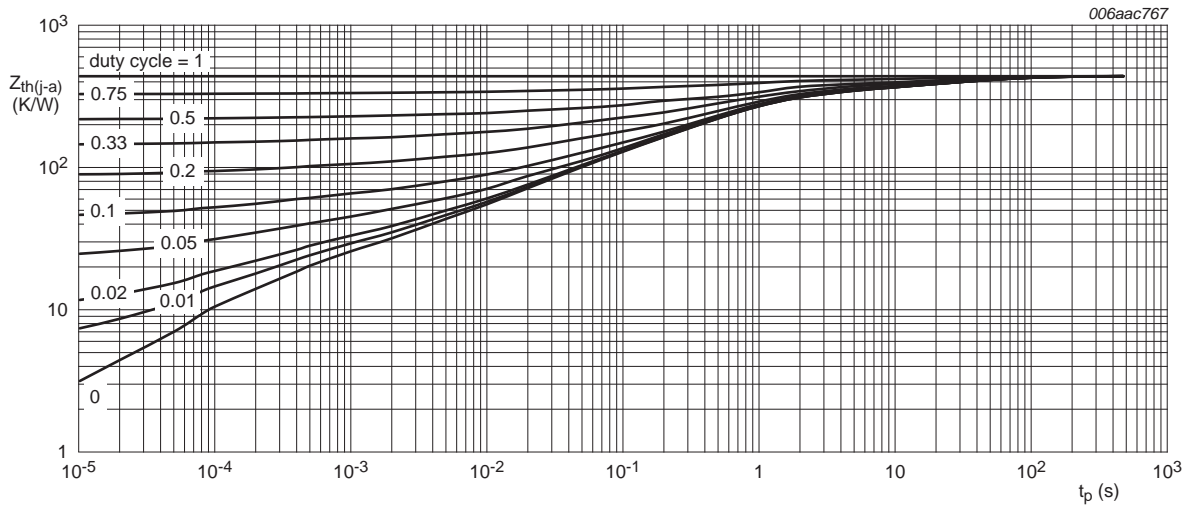
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---|-------------|-----|-----|-----|------|
| Per transistor | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | | | | |
| | PEMD2 (SOT666) | | [1] | - | 625 | K/W |
| | PIMD2 (SOT457) | | [1] | - | 500 | K/W |
| | PUMD2 (SOT363) | | [1] | - | 625 | K/W |
| Per device | | | | | | |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | | | | |
| | PEMD2 (SOT666) | | [1] | - | 417 | K/W |
| | PIMD2 (SOT457) | | [1] | - | 313 | K/W |
| | PUMD2 (SOT363) | | [1] | - | 417 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



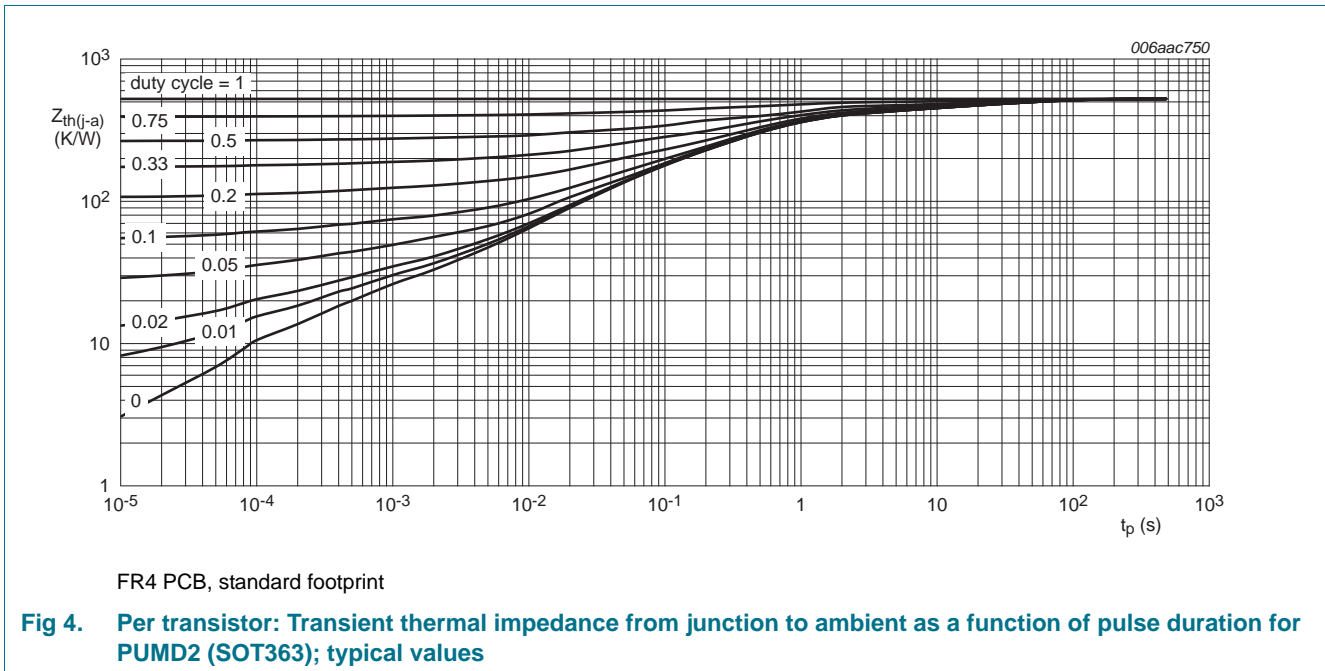
FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PEMD2 (SOT666); typical values



FR4 PCB, standard footprint

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PIMD2 (SOT457); typical values



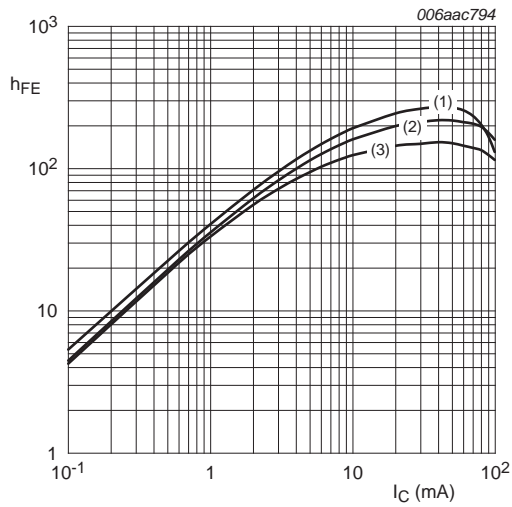
7. Characteristics

Table 8. Characteristics

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

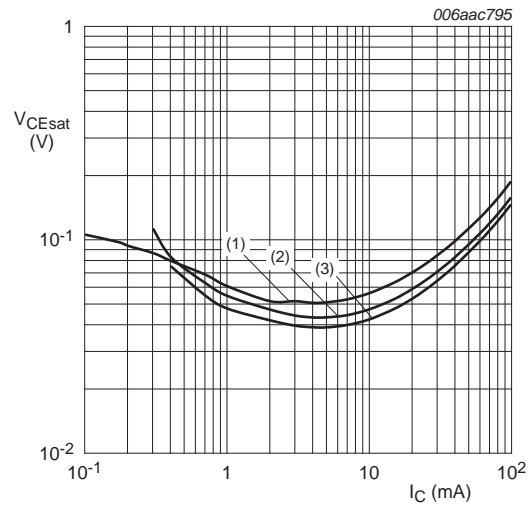
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--------------------------------------|--|------|-----|------|------|
| Per transistor; for the PNP transistor with negative polarity | | | | | | |
| I_{CBO} | collector-base cut-off current | $V_{CB} = 50\text{ V}; I_E = 0\text{ A}$ | - | - | 100 | nA |
| I_{CEO} | collector-emitter cut-off current | $V_{CE} = 30\text{ V}; I_B = 0\text{ A}$ | - | - | 100 | nA |
| | | $V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ °C}$ | - | - | 5 | μA |
| I_{EBO} | emitter-base cut-off current | $V_{EB} = 5\text{ V}; I_C = 0\text{ A}$ | - | - | 180 | μA |
| h_{FE} | DC current gain | $V_{CE} = 5\text{ V}; I_C = 5\text{ mA}$ | 60 | - | - | |
| V_{CEsat} | collector-emitter saturation voltage | $I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$ | - | - | 150 | mV |
| $V_{I(off)}$ | off-state input voltage | $V_{CE} = 5\text{ V}; I_C = 100\text{ μA}$ | - | 1.1 | 0.8 | V |
| $V_{I(on)}$ | on-state input voltage | $V_{CE} = 0.3\text{ V}; I_C = 5\text{ mA}$ | 2.5 | 1.7 | - | V |
| R1 | bias resistor 1 (input) | | 15.4 | 22 | 28.6 | kΩ |
| R2/R1 | bias resistor ratio | | 0.8 | 1 | 1.2 | |
| C_c | collector capacitance | $V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$ | | | | |
| | TR1 (NPN) | | - | - | 2.5 | pF |
| | TR2 (PNP) | | - | - | 3 | |
| f_T | transition frequency | $V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}$ | [1] | | | |
| | TR1 (NPN) | | - | 230 | - | MHz |
| | TR2 (PNP) | | - | 180 | - | MHz |

[1] Characteristics of built-in transistor



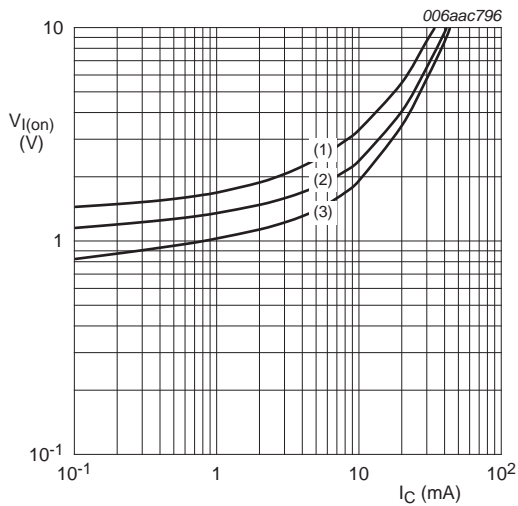
- $V_{CE} = 5 \text{ V}$
- (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 - (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 5. TR1 (NPN): DC current gain as a function of collector current; typical values



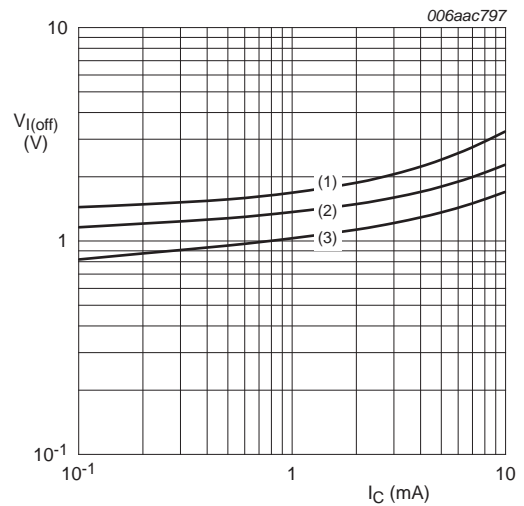
- $I_C/I_B = 20$
- (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 - (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 6. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



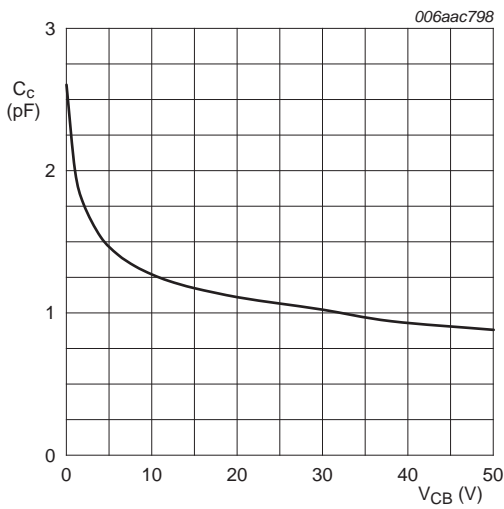
- $V_{CE} = 0.3 \text{ V}$
- (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 - (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 7. TR1 (NPN): On-state input voltage as a function of collector current; typical values



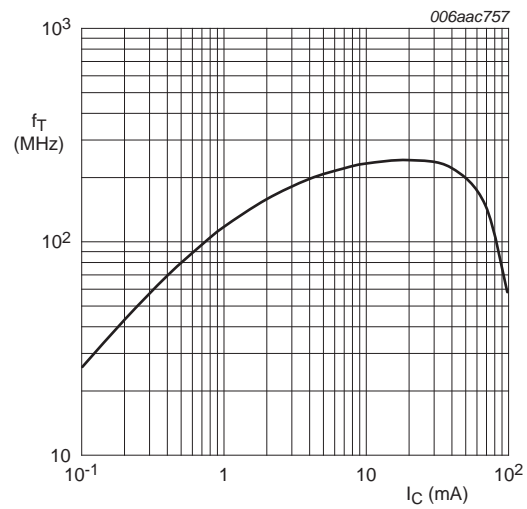
- $V_{CE} = 5 \text{ V}$
- (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 - (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 - (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 8. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



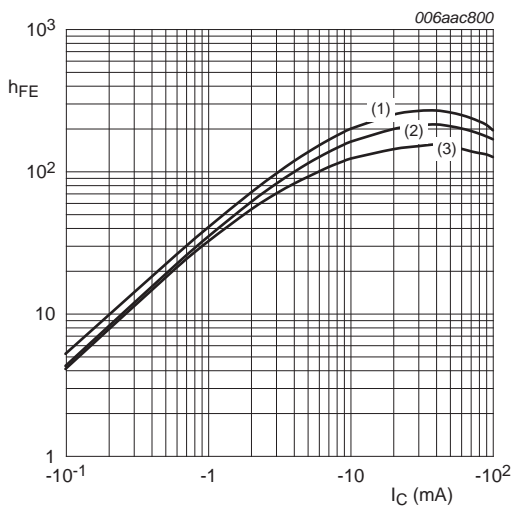
$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 9. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = 5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

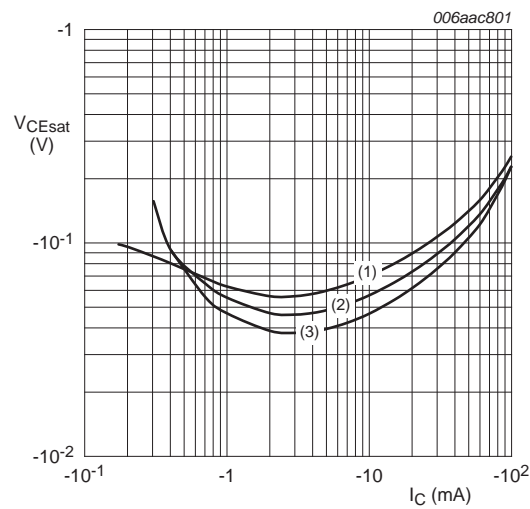
Fig 10. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



$V_{CE} = -5 \text{ V}$

- (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
- (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
- (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

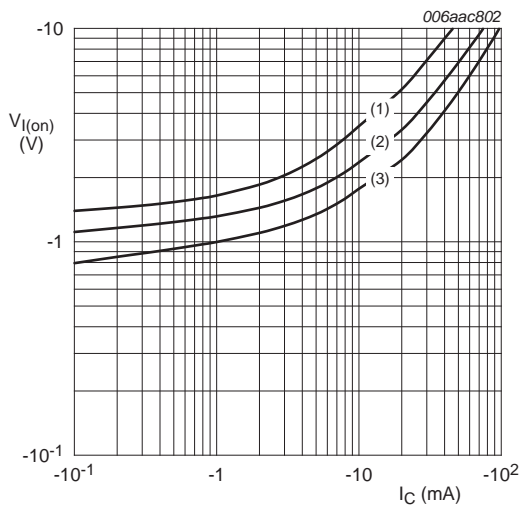
Fig 11. TR2 (PNP): DC current gain as a function of collector current; typical values



$I_C/I_B = 20$

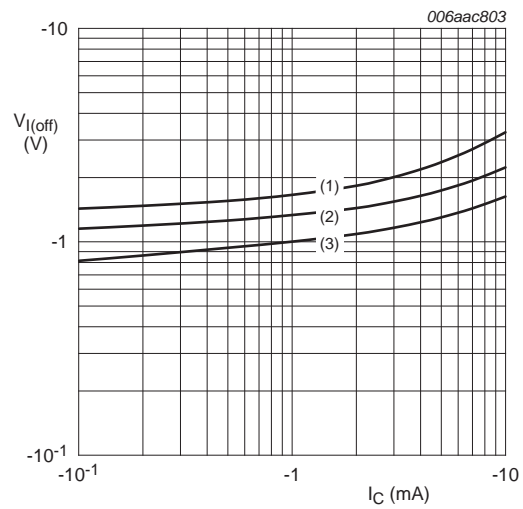
- (1) $T_{amb} = 100 \text{ }^\circ\text{C}$
- (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
- (3) $T_{amb} = -40 \text{ }^\circ\text{C}$

Fig 12. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



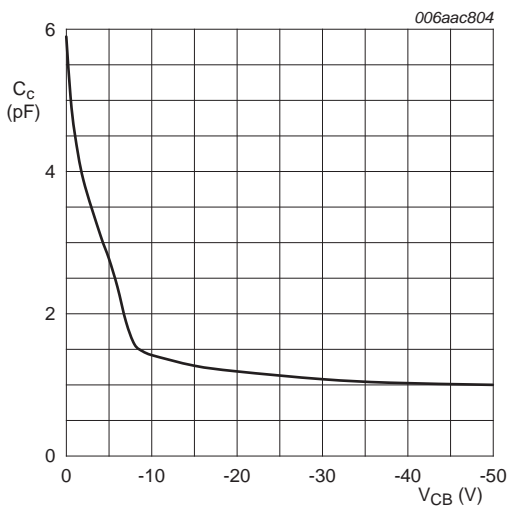
$V_{CE} = -0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 13. TR2 (PNP): On-state input voltage as a function of collector current; typical values



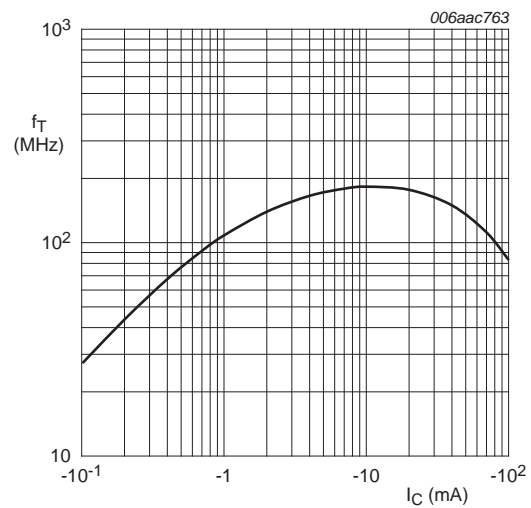
$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig 14. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 15. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = -5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

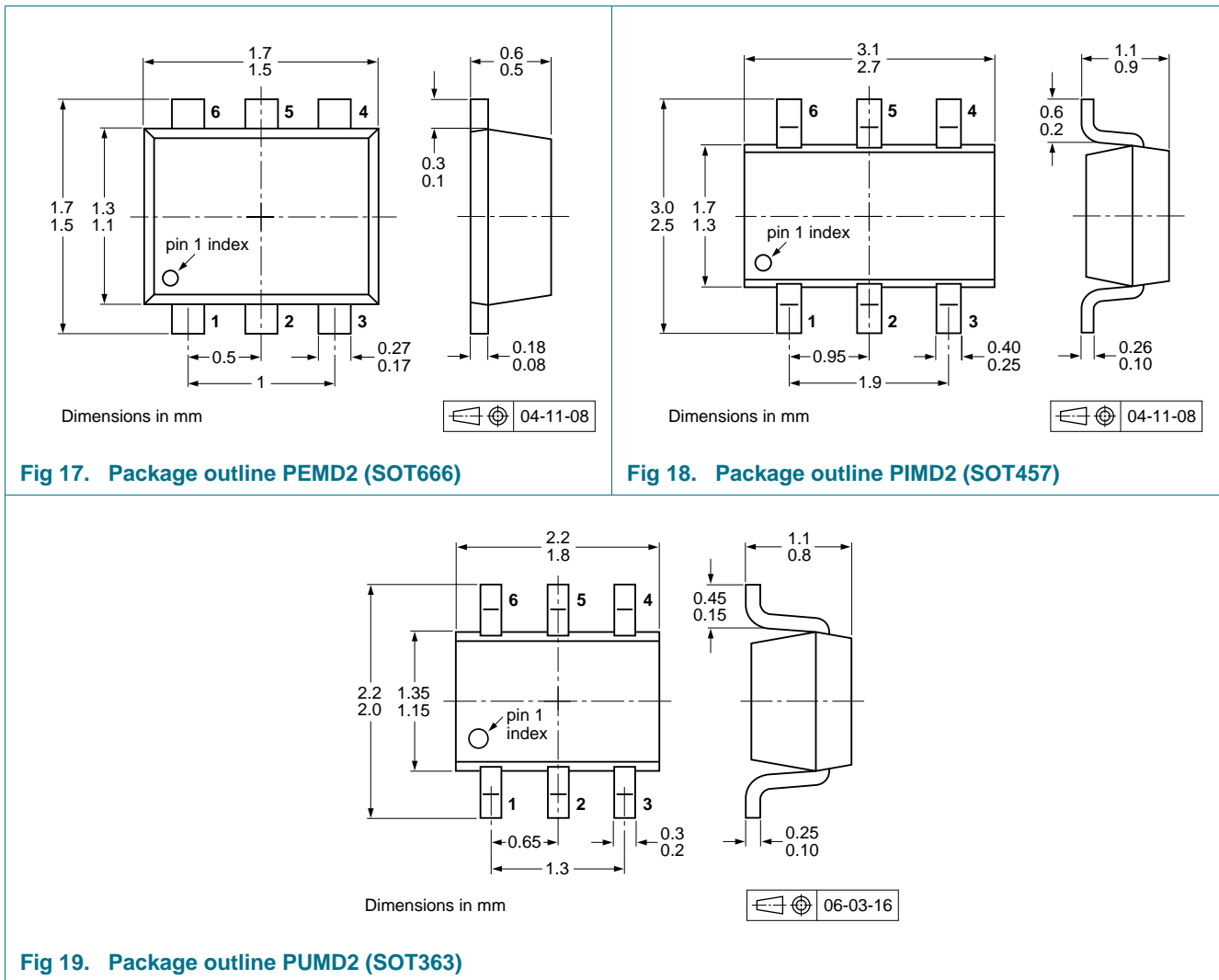
Fig 16. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Soldering

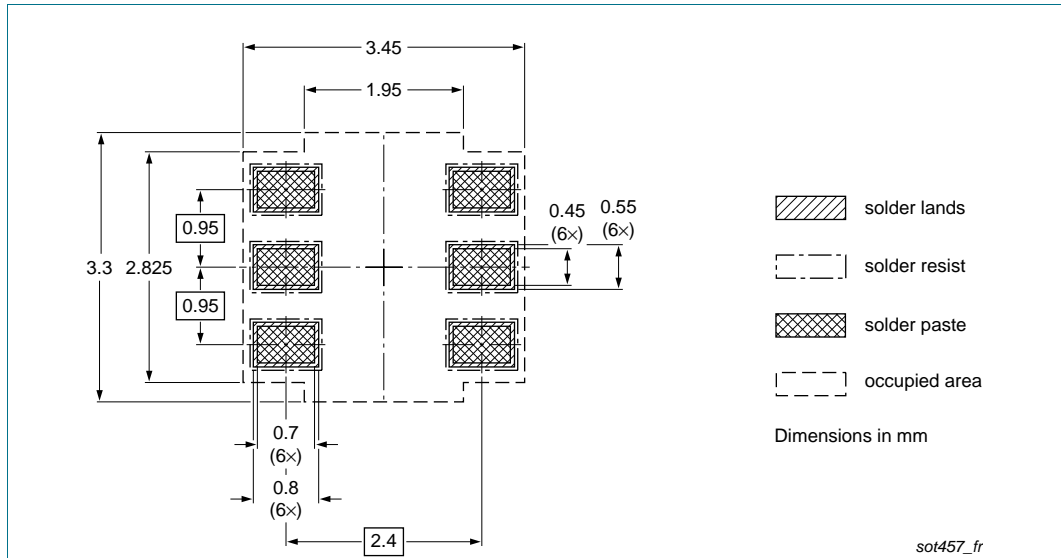


Fig 20. Reflow soldering footprint PIMD2 (SOT457)

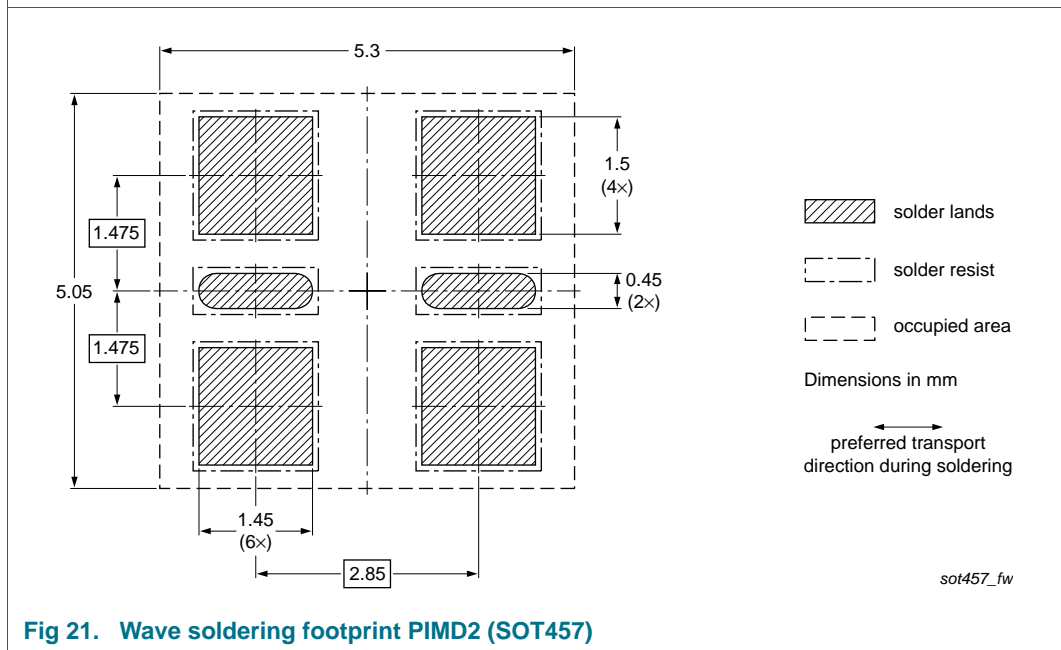


Fig 21. Wave soldering footprint PIMD2 (SOT457)

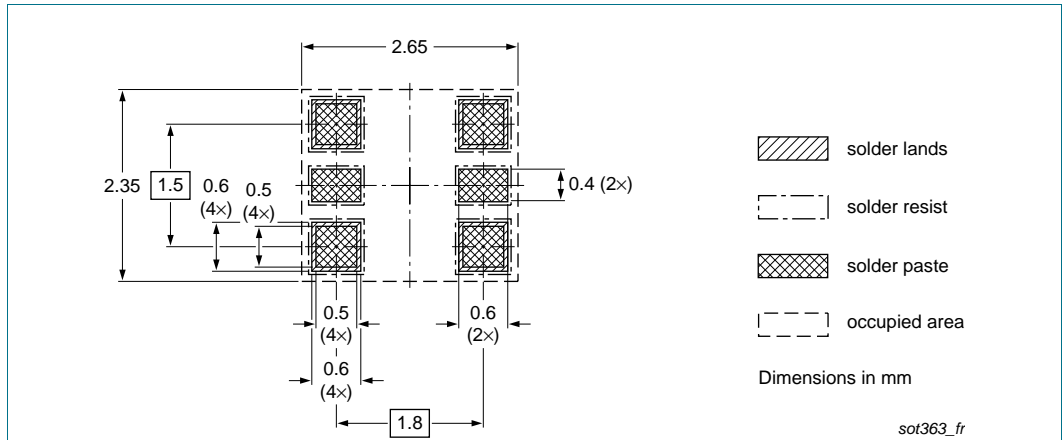


Fig 22. Reflow soldering footprint PUMD2 (SOT363)

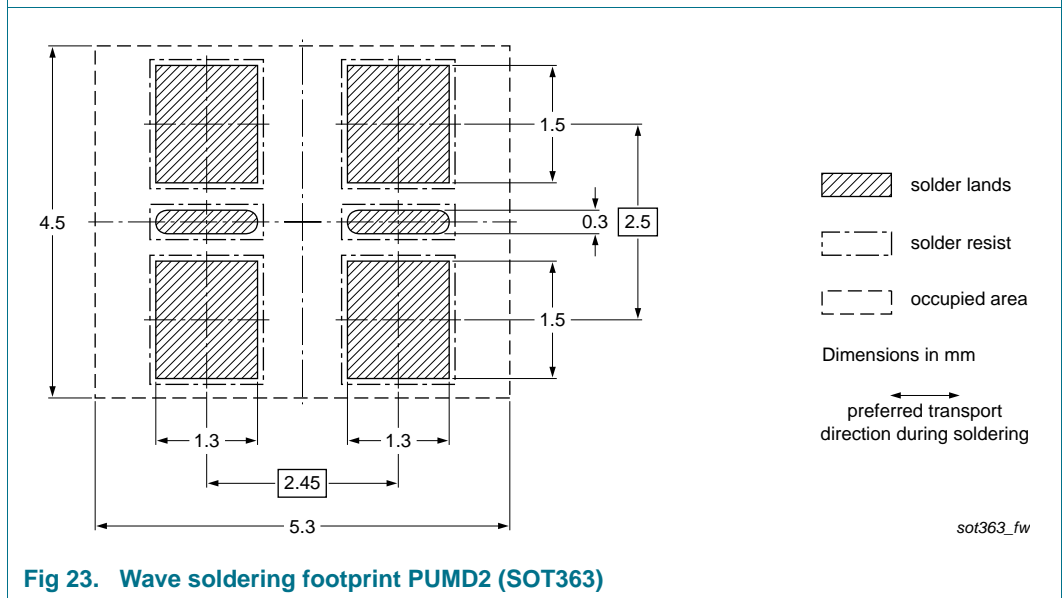
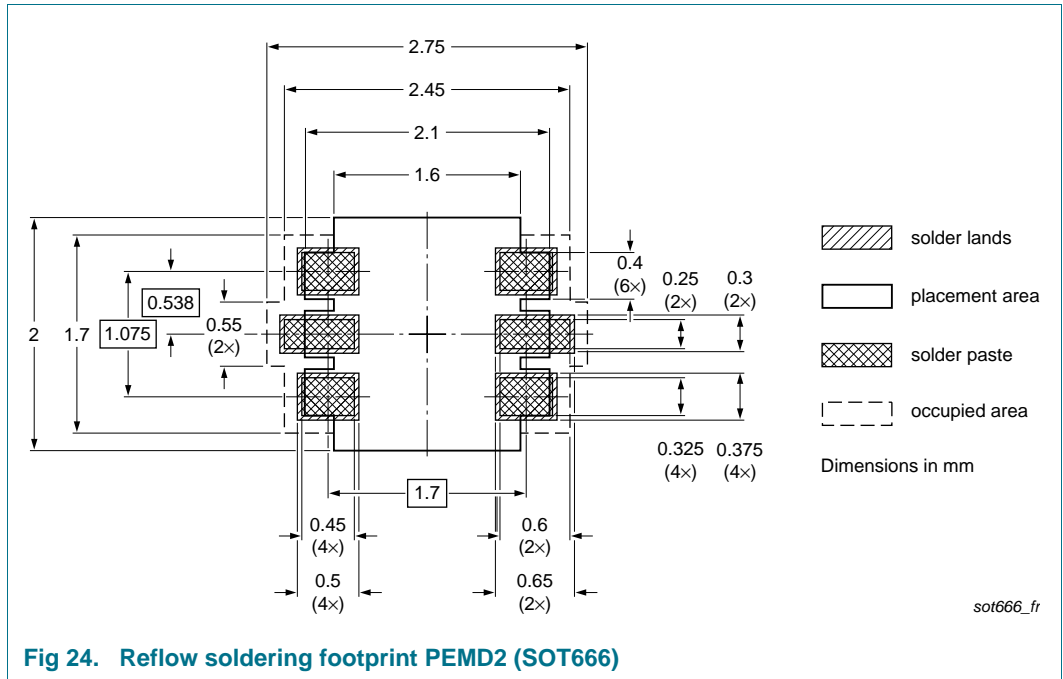


Fig 23. Wave soldering footprint PUMD2 (SOT363)



11. Revision history

Table 9. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------|--------------|--|---------------|-----------------------|
| PEMD2_PIMD2_PUMD2 v.8 | 20131114 | Product data sheet | - | PEMD2_PIMD2_PUMD2 v.7 |
| Modifications: | | <ul style="list-style-type: none"> • Section 1 “Product profile”: updated • Section 4 “Marking”: updated • Figure 1 to 4, 9, 10, 15 and 16: added • Section 5 “Limiting values”: updated • Section 6 “Thermal characteristics”: updated • Figure 5 to 8 and 11 to 14: updated • Table 8 “Characteristics”: I_{CEO} updated, f_T added • Section 8 “Test information”: added • Section 12 “Legal information”: updated | | |
| PEMD2_PIMD2_PUMD2 v.7 | 20080924 | Product data sheet | - | PEMD2_PIMD2_PUMD2 v.6 |
| PEMD2_PIMD2_PUMD2 v.6 | 20042104 | Product specification | - | PEMD2_PIMD2_PUMD2 v.5 |
| PEMD2_PIMD2_PUMD2 v.5 | 20030606 | Product specification | - | - |

12. Legal information

12.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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