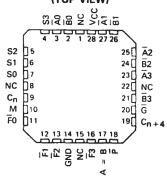
- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off
 Time
- Arithmetic Operating Modes: Addition Subtraction Shift Operand A One Position Magnitude Comparison Plus Twelve Other Arithmetic Operations
- Logic Function Modes: Exclusive-OR Comparator AND, NAND, OR, NOR Plus Ten Other Logic Operations

SN54LS181	, SN54S181	•	J	OR V	V P	ACKAGE
SN74LS181,	SN74S181	• •	. D\	N OR	N	PACKAGE

	TOP (TOP)	VIEW)	
BO	d T	724	Vcc
Ão		23	Ā1
S3	[]3	22	Ā1 B 1 Ā2 B 2 Ā3 B 3 G
S2	[]₄	21	Ā2
S1	[]5	20	B 2
S0	[6	19	Ā3
Cn	[] ¹	18	B 3
м	Цв	17	G
M F0 F1 F2	Ľ۹	16	<u>C</u> n + 4 P
F1	[]10	15	P
	יים	14	A ≃ B
GND	<u>[</u> 12	13	F3

SN54LS181, SN54S181... FK PACKAGE (TOP VIEW)



NC - No internal connection

TYPICAL ADDITION TIMES

NUMBER	ADDITI	ON TIMES	PA	CKAGE COUNT	CARRY METHOD
OF BITS	USING 'LS181 AND 'S182	USING 'S181 AND 'S182	ARITHMETIC/ LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	BETWEEN ALUs
1 to 4	24 ns	11 ns	1		NONE
5 to 8	40 ns	18 ns	2		RIPPLE
9 to 16	44 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	68 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The 'LS181 and 'S181 are arithmetic logic units (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54S182 or SN74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'S182 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under typical applications data for the 'S182.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description (continued)

The 'LS181 and 'S181 will accommodate active-high data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	Ā ₀	Bo	Ā1	B ₁	Ā2	B ₂	Ā3	B ₃	Ē٥	F ₁	F ₂	F3	Cn	C _{n+4}	P	Ğ
Active-high data (Table 2)	A ₀	BO	A ₁	B1	A ₂	B ₂	A ₃	B3	FO	F ₁	F2	F3	Ē'n	Cn+4	Х	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The 'LS181 or 'S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with $C_n = H$ when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (Cn + 4) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT Cn	OUTPUT C _{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
Н	н	A ≥ B	A < B
н	L	A < 8	A > B
L	н	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of -55 °C to 125°C; Series 74LS and 74S devices are characterized for operation from 0°C to 70°C.

signal designations

In both Figures 1 and 2, the polarity indicators (\square) indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'LS181 and 'S181, together with the 'S182, can be used with the signal designation of either Figure 1 or Figure 2.



SN54LS181, SN54S181 SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS SDLS136 – DECEMBER 1972 – REVISED MARCH 1988

'S182 'LS181 OR 'S181 CPG ALU C_n (1) S0<u>(6)</u> S1<u>(5)</u> CI 0 PO (3) (15) P (0...15) CP CP0 \$2⁽⁴⁾ $M \frac{0}{31}$ (17) G G0 (2) CGO (0...15) CG \$3⁽³⁾ (14) A = B P1 (5) 6(P=Q) CP1 <u>G</u>1 (4) $(16) C_{n+4}$ M(8) Cn(7) CG1 4 (0...15) CO P2 (8) (6) Cn + 8 CI CP1 CO1 G2(7) CG2 P3(10) $\overline{A0}\frac{(2)}{\overline{B0}}$ (11) Cn+16 (9) F0 Ρ CP3 1 CO3 [1] <u>G</u>3⁽⁹⁾ Q $\overline{\overline{A}1}\frac{(23)}{(22)}$ $\overline{B1}\frac{(23)}{(22)}$ CG3 $(17) C_{n+24}$ P4(14) Ρ (10) F1 [2] CP4 CO5 $\overline{G4}^{(13)}$ Ā2(21) Q CG4 B2(20) Ρ (11) F2 P5(16) (22) Cn + 32 [4] CP5 C07 Q A3(19) G5(15) (13) F3 Ρ CG5 B3(18) P6(19) [8] Q CP6 <u>G</u>6⁽¹⁸⁾ CG6 P7 (21) CP7 G7⁽²⁰⁾ CG7

logic symbols[†] and signal designations (active-low data)

[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for dual-in-line and "small outline" packages.

FIGURE 1 (USE WITH TABLE 1)

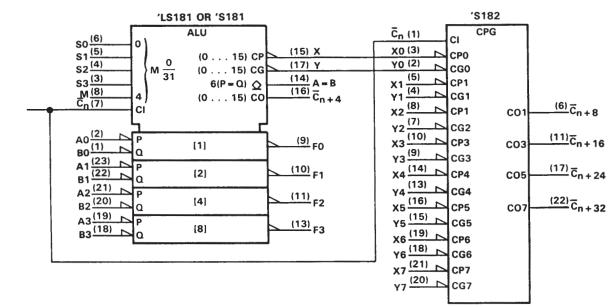
т	۰Δ	R	t.	F	1
	~	2	-	-	

					ACTIVE-LOW DA	ТА
	SELE	CTION		M = H	M = L; ARITHM	ETIC OPERATIONS
				LOGIC	Cn = L	Cn = H
S3	S2	S1	S0	FUNCTIONS	(no carry)	(with carry)
L	L	L	L	F=A	F = A MINUS 1	F = A
L	L	L	н	F = AB	F = AB MINUS 1	F = AB
ι L	L	н	L	F = A + B	$F = A\overline{B}$ MINUS 1	F = AB
L L	L	н	н	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	н	L	L	$F = \overline{A + B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
L	н	L	н	F = B	$F = AB PLUS (A + \overline{B})$	$F = AB PLUS (A + \overline{B}) PLUS 1$
L	н	н	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	н	н	н	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B}) PLUS 1$
н	L	L	L	F = AB	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
н	L	L	н	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
н	L	н	L	F=B	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
Н	L	н	н	F = A + B	F = (A + B)	F = (A + B) PLUS 1
Н	н	L	L	F=0	$F = A PLUS A^{\ddagger}$	F = A PLUS A PLUS 1
н	н	L	н	F ≕ AB	F = AB PLUS A	F = AB PLUS A PLUS 1
Н	н	н	L	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
н	н	н	н	F=A	F = A	F = A PLUS 1

[‡]Each bit is shifted to the next more significant position.



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logic symbols[†] and signal designations (active-high data)

[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for dual-in-line and "small outline" packages.

FIGURE 2 (USE WITH TABLE 2)

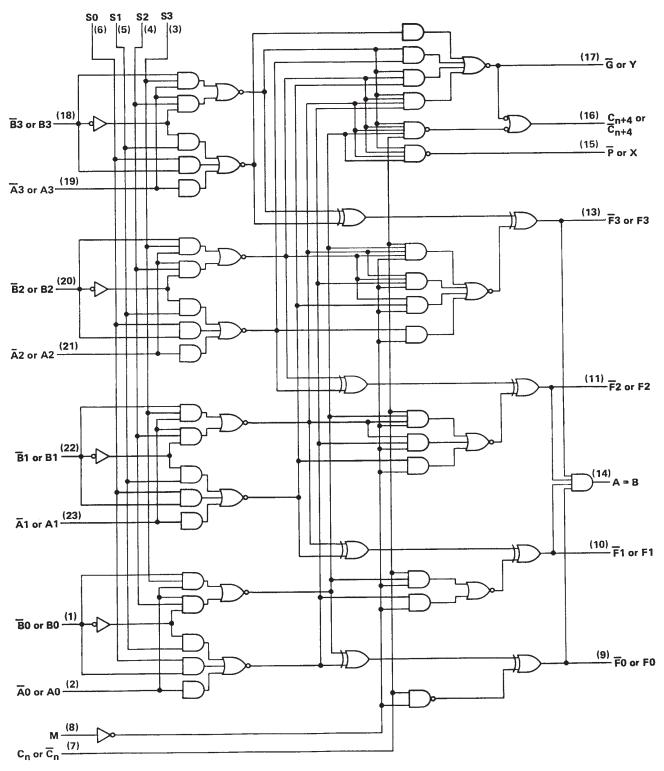
TABLE 2

	051.5	OTION			ACTIVE-HIGH DA	ТА
	SELE	CTION		M = H	M = L; ARITHM	ETIC OPERATIONS
S 3	S2	S1	S0	LOGIC	<mark>C</mark> n = H (no carry)	<mark>¯C</mark> n ≕ L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	н	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	н	L	F = AB	$F = A + \overline{B}$	$F = (A + \overline{B}) PLUS 1$
L	L	н	н	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	н	L	L	$F = \overline{AB}$	F = A PLUS AB	F = A PLUS AB PLUS 1
L	н	L	н	F = B	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS 1
L	н	н	L	F = A 🕀 B	F = A MINUS B MINUS 1	F = A MINUS B
L	н	н	н	F = AB	F = AB MINUS 1	$F = \overline{AB}$
н	L	L	L	F = A + B	F = A PLUS AB	F = A PLUS AB PLUS 1
н	L	L	н	F = A 🕀 B	F = A PLUS B	F = A PLUS B PLUS 1
н	L	н	L	F = B	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS 1
н	L	н	н	F = AB	F = AB MINUS 1	F = AB
н	н	L	L	F = 1	F = A PLUS A [†]	F = A PLUS A PLUS 1
н	н	L	н	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
н	н	н	L	F = A + B	$F = (A + \overline{B}) PLUS A$	$F = (A + \overline{B}) PLUS A PLUS 1$
н	н	н	н	F=A	F = A MINUS 1	F = A

[†] Each bit is shifted to the next more significant position.



logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.



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absolute maximum ratings over reco	on	nm	en	nde	ed	ор	er	ati	ing	j fi	ree)-a	ir :	ter	np	er	at	ur	e r	ar	Ige	e (1	un	le	S S	ot	he	rw	ise	n	oted)	
Supply voltage, V _{CC} (see Note 1)						•											•											•		•	7 V	
Input voltage														•	•												•	•			5.5 V	
Interemitter voltage (see Note 2)																																
Operating free-air temperature range																																
																															70°C	
Storage temperature range	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•		-6	۶°ئ	C t	o 1	150°C	

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with inputs S2 or S3, and to each \vec{B} input in conjunction with inputs S0 or S3.

recommended operating conditions

	SI	N54LS1	81	SM	174LS1	81	
	MIN	NOM	MAX	MIN	NOM	MAX	רואט
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH (All outputs except A = B)			-400			-400	μA
Low-level output current, IOL			4			8	mA
Operating free-air temperature, T _A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADA	METER	TEC	T CONDITIONS	.t	SI	154LS1	81	S	N74LS1	81	
	FANAI	VIETER	153	CONDITIONS		MIN	TYP [‡]	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level in	nput voltage				2			2			V
VIL	Low-level in	put voltage						0.7			0.8	V
VIK	Input clamp	voltage	V _{CC} = MIN,	I _I = -18 mA				-1.5			-1.5	V
Vон		utput voltage, except A = B	V _{CC} = MIN, V _{IL} = V _{IL} max,			2.5	3.4		2.7	3.4		v
юн		utput current,	$V_{CC} = MIN,$ $V_{1L} = V_{1L} max,$	V _{IH} = 2 V,	·			100			100	μA
			VIL VIL Max,	VOH 0.5 V	IOL = 4 mA		0.25	0.4		0.25	0.4	-
VOL	Low-level output	All outputs	V _{CC} = MIN,	V _{IH} = 2 V,	IOL = 8 mA					0.35	0.5	v
•OL	voltage	Output G	VIL = VIL max		I _{OL} = 16 mA		0.47	0.7		0.47	0.7	v
	Vortage	Output P			IOL = 8 mA		0.35	0.6		0.35	0.5	
	Input	Mode input						0.1			0.1	
ų.	current at	Any A or B input	V _{CC} = MAX,	V. = 5 5 V				0.3			0.3	
1	max. input	Any S input		v] = 5.5 v				0.4			0.4	mA
	voltage	Carry input						0.5			0.5	
	High-level	Mode input						20			20	
цн	input	Any \overline{A} or \overline{B} input	V _{CC} = MAX,	$V_1 = 2.7 V$				60			60	μA
.111	current	Any S input		• [- 2.7 •				80			80	μA
	burrent	Carry input						100			100	
	Low-level	Mode input						-0.4			-0.4	
hε	input	Any A or B input	V _{CC} = MAX,	$V_1 = 0.4 V$				-1.2			-1.2	mA
.16	current	Any S input		1 0.4 1				-1.6			-1.6	
		Carry input						-2			-2	1
los		t output current, except A = B §	V _{CC} = MAX			-6		40	-5		-42	mA
Icc	Supply curre	ent	V _{CC} = MAX,	See Note 3	Condition A		20	32		20	34	mA
					Condition B		21	35		21	37	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE 3: With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.



SN54LS181, SN54S181 SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS SDLS136 – DECEMBER 1972 – REVISED MARCH 1988

PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	мах	UNIT
^t PLH	C				18	27	ns
^t PHL	Cn	C _{n+4}			13	20	113
^t PLH	Any A or B	6	M = 0 V, S0 = S3 = 4.5 V,		25	38	ns
^t PHL	Any A or B	C _{n+4}	S1 = S2 = 0 V (SUM mode)		25	38	113
^t PLH	Any Ā or B		M = 0 V, S0 = S3 = 0 V		27	41	ns
^t PHL	Any A or B	C _{n+4}	S1 = S2 = 4.5 V (DIFF mode)		27	41] '''
^t PLH	<u> </u>	A F	M = 0 V		17	26	ns
^t PHL	C _n	Any F	(SUM or DIFF mode)		13	20	115
tPLH		G	M = 0 V, S0 = S3 = 4.5 V,		19	29	
tPHL	Any A or B		S1 = S2 = 0 V (SUM mode)		15	23	ns
^t PLH		Ğ	M = 0 V, S0 = S3 = 0 V,		21	32	
^t PHL	Any A or B	G	S1 = S2 = 4.5 V (DIFF mode)		21	32	ns
^t PLH		ব	M = 0 V, S0 = S3 = 4.5 V,		20	30	
tPHL	Any A or B	٢	S1 = S2 = 0 V, (SUM mode)		20	30	ns
tPLH			M = 0 V, S0 = S3 = 0 V,	1	20	30	
tPHL	Any A or B	P	S1 = S2 = 4.5 V (DIFF mode)		22	33	ns
tPLH	7 5	=	M = 0 V, S0 = S3 = 4.5 V,		21	32	
^t PHL	Ā _i or Ē _i	Fi	S1 = S2 = 0 V (SUM mode)		13	20	ns
tPLH	T D		M = 0 V, S0 = S3 = 0 V,		21	32	
tPHL.	Ā _i or B _i	Fi	S1 = S2 = 4.5 V (DIFF mode)		21	32	ns
tPLH	7 7	7			22	33	
tPHL.	Ā; or B;	Fi	M = 4.5 V (logic mode)		26	38	ns
^t PLH			M = 0 V, S0 = S3 = 0 V,	1	33	50	-
^t PHL	Any Ā or B	A = B	S1 = S2 = 4.5 V (DIFF mode)		41	62	ns

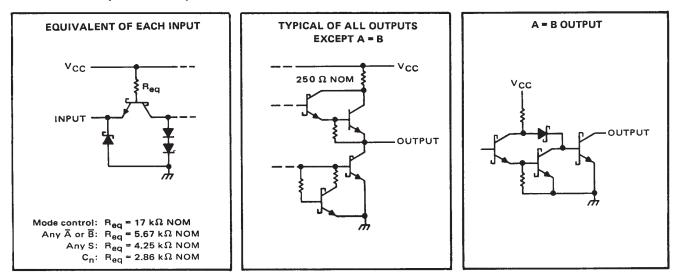
switching characteristics, V_{CC} = 5 V, T_A = 25°C, (C_L = 15 pF, R_L = 2 k Ω , see note 4)

[†]tpLH = propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage wveforms are shown in Section 1. Refer to Parameter Measurement Information page for test conditions.

schematics of inputs and outputs





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note	1)															•		. 7	V
Input voltage															•	•		. 5.5	V
Interemitter voltage (see Note 2																		. 5.5	V
Operating free-air temperature:	SN54S181											•				5!	5°C 1	to 125`	С
	SN74S181																0°C	; to 70	C
Storage temperature range				•			•	•	•	•	•		·	•		-6	5°C 1	to 150	°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple emitter transistor. For this circuit, this rating applies to each A input in conjunction with inputs S2 or S3, and to each \overline{B} input in conjunction with inputs S0 or S3.

recommended operating conditions

	S	N54S18	31	5			
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH (All outputs except A = B)			-1			-1	mA
Low-level output current, IOI			20			20	mA
Operating free-air temperature, TA	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER					+	S	SN54S18	31	5	UNIT			
	PARAN	IETER	TE	ST CONDITIONS	1	MIN	TYP‡	MAX	MIN	түр‡	MAX	UNIT	
VIH	High-level in	put voltage				2			2			V	
VIL	Low-level in							0.8			0.8	V	
VIK			V _{CC} = MIN,	l _l = -18 mA				-1.2			-1.2	V	
	High-level output voltage.			V _{IH} = 2 V,		0.5	2.4		2.7	3.4		v	
Vон	any output	except A = B	V _{IL} = 0.8 V,	IOH = -1 mA		2.5	3.4		2.1	3.4		v	
	High-level o	utput current,	V _{CC} = MIN,	V _{IH} = 2 V,				250			250	μA	
юн	A = B outpu	it only	V _{1L} = 0.8 V,	V _{OH} = 5.5 V				250			200	μ <u>η</u>	
			V _{CC} = MIN,	V _{IH} = 2 V,				0.5			0.5	v	
VOL	Low-level or	utput voltage	V _{IL} = 0.8 V,	l _{OL} = 20 mA				0.5					
	Input currer	nt at		Vi = 5.5 V				1			1	mA	
ų –	maximum input voltage		V _{CC} = MAX,	v] - 5.5 v		<u> </u>					•		
		Mode input						50			50		
	High-level	Any Ā or B input		V 2 E V				150			150	μΑ	
ΙΗ	input	Any S input		V _{CC} = MAX, V _I = 2.5 V				200			200	00	
	current	Carry input	1					250			250		
		Mode input						-2			-2		
	Low-level	Any A or B input		Vi = 0.5 V				-6			-6	I mA	
41	input	Any S input	V _{CC} = MAX,	VI ~ 0.5 V				-8		-8			
	current	Carry input	1				-10			-10			
1	Short-circui	t output current,	V _{CC} = MAX			-40		-100	-40		100	mA	
los	OS any output except $A = B^{\S}$								ļ				
			V _{CC} = MAX,	T _A = 125°C,	W package			195					
Icc	Supply curr	rent	See Note 3		only							mA	
			$V_{CC} = MAX,$	See Note 3	All packages		120	220		120	220		

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured for the following conditions (the typical and maximum values apply to both):

A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.

B. S0 through S3 and M are at 4.5 V, all other inputs grounded, and all outputs are open.



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PARAMETER [†]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNI
tPLH	0	6			7	10.5	ns
^t PHL	C _n	C _{n+4}			7	10.5	
tPLH	A	C	M = 0 V, S0 = S3 = 4.5 V,		12.5	18.5	ns
tPHL	Any Ā or B	C _{n+4}	S1 = S2 = 0 V (SUM mode)		12.5	18.5	
tPLH	Any Ā or B	C	M = 0 V, S0 = S3 = 0 V,		15.5	23	ns
tPHL	AnyAOrb	C _{n+4}	S1 = S2 = 4.5 V (DIFF mode)		15.5	23	
tPLH	0	Any F	M = 0 V		7	12	ns
tPHL	- C _n	Anyr	(SUM or DIFF mode)		7	12	
tPLH	A 7 7	ō	M = 0 V, S0 = S3 = 4.5 V,		8	12	ns
tPHL	- Any Ā or B	6	S1 = S2 = 0 V (SUM mode)		7.5	12	
tPLH		G	M = 0 V, S0 = S3 = 0 V,		10.5	15	ns
tPHL	Any Ā or B	G	$S1 = S2 = 4.5 V (\overline{DIFF} \text{ mode})$		10.5	15	
^t PLH	A	P	M = 0 V, S0 = S3 = 4.5 V,		7.5	12	ns
tPHL	Any à or B	F	S1 = S2 = 0 V (SUM mode)		7.5	12	
tPLH		Ŧ	M = 0 V, S0 = S3 = 0 V,		10.5	15	ns
tPHL	Any Ā or B	F	S1 = S2 = 4.5 V (DIFF mode)		10.5	15	
tPLH		Fi	M = 0 V, S0 = S3 = 4.5 V,		11	16.5	ns
^t PHL	- Ā _i or B _i	ri -	S1 = S2 = 0 V (SUM mode)		11	16.5	יי ך
^t PLH			M = 0 V, S0 = S3 = 0 V,		14	20	
^t PHL	$\overline{A_i}$ or $\overline{B_i}$	Fi	S1 = S2 = 4.5 V (DIFF mode)		14	22	- n
tPLH		_			14	20	
^t PHL	- Ā _i or B _i	Fi	M = 4.5 V (logic mode)		14	22] "
tPLH			M = 0 V, S0 = S3 = 0 V,		15	23	n
tPHL	Any Ā or B	A = B	S1 = S2 = 4.5 V (DIFF mode)		20	30	۳ [

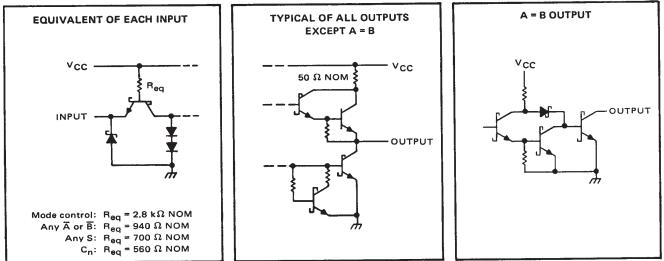
switching characteristics, V_{CC} = 5 V, T_A = 25°C (C_L = 15 pF, R_L = 280 Ω , see note 4)

 $^{\dagger}t_{PLH} \equiv$ propagation delay time, low-to-high-level output

tpHL = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage wveforms are shown in Section 1. Refer to Parameter Measurement Information page for test conditions.

schematics of inputs and outputs





SN54LS181, SN54S181 SN74LS181, SN74S181 **ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS** SDLS136 - DECEMBER 1972 - REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION SUM MODE TEST TABLE

			I INPUT E BIT	OTHER DA	TA INPUTS		OUTPUT	
PARAMETER	TEST APPLY APPLY APPLY 4.5 V GND 4.5 V		APPLY GND	TEST	(See Note 4)			
^Ն ԲԼℍ ՆԲℍԼ	Āi	Ξ _i	Bi None Remaining Cn A and B Cn Cn		Fi	In-Phase		
	Bi	Āi	None	Remaining A and B	Cn	Fi	In-Phase	
tPLH tPHL	Āi	Bi None None Remaining Â and B, Cr Â Â A </td <td>P</td> <td>In-Phase</td>		P	In-Phase			
	Bi	Āi	None	None	None Remaining Ā and B, C _n		in-Phase	
	Āj	None	Bi	Remaining B	Remaining Ā, C _n	G	in-Phase	
tPLH tPHL	Β _i	None	Āi	Remaining B	Remaining Ã, C _n	G	In-Phase	
	Cn	None	None	A11 Ā	AII B	Any F or C _{n+4}	In-Phase	
^t թլн ^t թнւ	Āi	None	B _i	Remaining B	Remaining Ã, C _n	C _{n+4}	Out-of-Phase	
	Bi	None	Āi	Remaining Remaining B A, Cn		Cn+4	Out-of-Phase	

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

DIFF MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

tPHL A, B, Cn Receiving						•			
APPLY TESTAPPLY 4.5 VAPPLY GNDAPPLY 4.5 VAPPLY GNDAPPLY GNDAPPLY GNDAPPLY GNDAPPLY GNDAPPLY GNDTEST(See Note 4) $IPLH$ \overline{A}_i None \overline{B}_i \overline{A}_i Remaining \overline{A} Remaining \overline{B}, C_n \overline{F}_i In-Phase $IPLH$ \overline{B}_i \overline{A}_i None \overline{B}_i Remaining \overline{A} $\overline{B}_i C_n$ \overline{F}_i Out-of-Phase $IPLH$ \overline{B}_i \overline{A}_i None \overline{B}_i NoneRemaining \overline{A} and \overline{B}, C_n \overline{P} In-Phase $IPLH$ \overline{B}_i \overline{A}_i None \overline{B}_i NoneRemaining \overline{A} and \overline{B}, C_n \overline{P} Out-of-Phase $IPLH$ \overline{B}_i \overline{A}_i NoneNoneRemaining \overline{A} and \overline{B}, C_n \overline{P} Out-of-Phase $IPLH$ \overline{B}_i \overline{A}_i NoneNoneRemaining \overline{A} and \overline{B}, C_n \overline{G} Out-of-Phase $IPHL$ \overline{A}_i \overline{B}_i None \overline{A}_i Remaining \overline{A} and \overline{B}, C_n \overline{G} Out-of-Phase $IPHL$ \overline{A}_i \overline{B}_i None \overline{A}_i Remaining \overline{A} and \overline{B}, C_n \overline{G} Out-of-Phase $IPHL$ \overline{A}_i None \overline{A}_i Remaining \overline{A} and \overline{B}, C_n $\overline{A} = B$ In-Phase $IPHL$ \overline{A}_i None \overline{A}_i Remaining \overline{A} and \overline{B} $\overline{A} = B$ Out-of Phase $IPHL$ \overline{A}_i \overline{A}_i None \overline{A}_i					OTHER DA				
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	PARAMETER		APPLY	APPLY	APPLY	APPLY			
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		TEST	4.5 V	GND	4.5 V	GND	1531	(266 14016 4)	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	^t PLH	7.	None	<u>.</u>		-	Ē	In-Phase	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	tPHL		None	51	Ā	B, C _n			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	tPLH		<u></u> .	None			Ē.	Out-of-Phase	
VPLH tPHLAiNoneBi ANoneA and B. CnPIn-PhaseIPLH IPLHBiAiNoneNoneRemaining A and B. CnPOut-of-PhaseIPLH IPLHBiAiNoneNoneRemaining A and B. CnPOut-of-PhaseIPLH IPLHAiBiNoneNoneRemaining A and B. CnGIn-PhaseIPLH IPHLAiBiNoneAiNoneRemaining A and B. CnGOut-of-PhaseIPLH IPHLAiNoneAiNoneRemaining B. CnGOut-of-PhaseIPLH IPHLAiNoneBi AA B. CnA BIn-PhaseIPLH IPHLAiNoneNoneRemaining B. CnA BOut-of-PhaseIPLH IPHLAiAiNoneRemaining A B. CnA BOut-of PhaseIPLH IPHLCnNoneNoneAiii A and BNoneCn+4 Gr any FIn-PhaseIPLH IPLHAiBiNoneNoneRemaining A B. CnA BOut-of PhaseIPLH IPHLCnNoneNoneAiii A and BNoneCn+4 Gr any FIn-PhaseIPLH IPLHAiBiNoneNoneRemaining A B. CnCn+4 Gr any FIn-Phase	^t ₽HL			INONE	Ā	B, C _n	.,		
tPHLHighHomeOrHomeA and B, CntPLH \overline{B}_i \overline{A}_i NoneNoneRemaining \overline{A} and B, Cn \overline{P} Out-of-PhasetPLH \overline{A}_i \overline{B}_i NoneNoneRemaining \overline{A} and B, Cn \overline{G} In-PhasetPLH \overline{A}_i \overline{B}_i None \overline{A}_i Remaining \overline{A} and B, Cn \overline{G} In-PhasetPLH \overline{A}_i None \overline{A}_i NoneRemaining \overline{A} and B, Cn \overline{G} Out-of-PhasetPLH \overline{A}_i None \overline{B}_i Remaining \overline{A} and \overline{B} , Cn $\overline{A} = B$ In-PhasetPLH \overline{A}_i None \overline{B}_i \overline{A} \overline{B}_i $\overline{A} = B$ In-PhasetPLH \overline{A}_i None \overline{B}_i \overline{A} \overline{B}_i $\overline{A} = B$ Out-of-PhasetPLH \overline{B}_i \overline{A}_i NoneRemaining \overline{A} \overline{B}_i $\overline{A} = B$ Out-of PhasetPLH \overline{B}_i \overline{A}_i None \overline{A} \overline{B}_i $\overline{A} = B$ Out-of PhasetPLH \overline{B}_i \overline{A}_i None \overline{A} \overline{B}_i $\overline{C}_n + 4$ In-PhasetPLH \overline{A}_i \overline{B}_i NoneNone \overline{A} \overline{A} $\overline{C}_n + 4$ In-PhasetPLH \overline{A}_i \overline{B}_i NoneNone \overline{A} \overline{A} $\overline{C}_n + 4$ Out-of-PhasetPLH \overline{A}_i \overline{B}_i NoneNone \overline{A} \overline{A} $\overline{C}_n + 4$ Out-of-Phase<	^t PLH	<u>Ā</u> .	None	.	None	-	P	In-Phase	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	1PHL		None		None	A and B, C _n			
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	^t PLH	5.	ā.	None	None		ā	Out-of-Phase	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	^t PHL	Pi			None	A and B, Cn		001077800	
tPHLHiHiHoneAAABOut-of-PhasetPLH \overline{B}_i None \overline{A}_i None \overline{A} and \overline{B} , C_n \overline{G} Out-of-PhasetPLH \overline{A}_i None \overline{B}_i \overline{A} Remaining \overline{A} \overline{B} , C_n $\overline{A} = B$ In-PhasetPLH \overline{A}_i None \overline{B}_i \overline{A} \overline{B} , C_n $A = B$ In-PhasetPLH \overline{B}_i \overline{A}_i NoneRemaining \overline{A} \overline{B} , C_n $A = B$ Out-of PhasetPLH \overline{B}_i \overline{A}_i None \overline{A} \overline{B} , C_n $A = B$ Out-of PhasetPLH C_n NoneNone \overline{A} \overline{B} , C_n $A = B$ In-PhasetPLH \overline{A}_i \overline{B}_i NoneNone \overline{A} \overline{B} , C_n $A = B$ Out-of PhasetPLH \overline{A}_i \overline{B}_i NoneNone \overline{A} \overline{B} C_{n+4} Out-of-PhasetPHL \overline{A}_i \overline{B}_i NoneNone \overline{A} \overline{B} C_{n+4} Out-of-PhasetPHL \overline{A}_i \overline{B}_i NoneNone \overline{A} \overline{A} \overline{C}_{n+4} Out-of-PhasetPHL \overline{A}_i \overline{B}_i NoneNone \overline{A} \overline{B} \overline{C}_{n+4} Out-of-Phase	^t PLH	<u>.</u>	<u>.</u>	None	None		อ	in-Phase	
Image: termBi iNoneAi iNoneAi iNoneAi and \overline{B} , C_n GOut-of-PhaseIPLH \overline{A}_i None \overline{B}_i Remaining \overline{A} Remaining \overline{B} , C_n A = BIn-PhaseIPLH \overline{B}_i \overline{A}_i NoneRemaining \overline{A} Remaining \overline{B} , C_n A = BOut-of PhaseIPLH \overline{B}_i \overline{A}_i NoneRemaining \overline{A} Remaining \overline{B} , C_n A = BOut-of PhaseIPLH \overline{C}_n NoneNoneAll \overline{A} and \overline{B} None \overline{C}_{n+4} or any \overline{F} In-PhaseIPLH \overline{A}_i \overline{B}_i NoneNoneRemaining $\overline{A}, \overline{B}, C_n$ C_{n+4}Out-of-PhaseIPLH \overline{A}_i \overline{B}_i NoneNoneRemaining $\overline{A}, \overline{B}, C_n$ C_{n+4}Out-of-PhaseIPHL \overline{A}_i \overline{B}_i NoneNoneRemaining $\overline{A}, \overline{B}, C_n$ C_{n+4}Out-of-Phase	^t PHL			None			, C		
tPHL A A and B, Cn tPLH \overline{A}_i None \overline{B}_i Remaining Remaining A = B In-Phase tPHL \overline{A}_i None \overline{B}_i \overline{A} \overline{B}_i \overline{B}_i \overline{A} \overline{B}_i \overline{B}_i \overline{A} \overline{B}_i \overline{B}_i \overline{A} \overline{A} \overline{B}_i \overline{A}	^t PLH	B .	None	Δ.	None	-	ត	Out-of-Phase	
ip HL Ai None Bi \overline{A} \overline{B} , C_n $A = B$ In-Phase ip HL \overline{B}_i \overline{A}_i None $\overline{Remaining}$ $\overline{C_{n+4}}$ $\overline{Out-of-Phase}$ ip HL \overline{A}_i \overline{B}_i None None $\overline{Remaining}$ $\overline{C_{n+4}}$ $\overline{Out-of-Phase}$ ip HL \overline{A}_i \overline{B}_i None None $\overline{Remaining}$ $\overline{C_{n+4}}$ $\overline{Out-of-Phase}$	^t PHL					A and B, Cn			
tPHL A B, Cn tPLH \overline{B}_i \overline{A}_i None Remaining Remaining \overline{B}_i $\overline{A} = B$ Out-of Phase tPHL \overline{C}_n None \overline{A} \overline{B}_i \overline{N}_i \overline{A} \overline{B}_i \overline{A} \overline{A}_i $$	^t PLH	7.	None	B .	-	-	A = B	In-Phase	
Image: second secon	^t PHL	1 1	Roma		Ā	B, Cn			
tPHL Di Ai B, Cn tPLH Cn None None All tPHL Cn None None All tPLH \overline{A}_i \overline{B}_i None All tPLH \overline{A}_i \overline{B}_i None \overline{A}_i \overline{B}_i In-Phase tPLH \overline{A}_i \overline{B}_i None None \overline{A}_i \overline{B}_i Out-of-Phase tPHL \overline{A}_i \overline{B}_i \overline{A}_i \overline{B}_i \overline{A}_i \overline{A}_i \overline{C}_{n+4} $\overline{Out-of-Phase}$	1PLH	<u>.</u>	<u>.</u>	None	l ~	-	A = B	Out-of Phase	
IPLIN Cn None None A and B None Cn + 4 or any F In-Phase IPLH Ai Bi None None Remaining A, B, Cn Cn + 4 Out-of-Phase	^t PHL		^	None	Ā	B, Cn			
tPHL On Hone Ā and 6 or any F tPLH Ā B None None Remaining Ā, B, Cn Cn+4 Out-of-Phase tPHL F F F F F F F	^t PLH	C.	None	None		None	Cn+4	In-Phase	
tPHL Ai Bi None None Ā, B, Cn Cn+4 Out-of-Phase	^t PHL			1 vone	A and B		or any F		
tPHL A, B, Cn Bampining	tPLH	Ā	B. None		None	-	Cate	Out-of-Phase	
tpi H = Remaining	^t PHL						-1174		
	^t PLH	B;	B _i None		None		Cn+4	In -Phase	
	^t PHL] -'				Ā, Ē, C _n		111-111020	

LOGIC MODE TEST TABLE FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER			E BIT	OTHER D	ATA INPUTS		OUTPUT WAVEFORM
PARAMETER	TEST	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	TEST	(See Note 4)
tPLH tPHL	Āi	Bi	None	None	Remaining Ā and B, C _n	Ŧ,	Out-of-Phase
tPLH tPHL	Ēi	Āi	None	None	Remaining Ā and B, C _n	Fi	Out-of-Phase

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.





11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	•	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
JM38510/07801BJA	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07801BJA	Samples
M38510/07801BJA	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 07801BJA	Samples
SN54LS181J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54LS181J	Samples
SN54S181J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54S181J	Samples
SN74LS181N	ACTIVE	PDIP	Ν	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS181N	Samples
SN74LS181N3	OBSOLETE	PDIP	Ν	24		TBD	Call TI	Call TI	0 to 70		
SN74LS181NE4	ACTIVE	PDIP	Ν	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS181N	Samples
SN74S181J	OBSOLETE	CDIP	J	24		TBD	Call TI	Call TI	0 to 70		
SN74S181N	OBSOLETE	PDIP	Ν	24		TBD	Call TI	Call TI	0 to 70		
SN74S181N3	OBSOLETE	PDIP	Ν	24		TBD	Call TI	Call TI	0 to 70		
SNJ54LS181FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 181FK	Samples
SNJ54LS181J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54LS181J	Samples
SNJ54LS181W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS181W	Samples
SNJ54S181FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 181FK	Samples
SNJ54S181J	ACTIVE	CDIP	J	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SNJ54S181J	Samples
SNJ54S181JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S181JT	Samples
SNJ54S181W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S181W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



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11-Apr-2013

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LS181, SN54S181, SN74LS181, SN74S181 :

• Catalog: SN74LS181, SN74S181

• Military: SN54LS181, SN54S181

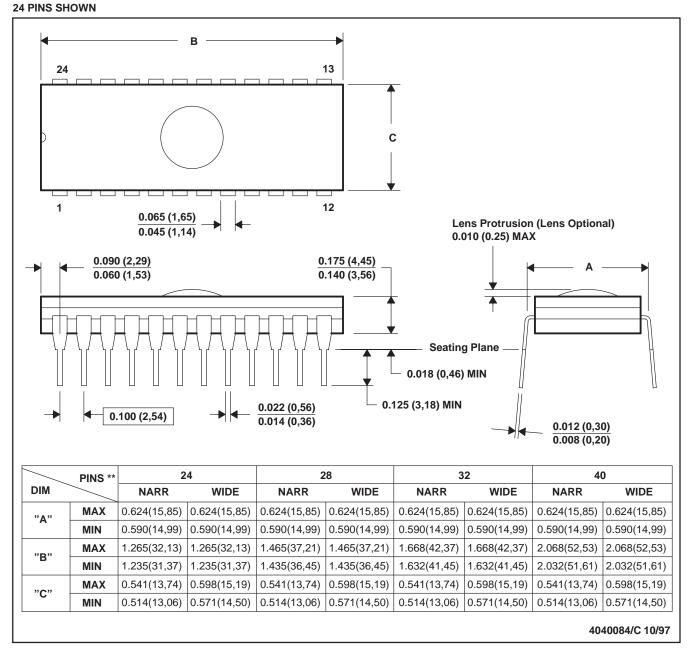
NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

MCDI004A - JANUARY 1995 - REVISED NOVEMBER 1997

CERAMIC DUAL-IN-LINE PACKAGE

J (R-GDIP-T**)



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
- D. This package can be hermetically sealed with a ceramic lid using glass frit.
- E. Index point is provided on cap for terminal identification.



MCER004A - JANUARY 1995 - REVISED JANUARY 1997

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN

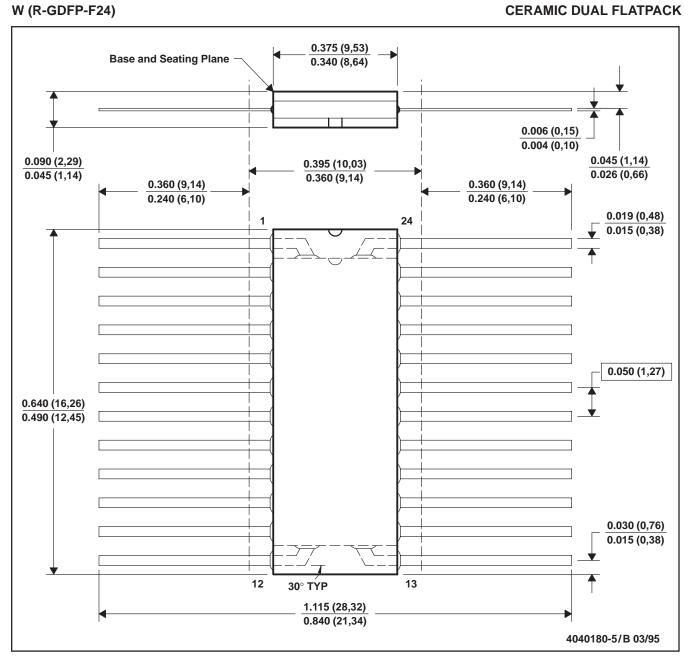


NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB



MCFP007 - OCTOBER 1994



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

- D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
- E. Index point is provided on cap for terminal identification only.



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. Falls within JEDEC MS-004

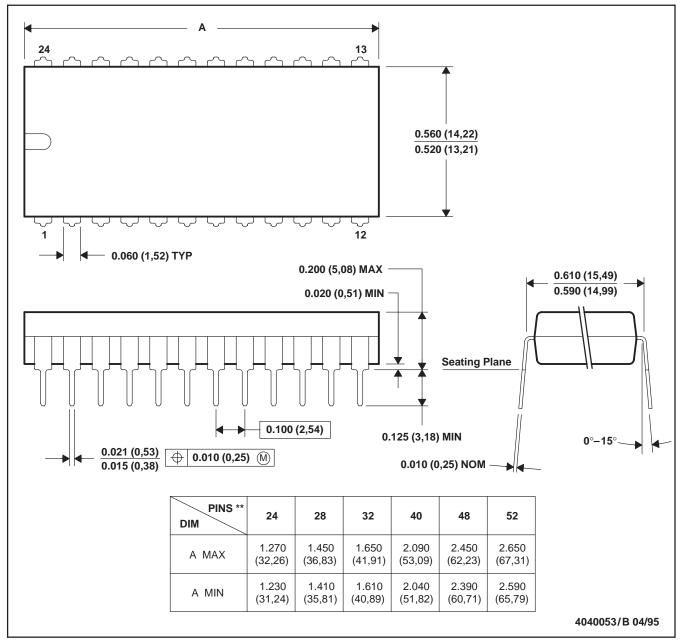


MPDI008 - OCTOBER 1994

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-011
- D. Falls within JEDEC MS-015 (32 pin only)



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