



74LVC161284

LOW VOLTAGE HIGH SPEED IEEE1284 TRANSCEIVER

- HIGH SPEED: $t_{PD} = 9\text{ns}$ (MAX.) at $V_{CC} = 3\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 20\mu\text{A}$ (MAX) at $V_{CC} = 3.6\text{V}$ $T_A = 85^\circ\text{C}$
- TTL COMPATIBLE INPUTS
 $V_{IH} = 2\text{V}$ (MIN) $V_{IL} = 0.8$ (MAX)
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 3.0\text{V}$ to 3.6V
- A PORT HAVE STANDARD 4mA TOTEM POLE OUTPUT
- B PORT HIGH DRIVE SOURCE/SINK CAPABILITY OF 14mA
- SUPPORT IEEE STD 1284-I (LEVEL 1 TYPE) AND IEEE STD 1284-II (LEVEL 2 TYPE) FOR BIDIRECTIONAL PARALLEL COMMUNICATIONS BETWEEN PERSONAL COMPUTER ANT PRINTING PERIPHERALS
- TRANSLATION CAPABILITY ALLOW OUTPUTS ON CABLE SIDE TO INTERFACE WITH 5V SIGNAL
- PULL-UP RESISTOR INTEGRATED ON ALL OPEN-DRAIN OUTPUT ELIMINATE THE NEED FOR DISCRETE RESISTOR
- REPLACE THE FUNCTION OF TWO 74LVC1284 DEVICES

DESCRIPTION

The 74LVC161284 contains eight high speed non inverting bidirectional buffers and eleven control/status non-inverting buffers with open drain outputs fabricated in silicon gate C²MOS technology. It's intended to provide a standard signaling method for a bi-direction parallel peripheral in an Extended Capabilities Port Mode (ECP). The HD (Active HIGH) input pin enables the Cable port to switch from Open Drain to a high drive totem pole output, capable of sourcing 14mA on all thirteen buffer and 84mA on PERI LOGIC OUTPUT buffer. The DIR input determines the direction of data flow on the bidirectional buffers. DIR (Active HIGH) enables data flow from A port to B port. DIR (Active LOW) enables data flow from B port to A port. It is available in the commercial temperature range.



ORDER CODES

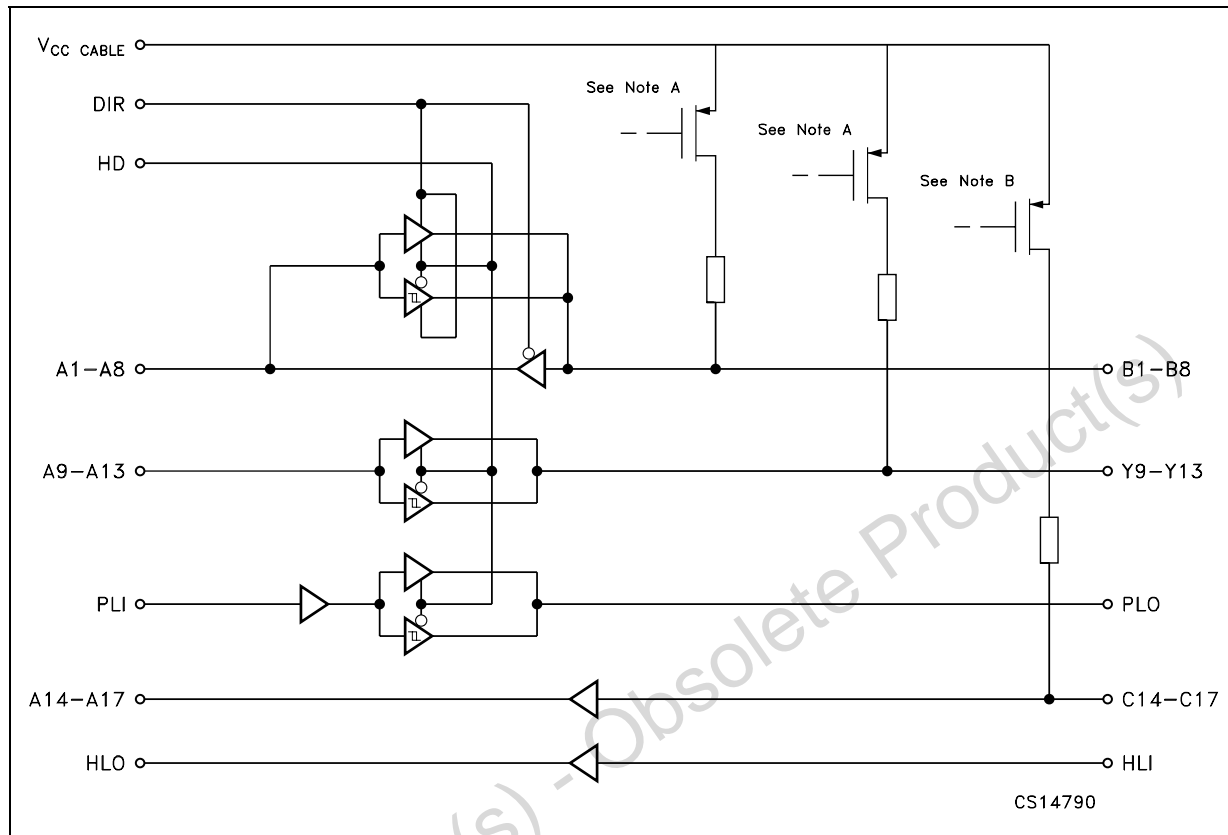
PACKAGE	TUBE	T & R
TSSOP		74LVC161284TTR

PIN CONNECTION

HD	1	48	DIR
A9	2	47	Y9
A10	3	46	Y10
A11	4	45	Y11
A12	5	44	Y12
A13	6	43	Y13
V _{CC}	7	42	V _{CC} /CABLE
A1	8	41	B1
A2	9	40	B2
GND	10	39	GND
A3	11	38	B3
A4	12	37	B4
A5	13	36	B5
A6	14	35	B6
GND	15	34	GND
A7	16	33	B7
A8	17	32	B8
V _{CC}	18	31	V _{CC} /CABLE
PLI	19	30	PLO
A14	20	29	C14
A15	21	28	C15
A16	22	27	C16
A17	23	26	C17
HLO	24	25	HLI

CS14380

LOGIC DIAGRAM



NOTE A: The PMOS transistors prevent backdriving current from the signal pins to $V_{CC/CABLE}$ when $V_{CC/CABLE}$ is open or at GND. The PMOS transistor is turned off when the associated driver is in the low state.

NOTE B: The PMOS transistor prevents backdriving current from the signal pins to $V_{CC/CABLE}$ when $V_{CC/CABLE}$ is open or at GND.

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	HD	High Drive Enable Input
2, 3, 4, 5, 6	A9 to A13	Side A Input
8, 9, 11, 12, 13, 14, 16, 17	A1 to A8	Side A Input or Output
19	PLI	Peripheral Logic Input
20, 21, 22, 23	A14 to A17	Side A Output
24	HLO	Host Logic Output
25	HLI	Host Logic Input
29, 28, 27, 26	C14 to C17	Side Cable Output
30	PLO	Peripheral Logic Output
41, 40, 38, 37, 36, 35, 33, 32	B1 to B8	Side Cable Input or Output
47, 46, 45, 44, 43	Y9 to Y13	Side Cable Output
48	DIR	Direction Control Input
10, 15, 34, 39	GND	Ground (0V)
7, 18	V_{CC}	Positive Supply Voltage
31, 42	$V_{CC/CABLE}$	Cable Power Supply

TRUTH TABLE

INPUT		OUTPUT	OUTPUT
DIR	HD		
L	L	B1-B8 Data to A1-A8 A9-A13 Data to Y9-Y13 C14-C17 Data to C14-C17	Y9-Y13 and PLO Open Drain
L	H		Y9-Y13 and PLO Totem Pole
H	L	A1-A8 Data to B1-B8 A9-A13 Data to Y9-Y13 C14-C17 Data to C14-C17	B1-B8 Y9-Y13 and PLO Open Drain
H	H		B1-B8 Y9-Y13 and PLO Totem Pole

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	-0.5 to +4.6	V	
$V_{CCcable}$	Cable Supply Voltage (must be $\geq V_{CC}$)	-0.5 to +7.0	V	
V_{IA}	DC Input Voltage A1-A13, PL_{IN} , DIR, HD_{IN}	-0.5 to $+V_{CC} + 0.5$	V	
V_{IB}	DC Input Voltage B1-B8, C14-C17, HL_{IN}	-0.5 to +5.5	V	
V_{IBp}	DC Input Voltage B1-B8, C14-C17, HL_{IN} (40ns transient)	-2 to +7	V	
V_{OA}	DC Output Voltage A1-A8, A14-A17, HL_{IN}	-0.5 to $+V_{CC} + 0.5$	V	
V_{OB}	DC Output Voltage B1-B8, Y9-Y13, PL_{IN}	-0.5 to +5.5	V	
V_{OBp}	DC Output Voltage B1-B8, Y9-Y13, PL_{IN} (40ns transient)	-2 to +7	V	
I_{IK}	DC Input Diode Current DIR, HD A9-A13, PL_{IN} C14-C17	- 20	mA	
I_{OK}	DC Output Diode Current	A1-A8, A14-A17, HL_{IN}	± 50	mA
		B1-B8, Y9-Y13, PL_{IN}	- 50	
I_O	DC Output Current	A1-A8, HL_{IN}	± 25	mA
		B1-B8, Y9-Y13	± 50	
		$PL_O = \text{LOW}$	84	
		$PL_O = \text{HIGH}$	-50	
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin	± 200	mA	
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$	
T_L	Lead Temperature (10 sec)	300	$^{\circ}\text{C}$	

Absolute Maximum Rating are those value beyond which damage to the device may occur. Functional operation under these condition is not implied

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	3.0 to 3.6	V
$V_{CCcable}$	Cable Supply Voltage	3.0 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Open Drain Output Voltage	0 to 5.5	V
T_{op}	Operating Temperature	-40 to 85	$^{\circ}\text{C}$

DC SPECIFICATIONS

Symbol	Parameter		Test Condition			Value		Unit
			V _{CC} (V)	V _{CCcable} (V)		-40 to 85 °C		
						Min.	Max.	
V _{IH}	High Level Input Voltage	An, Bn, PL _{IN} , DIR, HD	3.0 to 3.6	3.0 to 5.5		2		V
		Cn				2.3		
		HL _{IN}				2.6		
V _{IL}	Low Level Input Voltage	An, Bn, PL _{IN} , DIR, HD	3.0 to 3.6	3.0 to 5.5			0.8	V
		Cn					0.8	
		HL _{IN}					1.6	
V _{OH}	High Level Output Voltage	An, HL	3.0	3.0	I _O =-50μA	2.8		V
			3.0	3.0	I _O =-4mA	2.4		
		Bn, Yn	3.0	3.0	I _O =-14mA	2.0		
		Bn, Yn	3.0	4.5	I _O =-14mA	2.23		
		PL	3.15	3.15	I _O =-500μA	3.1		
V _{OL}	Low Level Output Voltage	An, HL	3.0	3.0	I _O =50μA		0.2	V
			3.0	3.0	I _O =4mA		0.4	
		Bn, Yn	3.0	3.0	I _O =14mA		0.8	
		Bn, Yn	3.0	4.5	I _O =14mA		0.77	
		PL	3.0	3.0	I _O =84mA		0.95	
		PL	3.0	4.5	I _O =84mA		0.90	
I _I	Input Current	Cn	3.6	3.6	V _I = V _{CC}		50	μA
			3.6	3.6	V _I =GND (Pull-up res)		-3.5	mA
		All input except B or C	3.6	5.0	V _I = V _{CC} or GND		± 1	μA
I _{CC}	Quiescent Supply Current		3.6	5.0	V _I = V _{CC} I _O =0		0.8	mA
					V _I =GND (12xPull-up)		45	
I _{OZ}	High Impedance Output Leakage Current	Bn	3.6	5.0	V _O = V _{CC}		20	μA
			3.6	3.6	V _O =GND (Pull-up res)		-3.5	mA
		A1-A8	3.6	5.0	V _O = V _{CC} or GND		± 20	μA
		Open Drain Y Output	3.6	3.6	V _O =GND (Pull-up res)		-3.5	mA
I _{OFF}	Power Off Leakage Current	B, Y output (to GND)	0	5.0	V _I or V _O = 0 to 7V		100	μA
		B, Y output (to V _{CC})	0	5.0	V _I or V _O = 0 to 7V		10	μA
V _{hys}	Input Hysteresis	An, Bn, PL _{IN} , DIR, HD	3.3	5.0		0.4		V
		Cn	3.3	5.0		0.8		
		HL _{IN}	3.3	5.0		0.2		
Z _O	Output Impedance	B1-B8, Y9-Y13	3.3	5.0	V _B = V _{OH}	30	55	Ω
R _P	Pull-up Resistance	B1-B8, Y9-Y13, C14-C17	3.3	5.0	V _B = V _{OH}	1150	1650	Ω

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Condition			Value		Unit
			V _{CC} (V)	V _{CCcable} (V)		-40 to 85 °C		
						Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	A1-A8 to B1-B8, A9-A13 to Y9-Y13	3.0 to 3.6	3.0 to 5.5	R _L =500Ω C _L =50pF	1	7.5	ns
		B1-B8 to A1-A8, C14-C17 to A14-A17			R _L =500Ω C _L =50pF	1	9.0	ns
		PL _{IN} to PL _{OUT}			R _L =500Ω C _L =50pF	1	7.0	ns
		HL _{IN} to HL _{OUT}			R _L =500Ω C _L =50pF	1	11.0	ns
t _{PZH} t _{PZL}	Enable Delay Time	DIR to A	3.0 to 3.6	3.0 to 5.5	R _L =500Ω C _L =50pF	1	12	ns
		HD to Bn, Y9-Y13			R _L =500Ω C _L =50pF	1	8.5	ns
t _{PLZ} t _{PHZ}	Disable Delay Time	DIR to A	3.0 to 3.6	3.0 to 5.5	R _L =500Ω C _L =50pF	1	8.5	ns
		DIR to A			R _L =500Ω C _L =50pF	1	8.5	ns
		HD to Bn, Y9-Y13			R _L =500Ω C _L =50pF	1	8.5	ns
t _r t _f	Rise and Fall Time B1-B8, Y9-Y13 Open Drain		3.0 to 3.6	3.0 to 5.5	R _L =500Ω C _L =50pF	1	120	ns
t _{OSLH} t _{OSHL}	Output To Output Skew Time (note1, 2)		3.0 to 3.6	3.0 to 5.5	R _{PULL-UP} =500Ω C _L =50pF	1	2	ns

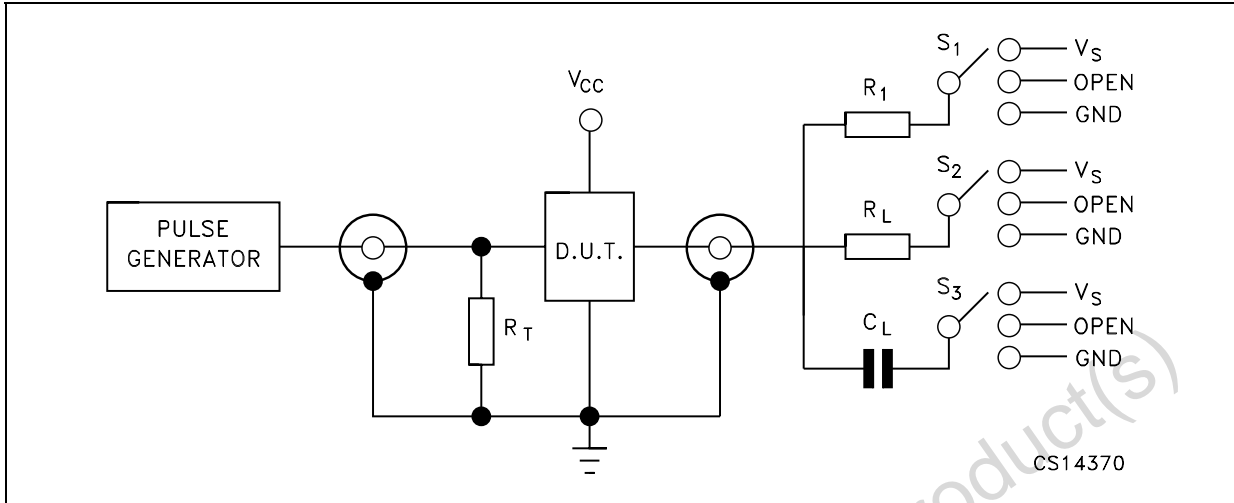
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)

2) Parameter guaranteed by design

CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V _{CC} (V)	V _{CC/CABLE} (V)	T _A = 25 °C			
				Min.	Typ.	Max.	
C _{IN}	Control Input Capacitance (HD, DIR, A9-A13, C14-C17, PL _{IN} , HL _{IN})	Open	Open		4		pF
C _{I/O}	I/O Pin Capacitance	3.3	5.0		6		pF

TEST CIRCUIT



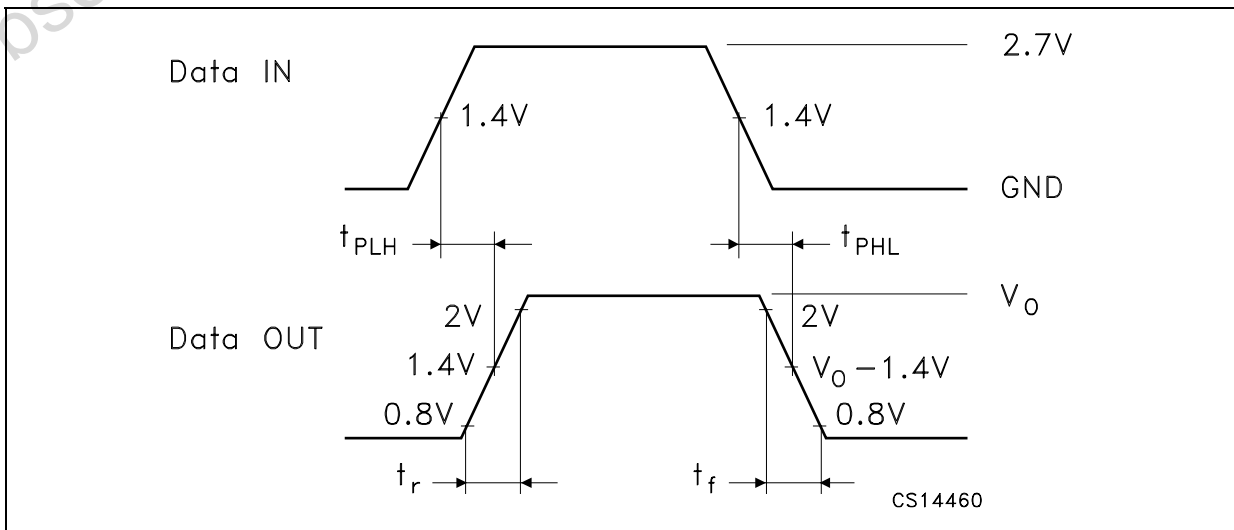
TEST	S1	S2	S3
t_{PHL} (A1-A8 to B1-B8, A9-A13 to Y9-Y13, PLH _{IN} to PLH) (see waveform 1)	Open	V _{CC}	V _{CC}
t_{PLH} (A1-A8 to B1-B8, A9-A13 to Y9-Y13, PLH _{IN} to PLH, HD to B1-B8, Y9-Y13, PLH) (see waveform 1)	Open	GND	GND
t_{PHL} , t_{PLH} (B1-B8 to A1-A8, C14-C17 to A14-A17, HLH _{IN} to HLH) (see waveform 2)	Open	GND	GND
t_r , t_f (A1-A8 to B1-B8, A9-A13 to Y9-Y13) (see waveform 1)	Open	V _{CC}	GND
t_{PLZ} (DIR to A1-A8) (see waveform 4)	6V	GND	GND
t_{PHZ} (DIR to A1-A8) (see waveform 4)	Open	GND	GND
t_{PZL} (DIR to A1-A8) (see waveform 3)	1.4V	GND	GND
t_{PZH} (DIR to A1-A8) (see waveform 3)	4.4V	GND	GND
t_{PLZ} (DIR to B1-B8) (see waveform 4)	6V	GND	GND
t_{PHZ} (DIR to B1-B8) (see waveform 4)	Open	GND	GND

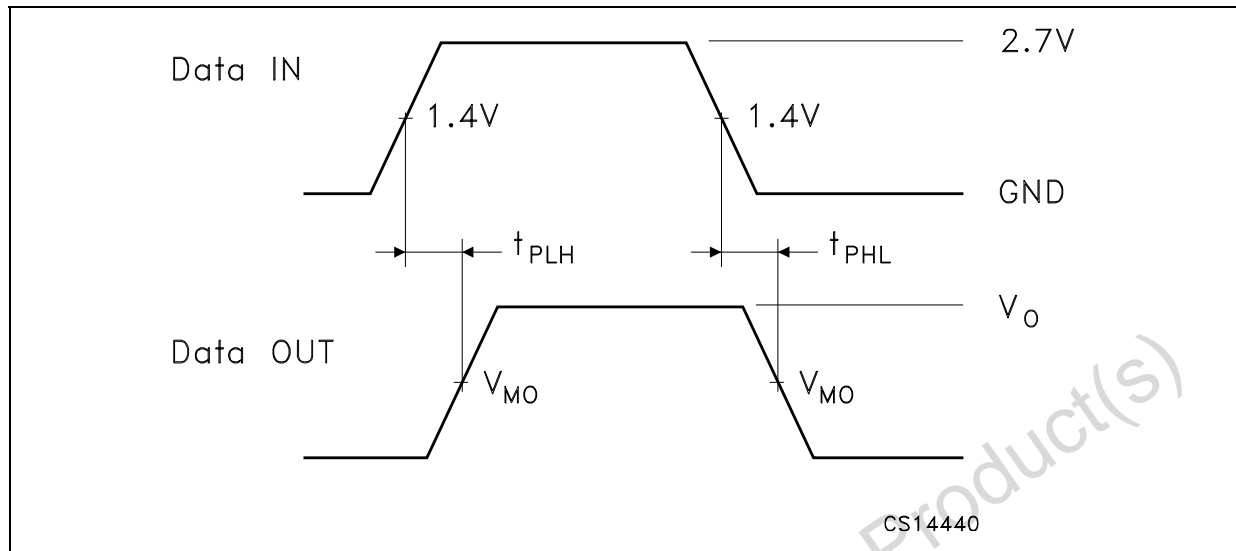
C_L = 50 pF or equivalent (includes jig and probe capacitance)

R_L = R_1 = 500Ω or equivalent

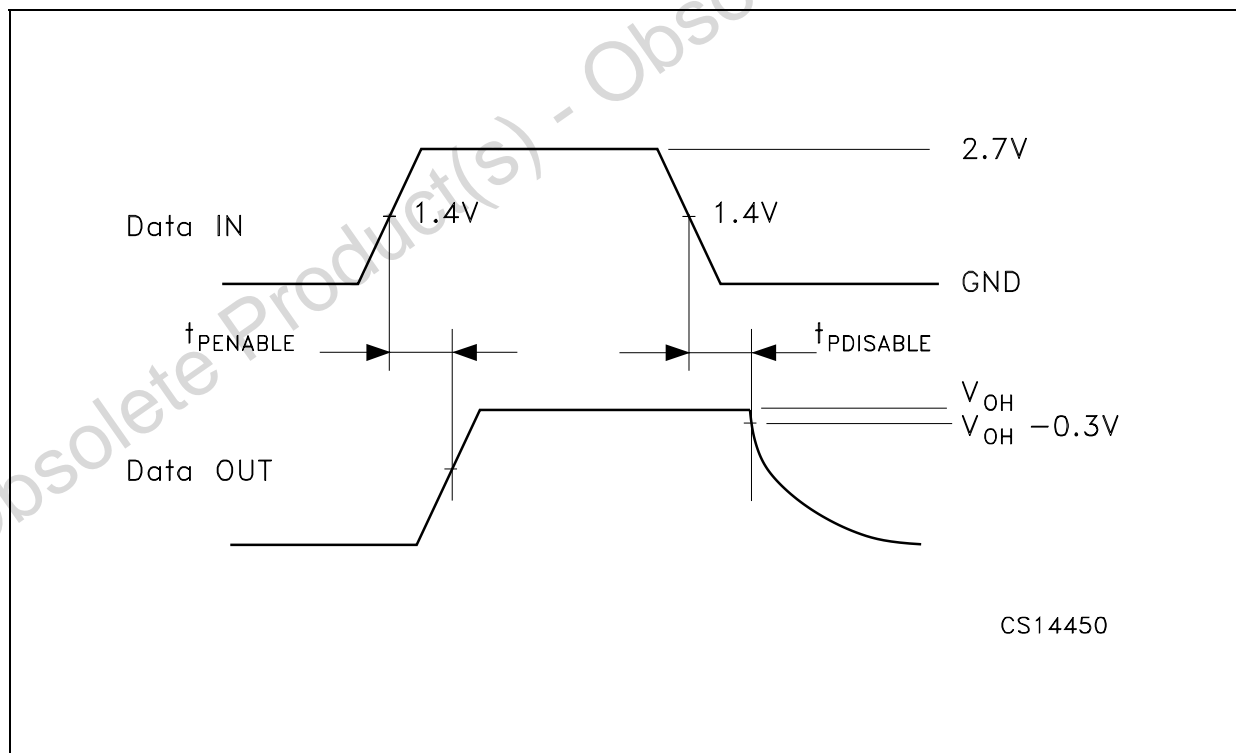
R_T = Z_{OUT} of pulse generator (typically 50Ω)

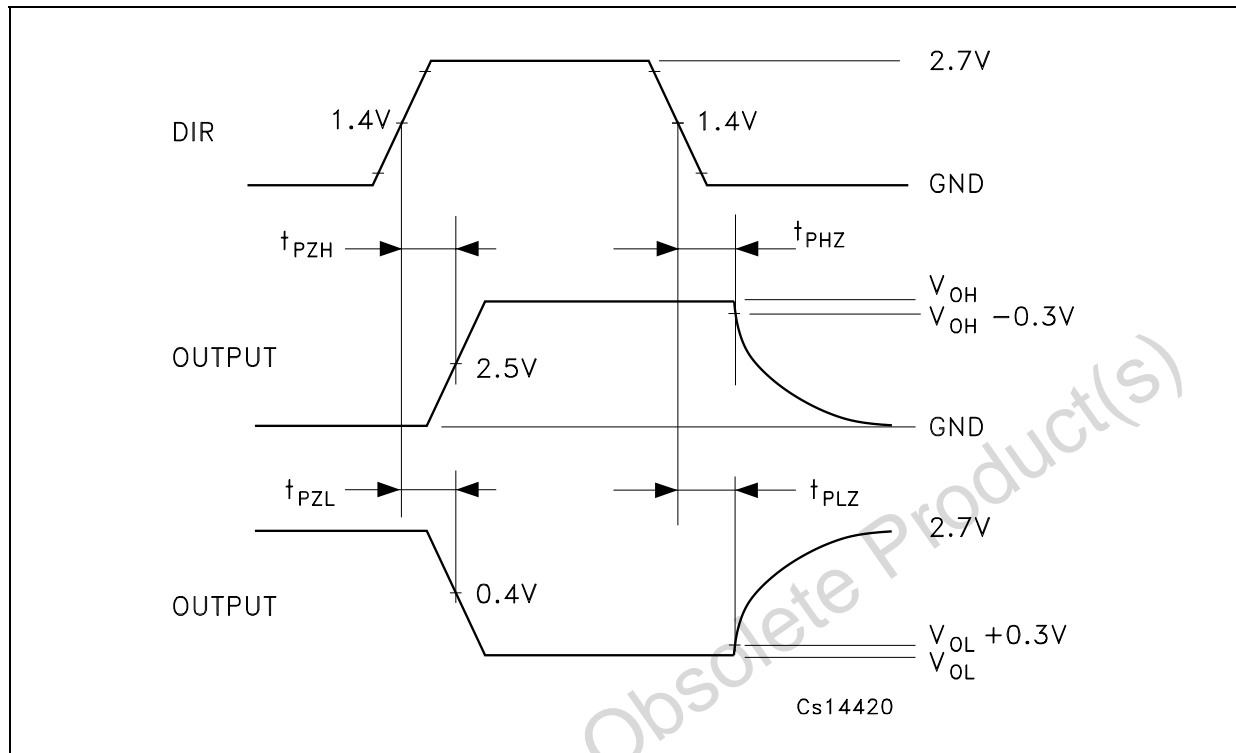
WAVEFORM 1: PROPAGATION DELAY INPUT An TO OUTPUT (f=1MHz; 50% duty cycle)



WAVEFORM 2: PROPAGATION DELAY INPUT Bn TO OUTPUT (f=1MHz; 50% duty cycle)

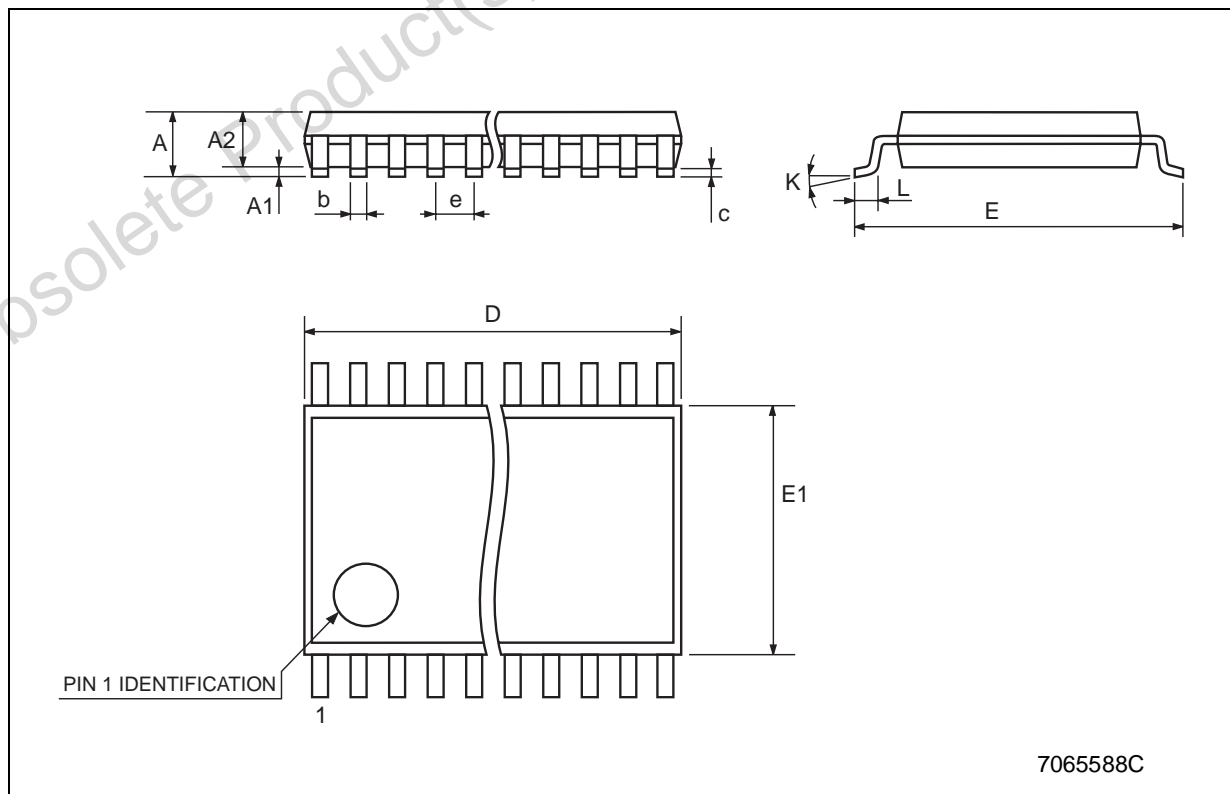
$V_{MO} = 50\%V_{CC}$

WAVEFORM 3: DATA TO OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

WAVEFORM 4: DIR TO OUTPUT ENABLE AND DISABLE TIME ($f=1\text{MHz}$; 50% duty cycle)

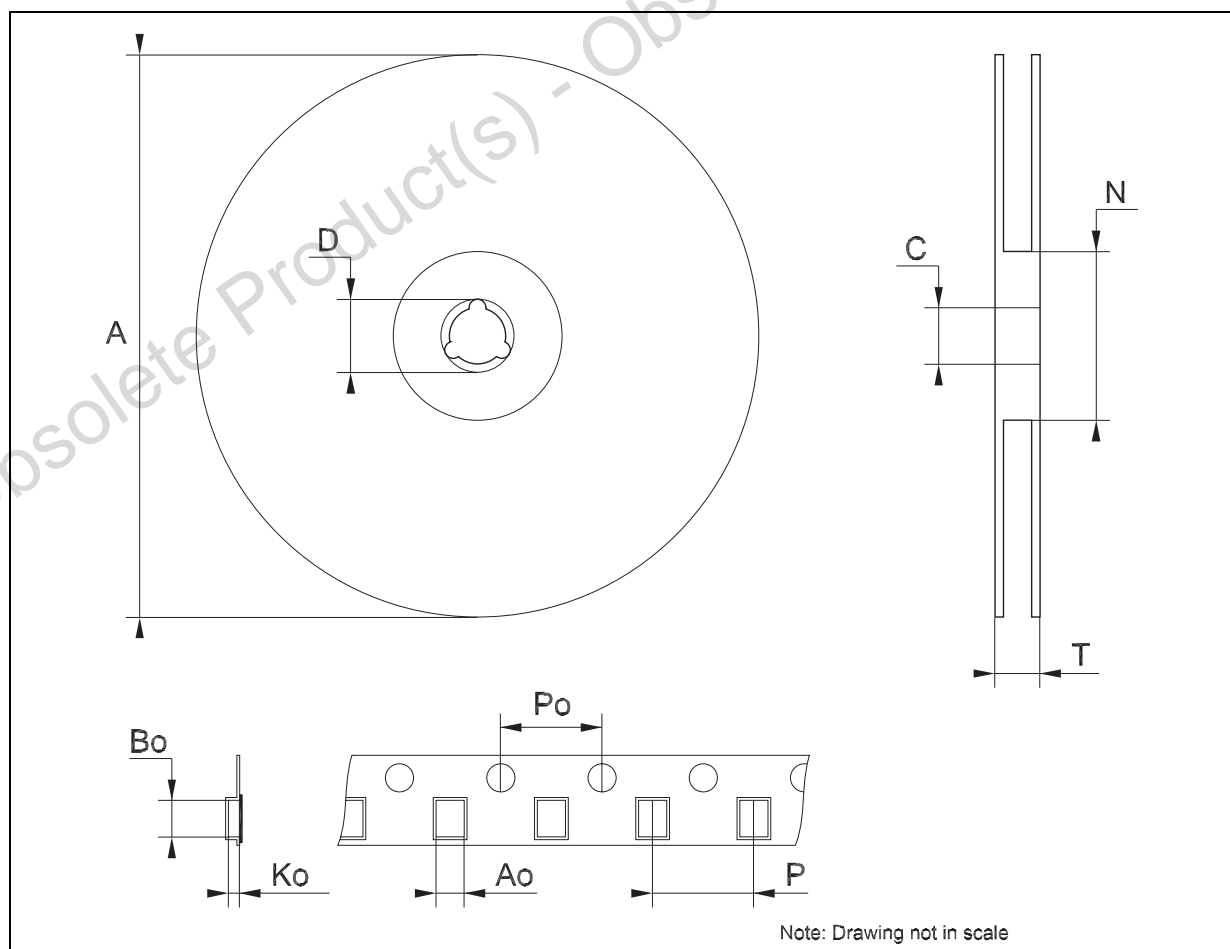
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Obsolete Product(s) - Obsolete Product(s)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>