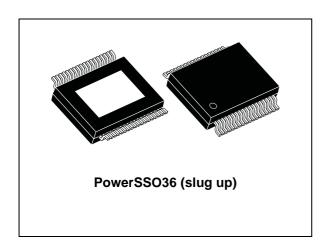


## 40 V, 3.5 A quad power half bridge

Datasheet - production data



#### **Features**

- Multipower BCD technology
- Minimum input output pulse width distortion
- 200 m $\Omega$  R<sub>dsON</sub> complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- Thermal warning output
- Undervoltage protection
- · Short-circuit protection

### **Description**

STA518 is a monolithic quad half bridge stage in multipower BCD technology. The device can be used also as dual bridge or reconfigured, by connecting CONFIG pin to  $V_{\rm dd}$  pin, as single bridge with double current capability.

The device is particularly designed to make the output stage of a stereo all-digital high efficiency (DDX<sup>TM</sup>) amplifier capable to deliver an output power of 24 W x 4 channels @ THD = 10% at  $V_{CC}$  30 V on 4 W load in single ended configuration.

It can also deliver 50 + 50 W @ THD = 10% at  $V_{CC}$  29 V as output power on 8 W load in BTL configuration and 70 W @ THD = 10% at  $V_{CC}$  34 V on 8 W in single paralleled BTL configuration.

The input pins have threshold proportional to V<sub>L</sub> pin voltage.

**Table 1. Device summary** 

Order code	Temperature range °C	Package	Packaging
STA51813TR	-40 to 90	PowerSSO36 (slug up)	Tape & reel

Contents STA518

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## 1 Audio application circuit

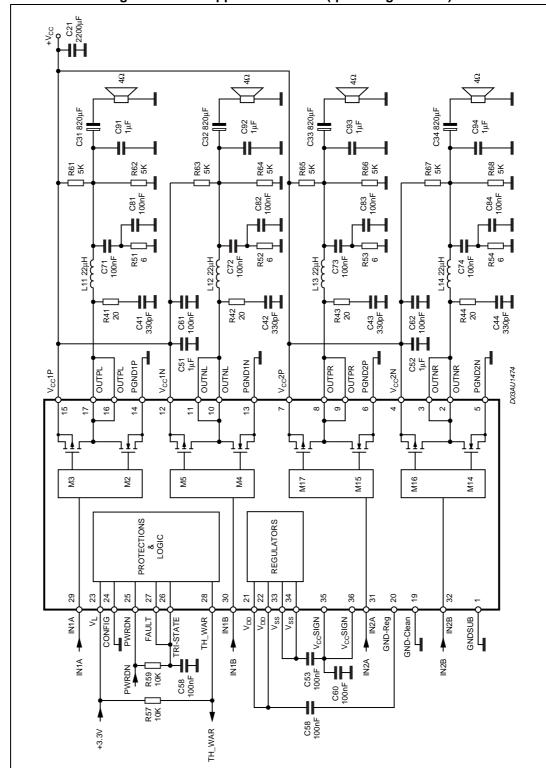


Figure 1. Audio application circuit (quad single ended)

Pins description STA518

## 2 Pins description

0 V<sub>CC</sub>Sign [ 36 1 ] GND-SUB V<sub>CC</sub>Sign [ 2 35 OUT2B 34 3 OUT2B V<sub>SS</sub> [ 4  $V_{SS}$ 33 V<sub>CC</sub>2B GND2B IN2B 32 5 GND2A IN2A 31 6 IN1B 30 7 J V<sub>CC</sub>2A IN1A 29 8 OUT2A TH\_WAR 28 9 OUT2A FAULT [ 27 10 OUT1B 26 TRI-STATE [ 11 OUT1B 25 PWRDN [ 12  $V_{CC}1B$ 24 CONFIG [ 13 ☐ GND1B 23 14 GND1A VL 22 15 ☐ V<sub>CC</sub>1A V<sub>DD</sub> 16 OUT1A 21  $V_{DD}$ 20 OUT1A GND-Reg 17 19 18 □ N.C. GND-Clean D01AU1273

Figure 2. Pin connection (top view)

**Table 2. Pin function** 

Pin n°	Name	Description
1	GND-SUB	Substrate ground
2, 3	OUT2B	Output half bridge 2B
4	Vcc2B	Positive supply
5	GND2B	Negative supply
6	GND2A	Negative supply
7	Vcc2A	Positive supply
8, 9	OUT2A	Output half bridge 2A
10, 11	OUT1B	Output half bridge 1B
12	Vcc1B	Positive supply
13	GND1B	Negative supply
14	GND1A	Negative supply
15	Vcc1A	Positive supply
16, 17	OUT1A	Output half bridge 1A
18	NC	Not connected

STA518 Pins description

Table 2. Pin function (continued)

Pin n°	Name	Description
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator V <sub>dd</sub>
21, 22	$V_{dd}$	5 V regulator referred to ground
23	$V_{L}$	Logic reference voltage
24	CONFIG	Configuration pin
25	PWRDN	Short-circuit pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
33, 34	V <sub>ss</sub>	5 V regulator referred to +V <sub>CC</sub>
35, 36	V <sub>CC</sub> Sign	Signal positive supply

Table 3. Functional pin status

Pin name	Pin n°	Locical value	IC - STATUS
FAULT	27	0	Fault detected (short-circuit, or thermal)
FAULT *	27	1	Normal operation
TRI-STATE	26	0	All powers in Hi-Z state
TRI-STATE	26	1	Normal operation
PWRDN	25	0	Low consumption
PWRDN	25	1	Normal operation
THWAR	28	0	Temperature of the IC = 130 °C
THWAR (1)	28	1	Normal operation

<sup>1.</sup> The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC supply voltage (Pin 4, 7, 12, 15)	40	V
V <sub>max</sub>	Maximum voltage on pins 23 to 32	5.5	V
T <sub>op</sub>	Operating temperature range	-40 to 90	°C
P <sub>tot</sub>	Power dissipation (T <sub>case</sub> = 70 °C)	21	W
T <sub>stg</sub> , T <sub>j</sub>	Storage and junction temperature	-40 to 150	°C

### 3.2 Recommended operating conditions

Table 5. Recommended operating conditions (1)

Symbol	Parameter	Min.	Тур.	Max.	Unit
V <sub>CC</sub>	DC supply voltage	10		36.0	V
$V_{L}$	Input logic reference	2.7	3.3	5.0	V
T <sub>amb</sub>	Ambient temperature	0		70	ů

<sup>1.</sup> Performances not guaranteed beyond recommended operating conditions

#### 3.3 Thermal data

Table 6. Thermal data (1)

Symbol	Parameter	Min.	Тур.	Max.	Unit
T <sub>j-case</sub>	Thermal resistance junction to case (thermal pad)			1.5	°C/W
T <sub>jSD</sub>	Thermal shut-down junction temperature		150		°C
T <sub>warn</sub>	Thermal warning temperature		130		°C
t <sub>hSD</sub>	Thermal shut-down hysteresis		25		°C

<sup>1.</sup> See Thermal information

#### 3.4 Thermal information

The power dissipated within the device depends primarily on the supply voltage, load impedance and output modulation level. The PSSO36 package of the STA518 includes an exposed thermal slug on the top of the device to provide a direct thermal path from the IC to the heatsink. For the Quad single ended application the dissipated power vs. output power is shown in *Figure 10*.

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Considering that for the STA518 the thermal resistance junction to slug is 1.5 °C/W and the estimated thermal resistance due to the grease placed between slug and heat sink is 2.3 °C/W (the use of thermal pads for this package is not recommended), the suitable heat sink  $R_{th}$  to be used can be drawn from the following graph *Figure 11*, where is shown the derating power vs.  $t_{amb}$  for different heat sinks.

#### 3.5 Electrical characteristics

Refer to circuit in *Figure 3* ( $V_L = 3.3 \text{ V}$ ;  $V_{CC} = 30 \text{ V}$ ;  $R_L = 8 \Omega$ ;  $f_{sw} = 384 \text{ kHz}$ ;  $T_{amb} = 25 ^{\circ}\text{C}$  unless otherwise specified)

**Table 7. Electrical characteristics** 

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
R <sub>dsON</sub>	Power P-channel / N-channel MOSFET R <sub>dsON</sub>	I <sub>d</sub> = 1A		200	270	mΩ
I <sub>dss</sub>	Power P-channel / N-channel leakage I <sub>dss</sub>	V <sub>CC</sub> = 35V			50	μA
9 <sub>N</sub>	Power P-channel R <sub>dsON</sub> Matching	I <sub>d</sub> = 1A	95			%
ЯР	Power N-channel R <sub>dsON</sub> Matching	I <sub>d</sub> = 1A	95			%
Dt_s	Low current dead time (static)	see test circuit Figure 3		10	20	ns
Dt_d	High current dead time (dynamic)	$L = 22\mu H; C = 470nF; R_L = 8 \Omega$ $I_d = 3A; see Figure 5$			50	ns
t <sub>d ON</sub>	Turn-on delay time	Resistive load; V <sub>CC</sub> = 30V			100	ns
t <sub>d OFF</sub>	Turn-off delay time	Resistive load; V <sub>CC</sub> = 30V			100	ns
t <sub>r</sub>	Rise time	Decistive leads on Figure 2			25	ns
t <sub>f</sub>	Fall time	Resistive load; as Figure 3			25	ns
V <sub>CC</sub>	Supply voltage operating voltage		10		36	V
V <sub>IN-H</sub>	High level input voltage				V <sub>L</sub> /2 +300mV	V
V <sub>IN-L</sub>	Low level input voltage		V <sub>L</sub> /2 - 300mV			V
I <sub>IN-H</sub>	Hi level input current	Pin voltage = V <sub>L</sub>		1		μΑ
I <sub>IN-L</sub>	Low level input current	Pin voltage = 0.3V		1		μΑ
I <sub>PWRDN</sub> -	Hi level PWRDN pin input current	V <sub>L</sub> = 3.3V		35		μА
V <sub>LOW</sub>	Low logical state voltage V <sub>LOW</sub> (pin PWRDN, TRISTATE) <sup>(1)</sup>	V <sub>L</sub> = 3.3V	0.8			V
V <sub>HIGH</sub>	High logical state voltage V <sub>HIGH</sub> (pin PWRDN, TRISTATE) <sup>(1)</sup>	V <sub>L</sub> = 3.3V			1.7	V
I <sub>VCC</sub> -	Supply current from $V_{CC}$ in power down	PWRDN = 0			3	mA



Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>FAULT</sub>	Output current pins FAULT -TH-WARN when FAULT CONDITIONS	V <sub>pin</sub> = 3.3V		1		mA
I <sub>VCC-hiz</sub>	Supply current from V <sub>CC</sub> in Tristate	V <sub>CC</sub> = 30V; Tri-state = 0		22		mA
I <sub>VCC</sub>	Supply current from V <sub>CC</sub> in operation (both channel switching)	V <sub>CC</sub> = 30V; Input pulse width = 50% Duty; Switching Frequency = 384kHz; No LC filters;		50		mA
I <sub>VCC-q</sub>	I <sub>sc</sub> (short-circuit current limit) (2)	V <sub>CC</sub> = 30V	3.5	6		Α
V <sub>UV</sub>	Undervoltage protection threshold			7		V
t <sub>pw_min</sub>	Output minimum pulse width	No Load	70		150	ns

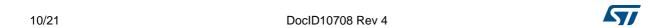
<sup>1.</sup> The Table 8 explains the  $\rm V_{LOW},\, \rm V_{HIGH}$  variation with  $\rm I_{bias}.$ 

Table 8.  $V_{LOW}$ ,  $V_{HIGH}$  variation with  $I_{bias}$ 

V <sub>L</sub>	V <sub>Low min</sub>	V <sub>High max</sub>	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Table 9. Logic truth table (see Figure 4)

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	Output mode
0	Х	Х	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used



<sup>2.</sup> See relevant Application Note AN1994

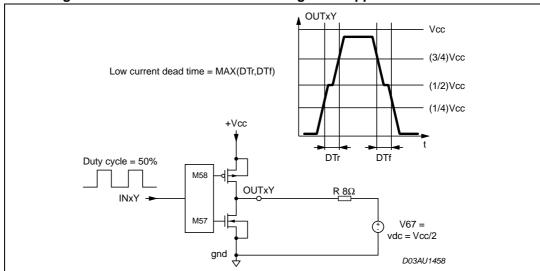


Figure 3. Low current dead time for single end application: test circuit.

Figure 4. High current dead time for bridge application: block diagram

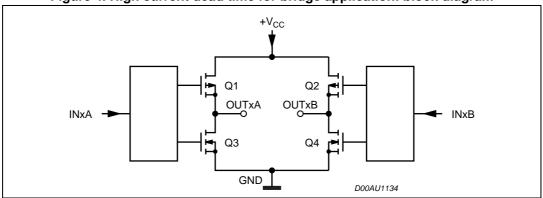
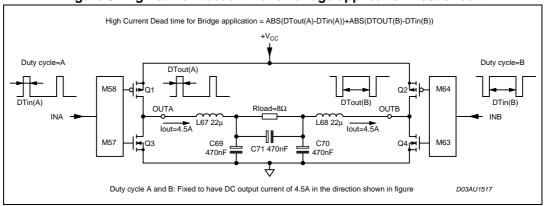


Figure 5. High current dead time for bridge application: test circuit



Technical information STA518

#### 4 Technical information

The STA518 is a dual channel H-Bridge that is able to deliver 50 W per channel (@ THD = 10%  $R_L$  = 8  $\Omega$ ,  $V_{CC}$  = 29 V) of audio output power in high efficiency.

The STA518 converts both DDX and binary-controlled PWM signals into audio power at the load. It includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs and thermal and short-circuit protection circuitry.

In DDX mode, two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to the damped ternary modulation operation.

In binary mode operation, both full bridge and half bridge modes are supported. The STA518 includes over-current and thermal protection as well as an undervoltage lockout with automatic recovery. A thermal warning status is also provided.

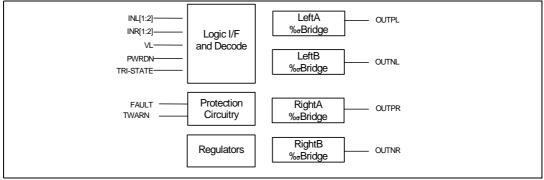
INL[1:2] OUTPL INR[1:2] I eft Logic I/F VL · H-Bridge and Decode **PWRDN** OUTNL TRI-STATE Protection FAULT OUTPR Circuitry **TWARN** Right H-Bridge

OUTNR

Figure 6. STA518 block diagram full-bridge DDX® or binary modes

Figure 7. STA518 block diagram binary half-bridge mode

Regulators



## 4.1 Logic interface and decode

The STA518 power outputs are controlled using one or two logic level timing signals. In order to provide a proper logic interface, the  $V_{\text{bias}}$  input must operate at the same voltage as the DDX control logic supply.

Protection circuitry:

The STA518 includes protection circuitry for over-current and thermal overload conditions. A thermal warning pin (pin. 28) is activated low (open drain MOSFET) when the IC

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STA518 Technical information

temperature exceeds 130 °C, in advance of the thermal shutdown protection. When a fault condition is detected, an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-Bridges in high impedance state. At the same time an open-drain MOSFET connected to the fault pin (pin.27) is switched on.

There are two possible modes subsequent to activating a fault:

- 1. **SHUTDOWN mode**: with FAULT (pull-up resistor) and TRI-STATE pins independent, an activated fault will disable the device, signaling low at the FAULT output. The device may subsequently be reset to normal operation by toggling the TRI-STATE pin from high to low to high using an external logic signal.
- 2. **AUTOMATIC recovery mode:** This is shown in the audio application circuit of quad single ended). The FAULT and TRI-STATE pins are shorted together and connected to a time constant circuit comprising R59 and C58.

An activated FAULT will force a reset on the TRI-STATE pin causing normal operation to resume following a delay determined by the time constant of the circuit.

If the fault condition is still present, the circuit operation will continue repeating until the fault condition is removed.

An increase in the time constant of the circuit will produce a longer recovery interval. Care must be taken in the overall system design as not to exceed the protection thresholds under normal operation.

### 4.2 Power outputs

The STA518 power and output pins are duplicated to provide a low impedance path for the device's bridged outputs. All duplicate power, ground and output pins must be connected for proper operation.

The PWRDN or TRI-STATE pins should be used to set all MOSFETS to the Hi-Z state during power-up until the logic power supply,  $V_L$ , is settled.

### 4.3 Parallel output / high current operation

When using DDX mode output, the STA518 outputs can be connected in parallel in order to increase the output current capability to a load. In this configuration the STA518 can provide 70 W into 8 ohm.

This mode of operation is enabled with the CONFIG pin, the (pin 24) connected to VREG1 and the inputs combined INLA=INLB, INRA=INRB and the outputs combined OUTLA=OTLB, OUTRA=OUTRB.

#### 4.4 Additional information

Output Filter: A passive 2<sup>nd</sup> order passive filter is used on the STA518 power outputs to reconstruct an analog audio signal. System performance can be significantly affected by the output filter design and choice of passive components. A filter design for 6 ohm / 8 ohm loads is shown in the typical application circuit of *Figure 9*.

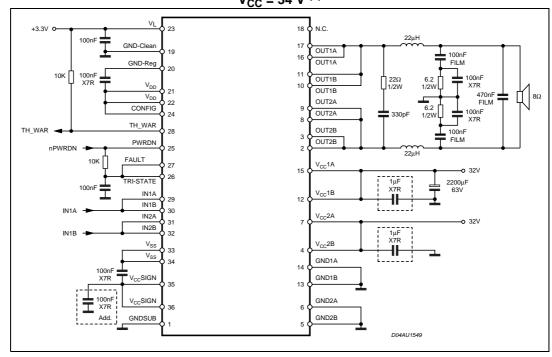
Quad single ended circuit (Figure 1) shows a filter for ½ bridge mode, 4 ohm loads.

Technical information STA518

+V<sub>CC</sub> C55 1000μF L18 22μH OUT1A 16 CONFIG 24 OUT1A PWRDN 25 M2 GND1A PROTECTIONS 27 R100 6 & LOGIC 8Ω 12 C31 1µF M5 OUT1B 10 IN1B M4 V<sub>DD</sub> 21 V<sub>DD</sub> 22 V<sub>SS</sub> 33 REGULATORS C32 1μF M17 L113 22μH C110 100nF OUT2A M15 GND2A C107 100nF IN2A GND-Reg R102 6 C33 1μF M16 OUT2B OUT2B M14 GND2E

Figure 8. Typical stereo full bridge configuration to obtain 50 + 50 W @ THD = 10%, R\_{L} = 8  $\Omega$ , V<sub>CC</sub> = 29 V

Figure 9. Typical single BTL configuration to obtain 70 W @ THD 10%, R<sub>L</sub> = 8  $\Omega$ ,  $V_{CC}$  = 34 V <sup>(a)</sup>



a. A PWM modulator as driver is needed. In particular, this result is performed using the STA308 + STA518 + STA50X demo board". Peak Power for t ≤ 1sec.

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### 5 Characterizations curves

The following characterization are obtained using the quad single ended configuration (*Figure 1*) with STA308A controller.

Figure 10. Power dissipation vs. output power

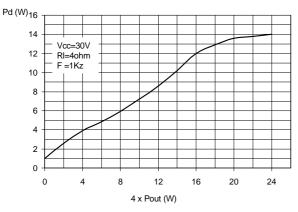


Figure 12. THD+N vs. output power

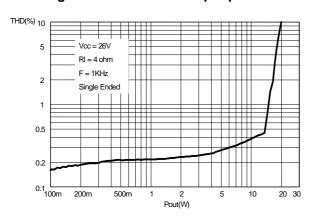


Figure 14. THD vs. frequency

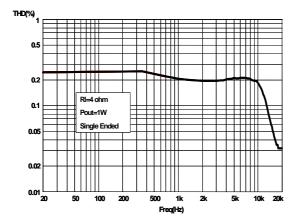


Figure 11. Power derating curve

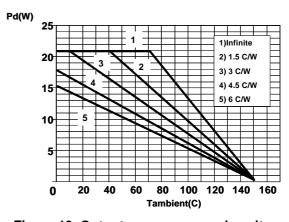
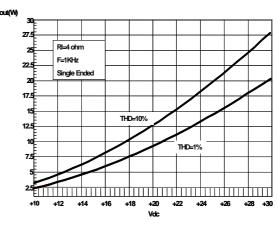


Figure 13. Output power vs. supply voltage

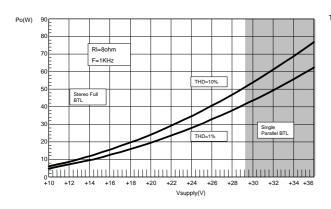


**Characterizations curves STA518** 

> The following characterizations are obtained using the stereo full bridge configuration (Figure 8) with STA308A controller.

Figure 15. Output power vs. supply voltage

Figure 16. THD+N vs. output power



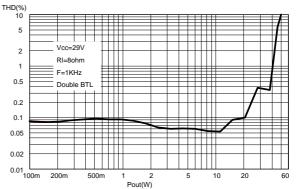
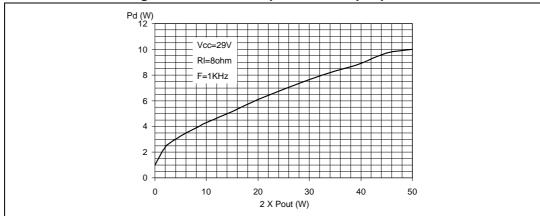


Figure 17. Power dissipation vs. output power



The following characterizations are obtained using the single BTL configuration (Figure 9) with STA308A controller.

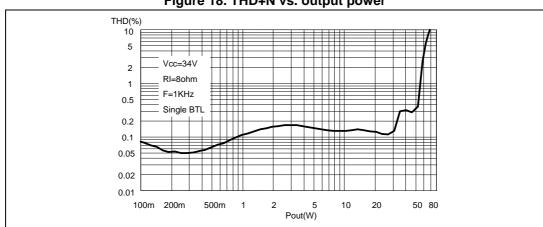


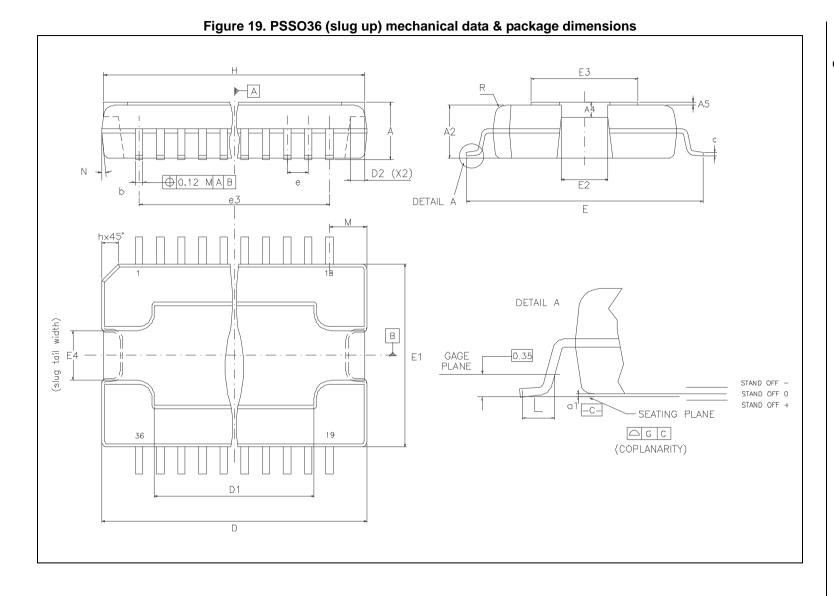
Figure 18. THD+N vs. output power

STA518 Package information

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: <a href="https://www.st.com">www.st.com</a>. ECOPACK<sup>®</sup> is an ST trademark.







STA518 Package information

Table 10. PowerSO36 exposed pad up dimensions

	Dimensions in mm.			Dimensions in inch.			
Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	
А	3.25	-	3.43	0.128	-	0.135	
A2	3.10	-	3.20	0.122	-	0.126	
A4	0.80	-	1.00	0.031	-	0.039	
A5	-	0.20	-	-	0.008	-	
a1	0.03	-	-0.04	0.001	-	-0.002	
b	0.22	-	0.38	0.009	-	0.015	
С	0.23	-	0.32	0.009	-	0.013	
D	15.80	-	16.00	0.622	-	0.630	
D1	9.40	-	9.80	0.370	-	0.386	
D2	-	1.00	-	-	0.039	-	
Е	13.90	-	14.50	0.547	-	0.571	
E1	10.90	-	11.10	0.429	-	0.437	
E2	-	-	2.90	-	-	0.114	
E3	5.80	-	6.20	0.228	-	0.244	
E4	2.90	-	3.20	0.114	-	0.126	
е	-	0.65	-	-	0.026	-	
e3	-	11.05	-	-	0.435	-	
G	0	-	0.08	0	-	0.003	
Н	15.50	-	15.90	0.610	-	0.626	
h	-	-	1.10	-	-	0.043	
L	0.80	-	1.10	0.031	-	0.043	
М	2.25	-	2.60	0.089	-	0.102	
N	-	-	10 degrees	-	-	10 degrees	
R	-	0.6	-	-	0.024	-	
s	-	-	8 degrees	-	-	8 degrees	

Revision history STA518

# 7 Revision history

**Table 11. Document revision history** 

Date	Revision	Changes
19-Aug-2004	1	Initial release.
11-Nov-2004	2	Changed symbol in "Electrical Characteristics".
18-May-2006	3	Changed operating temperature range value to -40 to 90°C (see <i>Table 4</i> ).
26-Feb-2014	4	Updated order code Table 1 on page 1

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