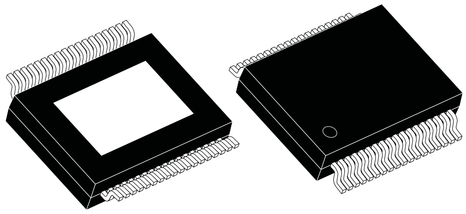
40 V, 3.5 A quad power half bridge

Datasheet - production data



PowerSSO36 (slug up)

Features

- Multipower BCD technology
- Minimum input output pulse width distortion
- 200 mΩ R_{dsON} complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- Thermal warning output
- Undervoltage protection
- Short-circuit protection

Description

STA518 is a monolithic quad half bridge stage in multipower BCD technology. The device can be used also as dual bridge or reconfigured, by connecting CONFIG pin to V_{dd} pin, as single bridge with double current capability.

The device is particularly designed to make the output stage of a stereo all-digital high efficiency (DDX™) amplifier capable to deliver an output power of 24 W x 4 channels @ THD = 10% at V_{CC} 30 V on 4 W load in single ended configuration.

It can also deliver 50 + 50 W @ THD = 10% at V_{CC} 29 V as output power on 8 W load in BTL configuration and 70 W @ THD = 10% at V_{CC} 34 V on 8 W in single paralleled BTL configuration.

The input pins have threshold proportional to V_L pin voltage.

Table 1. Device summary

Order code	Temperature range °C	Package	Packaging
STA51813TR	-40 to 90	PowerSSO36 (slug up)	Tape & reel

Contents

1 Audio application circuit 5

2 Pins description 6

3 Electrical specifications 8

3.1 Absolute maximum ratings 8

3.2 Recommended operating conditions 8

3.3 Thermal data 8

3.4 Thermal information 8

3.5 Electrical characteristics 9

4 Technical information 12

4.1 Logic interface and decode 12

4.2 Power outputs 13

4.3 Parallel output / high current operation 13

4.4 Additional information 13

5 Characterizations curves 15

6 Package information 17

7 Revision history 20

List of tables

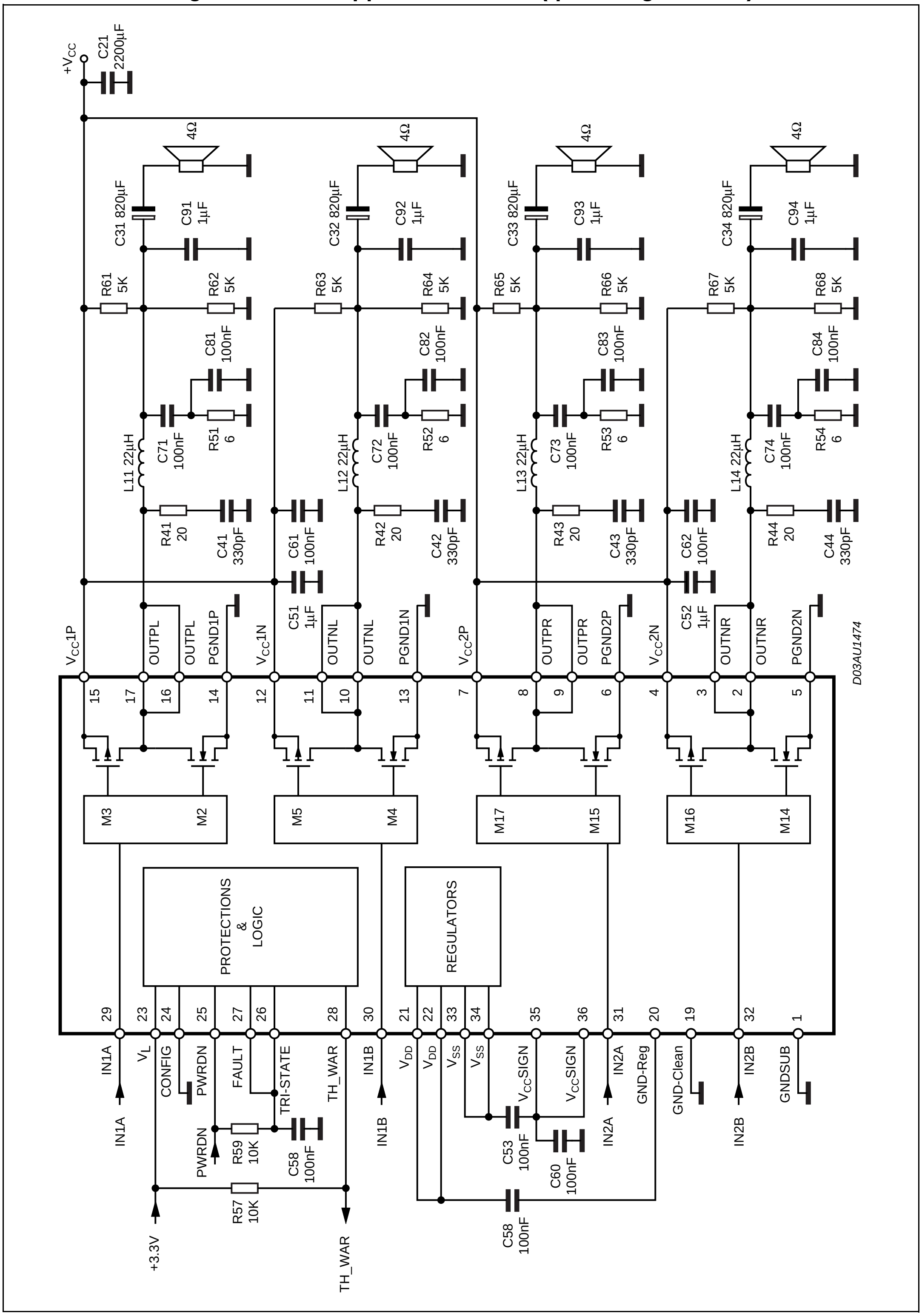
Table 1. Device summary 1
Table 2. Pin function 6
Table 3. Functional pin status 7
Table 4. Absolute maximum ratings 8
Table 5. Recommended operating conditions 8
Table 6. Thermal data 8
Table 7. Electrical characteristics 9
Table 8. V_{LOW}, V_{HIGH} variation with I_{bias} 10
Table 9. Logic truth table (see *Figure 4*) 10
Table 10. PowerSO36 exposed pad up dimensions 19
Table 11. Document revision history 20

List of figures

Figure 1. Audio application circuit (quad single ended) 5
Figure 2. Pin connection (top view) 6
Figure 3. Low current dead time for single end application: test circuit. 11
Figure 4. High current dead time for bridge application: block diagram. 11
Figure 5. High current dead time for bridge application: test circuit 11
Figure 6. STA518 block diagram full-bridge DDX® or binary modes. 12
Figure 7. STA518 block diagram binary half-bridge mode. 12
Figure 8. Typical stereo full bridge configuration to obtain 50 + 50 W @ THD = 10%, R_L = 8 W, V_{CC} = 29 V 14
Figure 9. Typical single BTL configuration to obtain 70 W @ THD 10%, R_L = 8 W, V_{CC} = 34 V . . . 14
Figure 10. Power dissipation vs. output power 15
Figure 11. Power derating curve 15
Figure 12. THD+N vs. output power 15
Figure 13. Output power vs. supply voltage 15
Figure 14. THD vs. frequency 15
Figure 15. Output power vs. supply voltage 16
Figure 16. THD+N vs. output power 16
Figure 17. Power dissipation vs. output power 16
Figure 18. THD+N vs. output power 16
Figure 19. PSSO36 (slug up) mechanical data & package dimensions 18

1 Audio application circuit

Figure 1. Audio application circuit (quad single ended)



2 Pins description

Figure 2. Pin connection (top view)

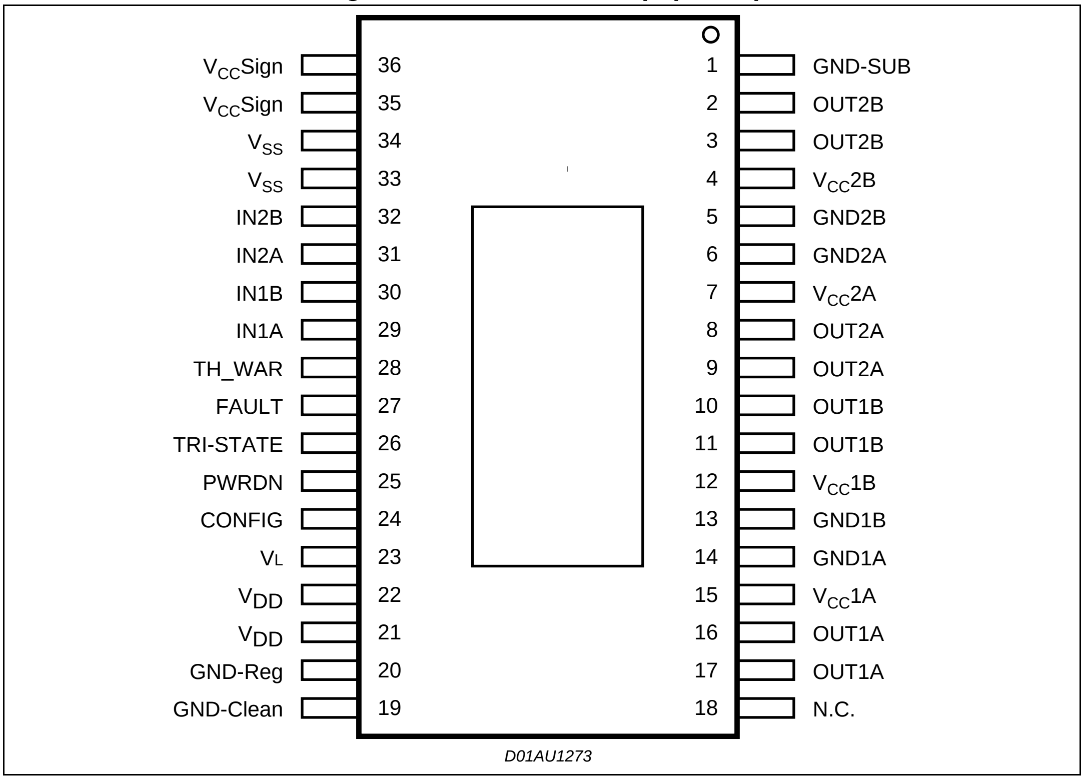


Table 2. Pin function

Pin n°	Name	Description
1	GND-SUB	Substrate ground
2, 3	OUT2B	Output half bridge 2B
4	Vcc2B	Positive supply
5	GND2B	Negative supply
6	GND2A	Negative supply
7	Vcc2A	Positive supply
8, 9	OUT2A	Output half bridge 2A
10, 11	OUT1B	Output half bridge 1B
12	Vcc1B	Positive supply
13	GND1B	Negative supply
14	GND1A	Negative supply
15	Vcc1A	Positive supply
16, 17	OUT1A	Output half bridge 1A
18	NC	Not connected

Table 2. Pin function (continued)

Pin n°	Name	Description
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator V_{dd}
21, 22	V_{dd}	5 V regulator referred to ground
23	V_L	Logic reference voltage
24	CONFIG	Configuration pin
25	PWRDN	Short-circuit pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half bridge 1A
30	IN1B	Input of half bridge 1B
31	IN2A	Input of half bridge 2A
32	IN2B	Input of half bridge 2B
33, 34	V_{ss}	5 V regulator referred to $+V_{CC}$
35, 36	V_{CC} Sign	Signal positive supply

Table 3. Functional pin status

Pin name	Pin n°	Locical value	IC - STATUS
FAULT	27	0	Fault detected (short-circuit, or thermal)
FAULT *	27	1	Normal operation
TRI-STATE	26	0	All powers in Hi-Z state
TRI-STATE	26	1	Normal operation
PWRDN	25	0	Low consumption
PWRDN	25	1	Normal operation
THWAR	28	0	Temperature of the IC = 130 °C
THWAR (1)	28	1	Normal operation

1. The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (Pin 4, 7, 12, 15)	40	V
V_{max}	Maximum voltage on pins 23 to 32	5.5	V
T_{op}	Operating temperature range	-40 to 90	°C
P_{tot}	Power dissipation (T_{case} = 70 °C)	21	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

3.2 Recommended operating conditions

Table 5. Recommended operating conditions (1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	DC supply voltage	10		36.0	V
V_L	Input logic reference	2.7	3.3	5.0	V
T_{amb}	Ambient temperature	0		70	°C

1. Performances not guaranteed beyond recommended operating conditions

3.3 Thermal data

Table 6. Thermal data (1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)			1.5	°C/W
T_{jSD}	Thermal shut-down junction temperature		150		°C
T_{warn}	Thermal warning temperature		130		°C
t_{hSD}	Thermal shut-down hysteresis		25		°C

1. See Thermal information

3.4 Thermal information

The power dissipated within the device depends primarily on the supply voltage, load impedance and output modulation level. The PSSO36 package of the STA518 includes an exposed thermal slug on the top of the device to provide a direct thermal path from the IC to the heatsink. For the Quad single ended application the dissipated power vs. output power is shown in *Figure 10*.

Considering that for the STA518 the thermal resistance junction to slug is 1.5 °C/W and the estimated thermal resistance due to the grease placed between slug and heat sink is 2.3 °C/W (the use of thermal pads for this package is not recommended), the suitable heat sink R_{th} to be used can be drawn from the following graph *Figure 11*, where is shown the derating power vs. t_{amb} for different heat sinks.

3.5 Electrical characteristics

Refer to circuit in *Figure 3* (V_L = 3.3 V; V_{CC} = 30 V; R_L = 8 Ω; f_{sw} = 384 kHz; T_{amb} = 25 °C unless otherwise specified)

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power P-channel / N-channel MOSFET R_{dsON}	I_d = 1A		200	270	mΩ
I_{dss}	Power P-channel / N-channel leakage I_{dss}	V_{CC} = 35V			50	µA
g_N	Power P-channel R_{dsON} Matching	I_d = 1A	95			%
g_P	Power N-channel R_{dsON} Matching	I_d = 1A	95			%
Dt_s	Low current dead time (static)	see test circuit *Figure 3*		10	20	ns
Dt_d	High current dead time (dynamic)	L = 22µH; C = 470nF; R_L = 8 Ω I_d = 3A; see*Figure 5*			50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load; V_{CC} = 30V			100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load; V_{CC} = 30V			100	ns
t_r	Rise time	Resistive load; as *Figure 3*			25	ns
t_f	Fall time				25	ns
V_{CC}	Supply voltage operating voltage		10		36	V
V_{IN-H}	High level input voltage				V_L/2 +300mV	V
V_{IN-L}	Low level input voltage		V_L/2 - 300mV			V
I_{IN-H}	Hi level input current	Pin voltage = V_L		1		µA
I_{IN-L}	Low level input current	Pin voltage = 0.3V		1		µA
$I_{PWRDN-H}$	Hi level PWRDN pin input current	V_L = 3.3V		35		µA
V_{LOW}	Low logical state voltage V_{LOW} (pin PWRDN, TRISTATE) (1)	V_L = 3.3V	0.8			V
V_{HIGH}	High logical state voltage V_{HIGH} (pin PWRDN, TRISTATE) (1)	V_L = 3.3V			1.7	V
$I_{VCC-PWRDN}$	Supply current from V_{CC} in power down	PWRDN = 0			3	mA

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{FAULT}	Output current pins FAULT -TH-WARN when FAULT CONDITIONS	V_{pin} = 3.3V		1		mA
$I_{VCC-hiz}$	Supply current from V_{CC} in Tri-state	V_{CC} = 30V; Tri-state = 0		22		mA
I_{VCC}	Supply current from V_{CC} in operation (both channel switching)	V_{CC} = 30V; Input pulse width = 50% Duty; Switching Frequency = 384kHz; No LC filters;		50		mA
I_{VCC-q}	I_{sc} (short-circuit current limit) (2)	V_{CC} = 30V	3.5	6		A
V_{UV}	Undervoltage protection threshold			7		V
t_{pw_min}	Output minimum pulse width	No Load	70		150	ns

1. The *Table 8* explains the V_{LOW}, V_{HIGH} variation with I_{bias}.
2. See relevant Application Note AN1994

Table 8. V_{LOW}, V_{HIGH} variation with I_{bias}

V_L	$V_{Low\ min}$	$V_{High\ max}$	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Table 9. Logic truth table (see *Figure 4*)

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	Output mode
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 3. Low current dead time for single end application: test circuit.

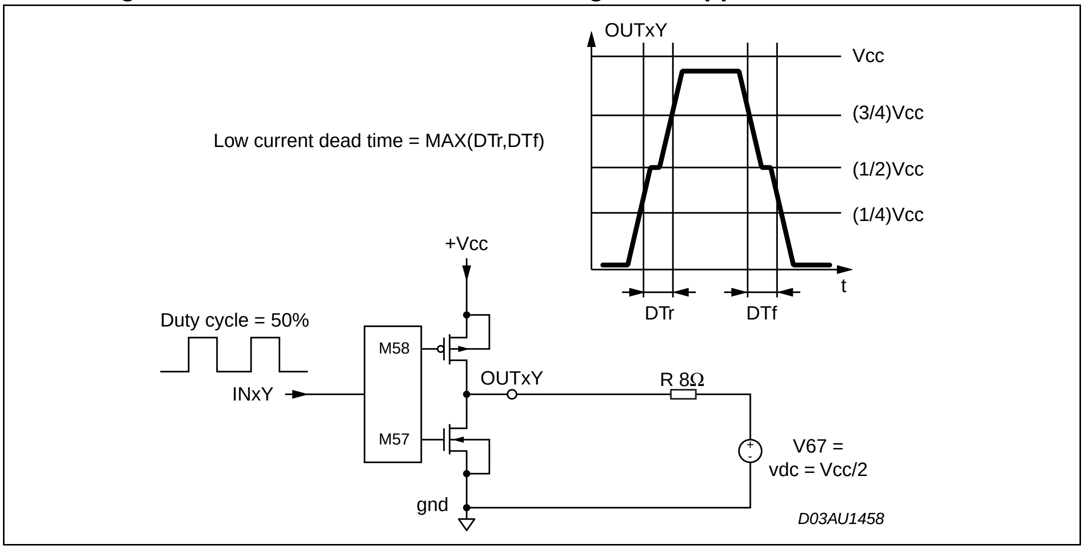


Figure 4. High current dead time for bridge application: block diagram

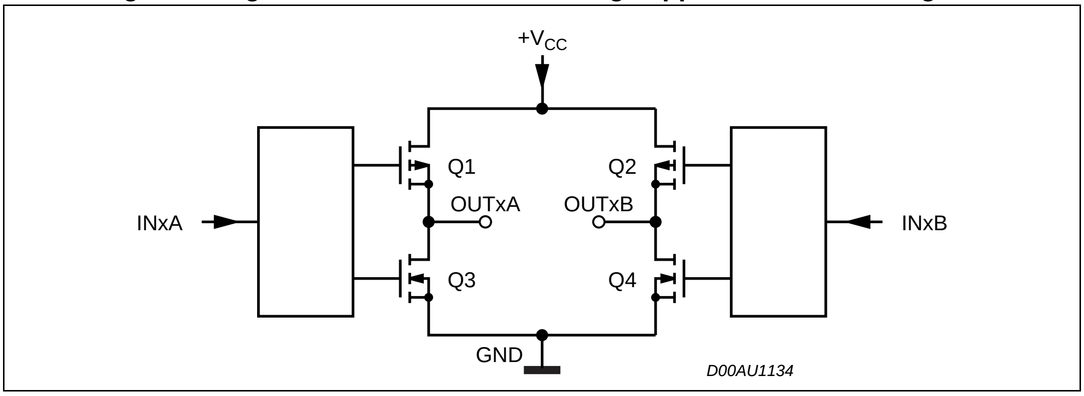
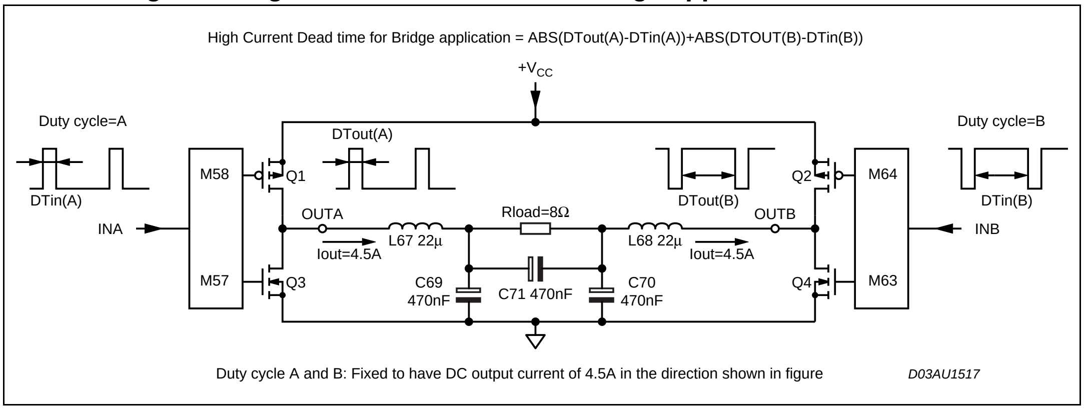


Figure 5. High current dead time for bridge application: test circuit



4 Technical information

The STA518 is a dual channel H-Bridge that is able to deliver 50 W per channel (@ THD = 10% R_L = 8 Ω, V_{CC} = 29 V) of audio output power in high efficiency.

The STA518 converts both DDX and binary-controlled PWM signals into audio power at the load. It includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs and thermal and short-circuit protection circuitry.

In DDX mode, two logic level signals per channel are used to control high-speed MOSFET switches to connect the speaker load to the input supply or to ground in a bridge configuration, according to the damped ternary modulation operation.

In binary mode operation, both full bridge and half bridge modes are supported. The STA518 includes over-current and thermal protection as well as an undervoltage lockout with automatic recovery. A thermal warning status is also provided.

Figure 6. STA518 block diagram full-bridge DDX® or binary modes

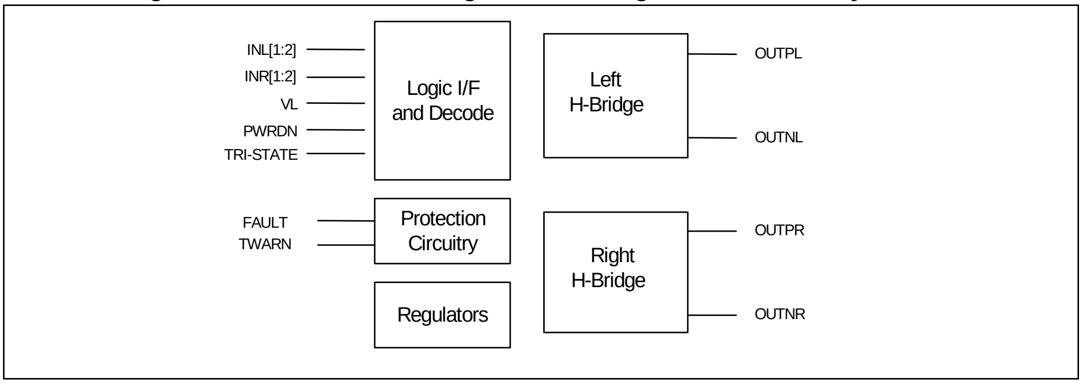
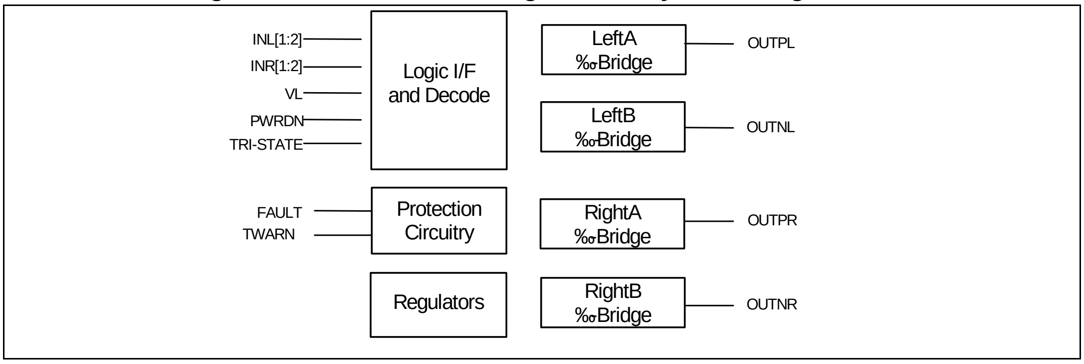


Figure 7. STA518 block diagram binary half-bridge mode



4.1 Logic interface and decode

The STA518 power outputs are controlled using one or two logic level timing signals. In order to provide a proper logic interface, the V_{bias} input must operate at the same voltage as the DDX control logic supply.

Protection circuitry:

The STA518 includes protection circuitry for over-current and thermal overload conditions. A thermal warning pin (pin. 28) is activated low (open drain MOSFET) when the IC temperature exceeds 130 °C, in advance of the thermal shutdown protection. When a fault condition is detected, an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-Bridges in high impedance state. At the same time an open-drain MOSFET connected to the fault pin (pin.27) is switched on.

There are two possible modes subsequent to activating a fault:

1. **SHUTDOWN mode**: with FAULT (pull-up resistor) and TRI-STATE pins independent, an activated fault will disable the device, signaling low at the FAULT output.
   The device may subsequently be reset to normal operation by toggling the TRI-STATE pin from high to low to high using an external logic signal.
2. **AUTOMATIC recovery mode:** This is shown in the audio application circuit of quad single ended). The FAULT and TRI-STATE pins are shorted together and connected to a time constant circuit comprising R59 and C58.
   An activated FAULT will force a reset on the TRI-STATE pin causing normal operation to resume following a delay determined by the time constant of the circuit.
   If the fault condition is still present, the circuit operation will continue repeating until the fault condition is removed.
   An increase in the time constant of the circuit will produce a longer recovery interval. Care must be taken in the overall system design as not to exceed the protection thresholds under normal operation.

4.2 Power outputs

The STA518 power and output pins are duplicated to provide a low impedance path for the device's bridged outputs. All duplicate power, ground and output pins must be connected for proper operation.

The PWRDN or TRI-STATE pins should be used to set all MOSFETS to the Hi-Z state during power-up until the logic power supply, V_L, is settled.

4.3 Parallel output / high current operation

When using DDX mode output, the STA518 outputs can be connected in parallel in order to increase the output current capability to a load. In this configuration the STA518 can provide 70 W into 8 ohm.

This mode of operation is enabled with the CONFIG pin, the (pin 24) connected to VREG1 and the inputs combined INLA=INLB, INRA=INRB and the outputs combined OUTLA=OTLB, OUTRA=OUTRB.

4.4 Additional information

Output Filter: A passive 2nd order passive filter is used on the STA518 power outputs to reconstruct an analog audio signal. System performance can be significantly affected by the output filter design and choice of passive components. A filter design for 6 ohm / 8 ohm loads is shown in the typical application circuit of *Figure 9*.

Quad single ended circuit (*Figure 1*) shows a filter for ½ bridge mode, 4 ohm loads.

Figure 8. Typical stereo full bridge configuration to obtain 50 + 50 W @ THD = 10%, $R_L = 8\ \Omega$, $V_{CC} = 29$ V

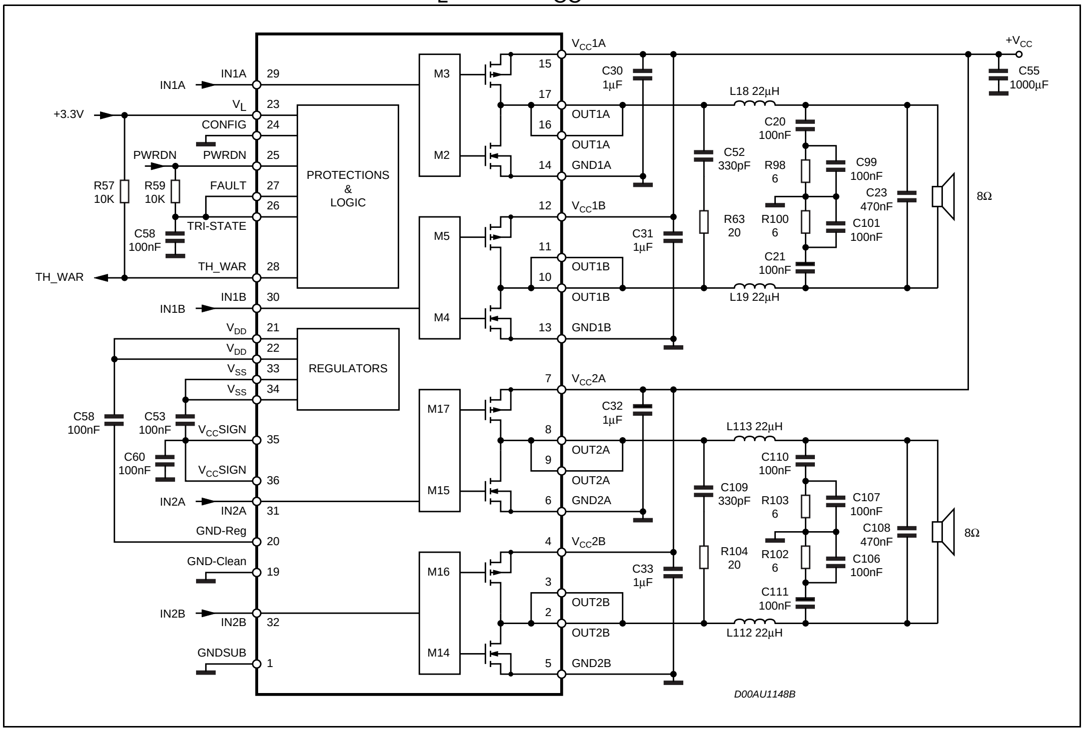
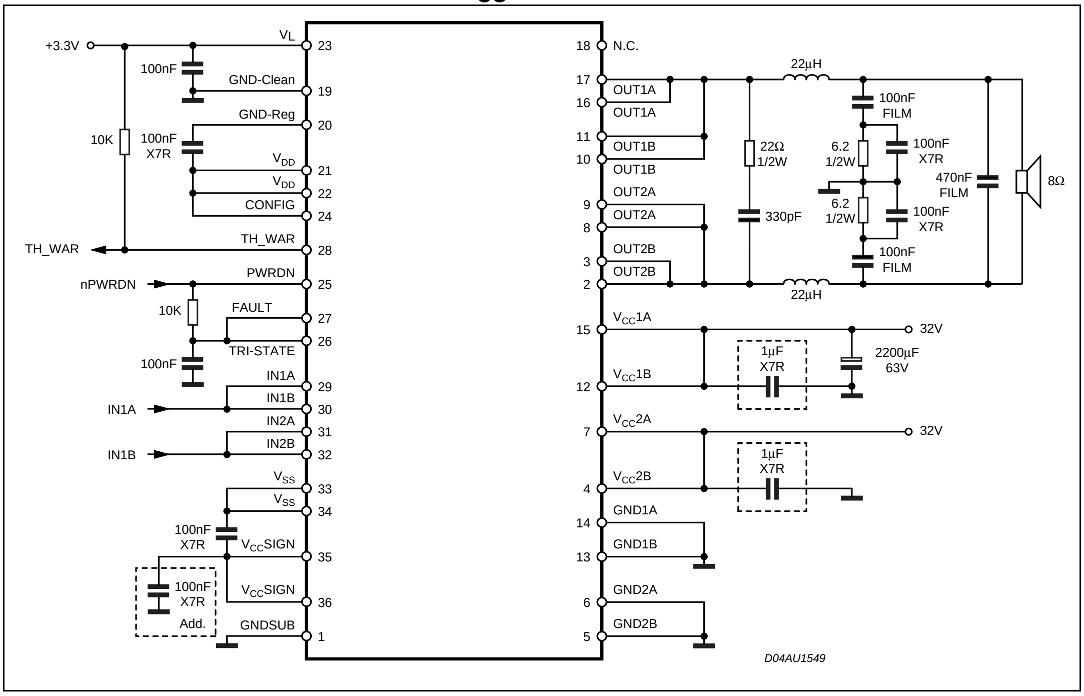


Figure 9. Typical single BTL configuration to obtain 70 W @ THD 10%, $R_L = 8\ \Omega$, $V_{CC} = 34$ V [(a)]



a. A PWM modulator as driver is needed. In particular, this result is performed using the STA308 + STA518 + STA50X demo board". Peak Power for t ≤ 1sec.

5 Characterizations curves

The following characterization are obtained using the quad single ended configuration (*Figure 1*) with STA308A controller.

Figure 10. Power dissipation vs. output power

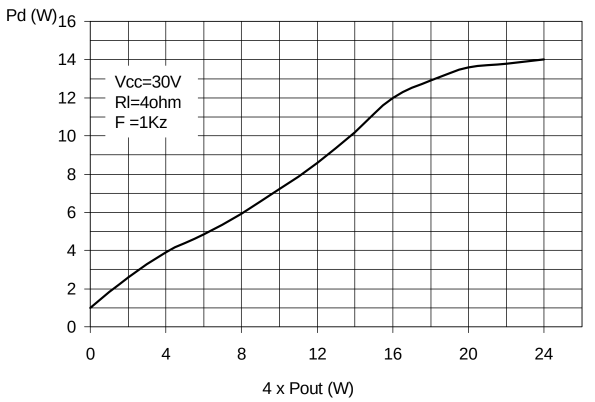


Figure 11. Power derating curve

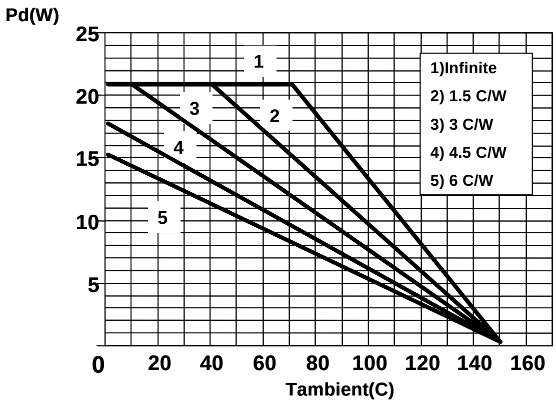


Figure 12. THD+N vs. output power

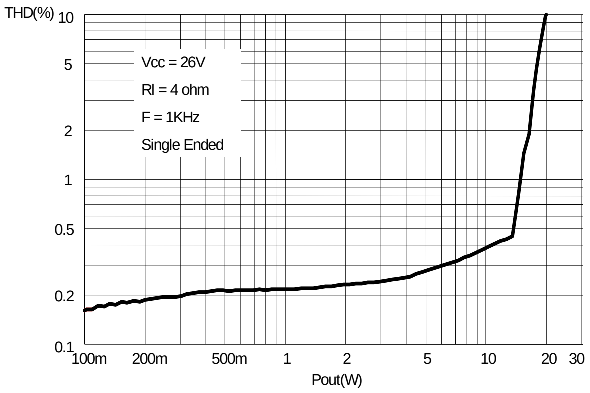


Figure 13. Output power vs. supply voltage

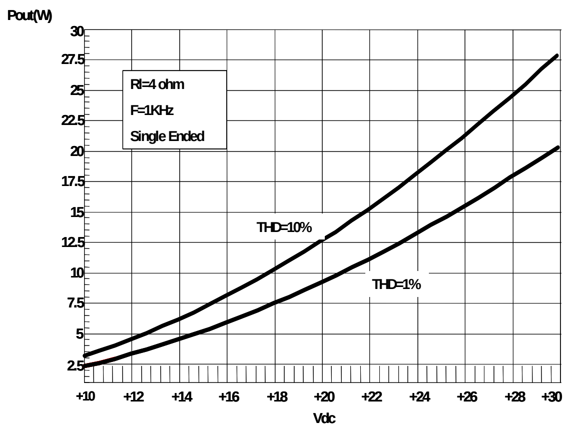
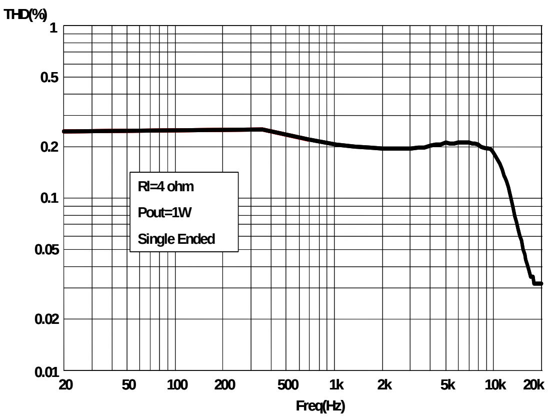


Figure 14. THD vs. frequency



The following characterizations are obtained using the stereo full bridge configuration (*Figure 8*) with STA308A controller.

Figure 15. Output power vs. supply voltage

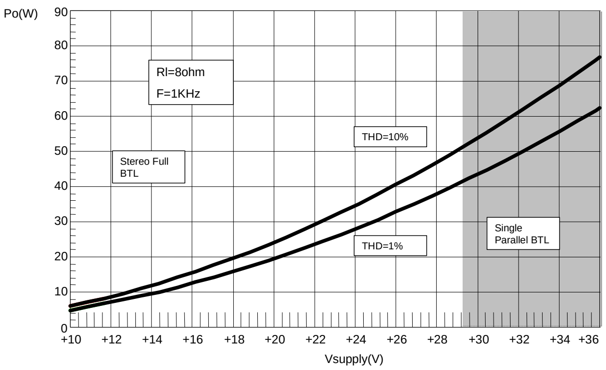


Figure 16. THD+N vs. output power

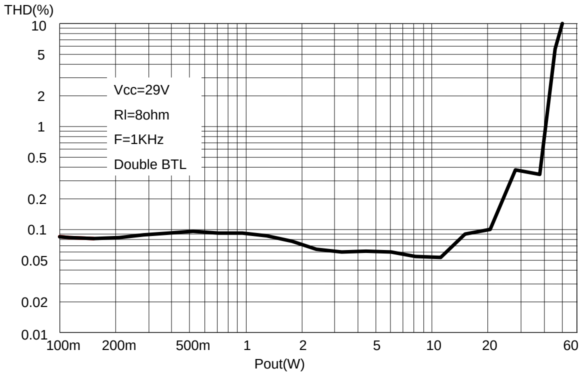
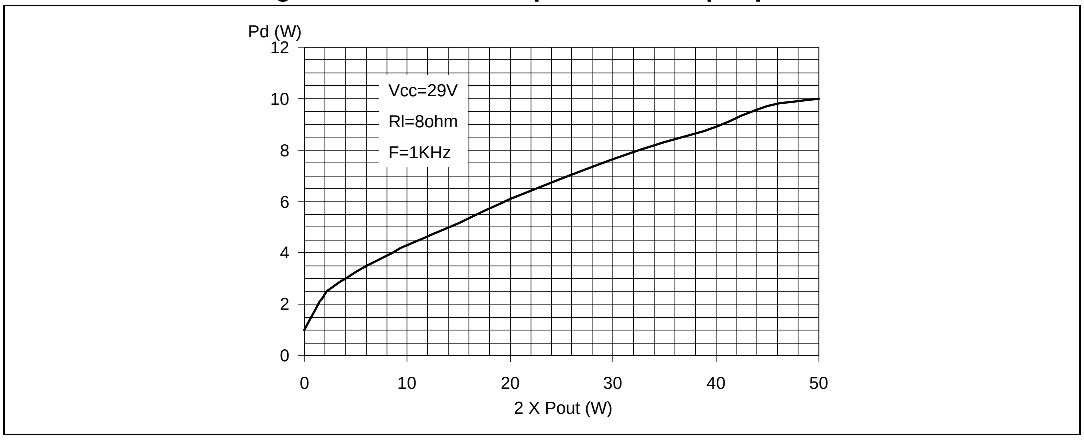
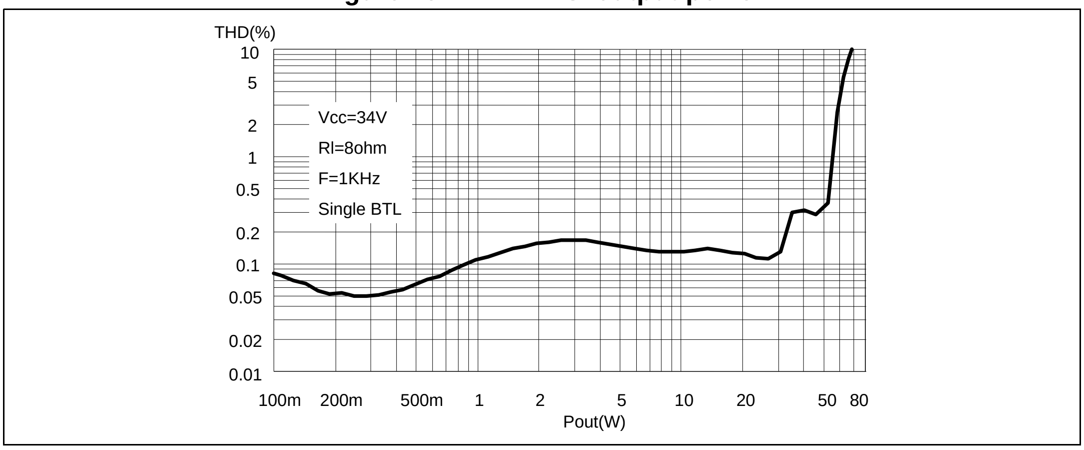


Figure 17. Power dissipation vs. output power



The following characterizations are obtained using the single BTL configuration (*Figure 9*) with STA308A controller.

Figure 18. THD+N vs. output power



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. PSSO36 (slug up) mechanical data & package dimensions

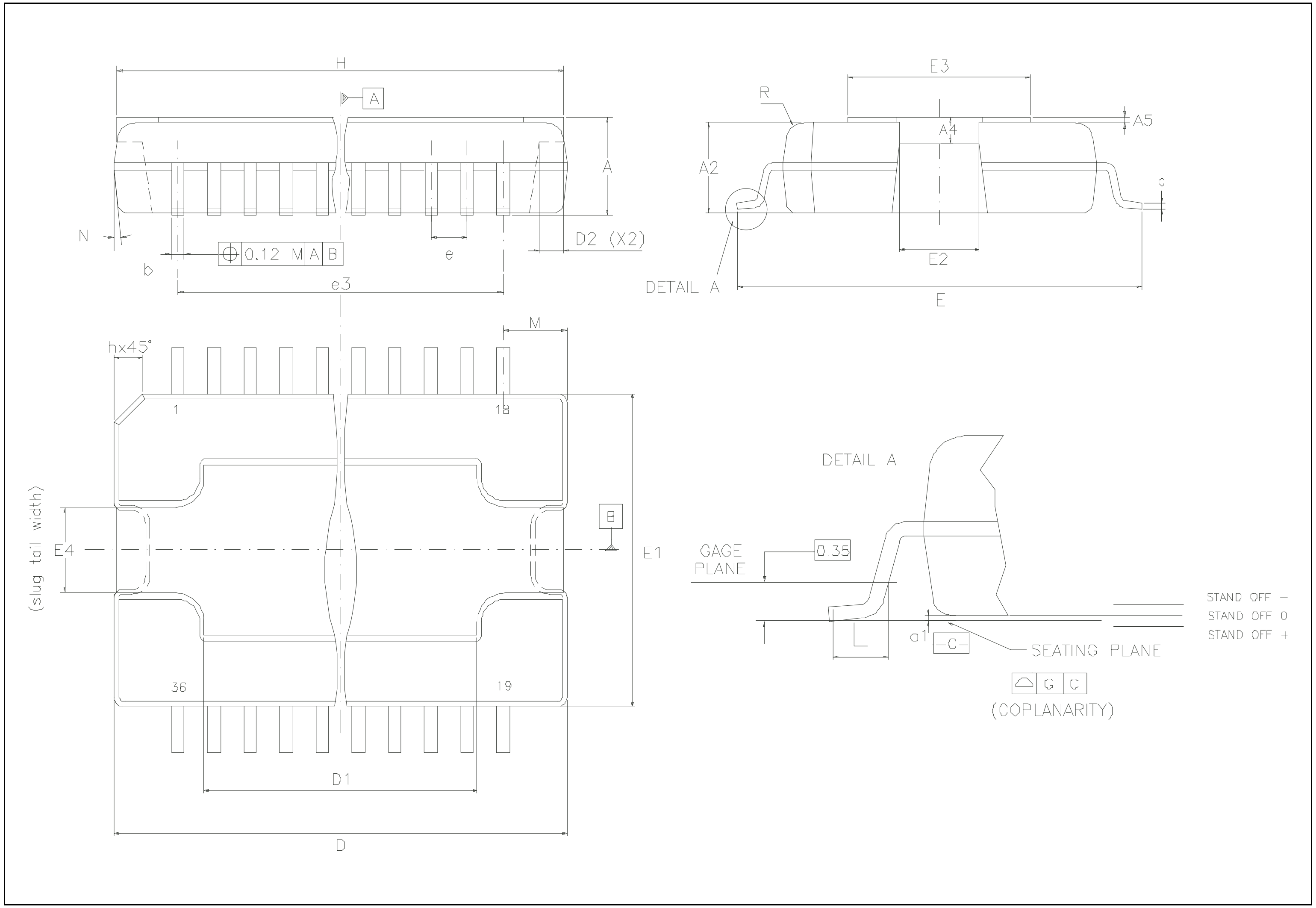


Table 10. PowerSO36 exposed pad up dimensions

Symbol	Dimensions in mm.			Dimensions in inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.25	-	3.43	0.128	-	0.135
A2	3.10	-	3.20	0.122	-	0.126
A4	0.80	-	1.00	0.031	-	0.039
A5	-	0.20	-	-	0.008	-
a1	0.03	-	-0.04	0.001	-	-0.002
b	0.22	-	0.38	0.009	-	0.015
c	0.23	-	0.32	0.009	-	0.013
D	15.80	-	16.00	0.622	-	0.630
D1	9.40	-	9.80	0.370	-	0.386
D2	-	1.00	-	-	0.039	-
E	13.90	-	14.50	0.547	-	0.571
E1	10.90	-	11.10	0.429	-	0.437
E2	-	-	2.90	-	-	0.114
E3	5.80	-	6.20	0.228	-	0.244
E4	2.90	-	3.20	0.114	-	0.126
e	-	0.65	-	-	0.026	-
e3	-	11.05	-	-	0.435	-
G	0	-	0.08	0	-	0.003
H	15.50	-	15.90	0.610	-	0.626
h	-	-	1.10	-	-	0.043
L	0.80	-	1.10	0.031	-	0.043
M	2.25	-	2.60	0.089	-	0.102
N	-	-	10 degrees	-	-	10 degrees
R	-	0.6	-	-	0.024	-
s	-	-	8 degrees	-	-	8 degrees

7 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-Aug-2004	1	Initial release.
11-Nov-2004	2	Changed symbol in “Electrical Characteristics”.
18-May-2006	3	Changed operating temperature range value to -40 to 90°C (see*Table 4*).
26-Feb-2014	4	Updated order code *Table 1 on page 1*

Please Read Carefully: