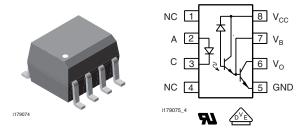


High Speed Optocoupler, 100 kBd, Low Input Current, High Gain



DESCRIPTION

Very high current ratio together with 4000 V_{RMS} isolation are achieved by coupling an LED with an integrated high gain photo detector in a SOIC-8 package. Separate pins for the photo diode and output stage enable TTL compatible saturation voltages with high speed operation. Photodarlington operation is achieved by tying the V_{CC} and V_{O} terminals together. Access to the base terminal allows adjustment to the gain bandwidth.

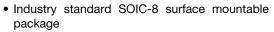
The SFH6318T is ideal for TTL applications since the 300 % minimum current transfer ratio with an LED current of 1.6 mA enables operation with one unit load-in and one unit load-out with a 2.2 k Ω pull-up resistor.

The SFH6319T is best suited for low power logic applications involving CMOS and low power TTL. A 400 % current transfer ratio with only 0.5 mA of LED current is guaranteed from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

Caution:

Due to the small geometries of this device, it should be handled with electrostatic discharge (ESD) precautions. Proper grounding would prevent damage further and/or degradation which may be induced by ESD.

FEATURES





- High current transfer ratio, 300 %
- Low input current, 0.5 mA
- High output current, 60 mA
- la alation toot valtage 4000 V
- Isolation test voltage, 4000 V_{RMS}
- TTL compatible output, V_{OL} = 0.1 V
- · Adjustable bandwidth access to base
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Logic ground isolation -TTL/TTL, TTL/CMOS, CMOS/CMOS, CMOS/TTL
- EIA RS 232C line receiver
- · Low input current line receiver long lines, party lines
- Telephone ring detector
- 117 VAC line voltage status indication low input power dissipation
- Low power systems ground isolation

AGENCY APPROVALS

- UL1577, file no. E52744, system code Y, double protection
- DIN EN 60747-5-5 (VDE 0884-5) available with option 1
- CSA 93751

ORDERING INFORMATION					
S F H	6 3 # #	T SOIC-8			
	PART NUMBER	6.1 mm			
AGENCY CERTIFIED/PACKAGE	CTR (%)				
UL, CSA	≥ 300	≥ 500			
SOIC-8	SFH6318T ⁽¹⁾	SFH6319T ⁽¹⁾			
SOIC-8, tube	SFH6318	SFH6319			

Note

(1) Available in tubes and in tape and reel



PARAMETER	TEST CONDITION	PART	SYMBOL	VALUE	UNIT
INPUT					
Reverse voltage			V _R	3	V
Cumply and autout valtage	V (nin 8 to 5) V (nin 6 to 5)	SFH6318T	V _{CC} , V _O	- 0.5 to 7	V
Supply and output voltage	V _{CC} (pin 8 to 5), V _O (pin 6 to 5)	SFH6319T	V _{CC} , V _O	- 0.5 to 18	V
Input power dissipation			P _{diss}	35	mW
Derate linearly above				50	°C
Free air temperature				0.7	mW/°C
Average input current			I _{F(AVG)}	20	mA
Peak input current	50 % duty cycle - 1 ms pulse width		I _{FRM}	40	mA
Peak transient input current	t _p ≤ 1 μs, 300 pps		I _{FSM}	1	Α
OUTPUT					
Output current (pin 6)			I ₀	60	mA
Emitter-base reverse current (pin 5 to 7)				0.5	V
Output power dissipation			P _{diss}	150	mW
Derate linearly from 25 °C				2	mW/°C
COUPLER					
Isolation test voltage between emitter and detector			V _{ISO}	4000	V _{RMS}
Storage temperature			T _{stg}	- 55 to + 125	°C
Lead soldering temperature (1)	t = 10 s		T _{sld}	260	°C
Junction temperature			Tj	100	°C
Ambient temperature range			T _{amb}	- 55 to + 100	°C
Pollution degree (DIN VDE 0110)				2	
Creepage distance				≥ 4	mm
Clearance distance				≥ 4	mm
Comparative tracking index per DIN IEC112/VDE 0303, part 1			СТІ	175	
location veniatores	V _{IO} = 500 V, T _{amb} = 25 °C		R _{IO}	≥ 10 ¹²	Ω
Isolation resistance	V _{IO} = 500 V, T _{amb} = 100 °C		R _{IO}	≥ 10 ¹¹	Ω

Notes

⁽¹⁾ Refer to reflow profile soldering conditions for surface mounted devices.

ELECTRICAL CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)										
PARAMETER	TEST CONDITION SYMBOL		MIN.	TYP.	MAX.	UNIT				
INPUT										
Forward voltage	I _F = 1.6 mA	V _F		1.4	1.7	V				
Temperature coefficient, forward voltage	I _F = 1.6 mA	$\Delta V_F/\Delta T_{amb}$		- 1.8		mV/°C				
OUTPUT										
	$I_F = 1.6 \text{ mA}, I_O = 4.8 \text{ mA}, V_{CC} = 4.5 \text{ V}$	V _{OL}		0.1	0.4	V				
Logic low output voltage (1)	$I_F = 1.6 \text{ mA}, I_O = 8 \text{ mA}, V_{CC} = 4.5 \text{ V}$	V _{OL}		0.1	0.4	V				
Logic low output voltage (**)	$I_F = 5 \text{ mA}, I_O = 15 \text{ mA}, V_{CC} = 4.5 \text{ V}$	V _{OL}		0.15	0.4	V				
	$I_F = 12 \text{ mA}, I_O = 24 \text{ mA}, V_{CC} = 4.5 \text{ V}$	V _{OL}		0.25	0.4	V				
Logic bigh output ourrent (1)	$I_F = 0 \text{ mA}, V_O = V_{CC} = 7 \text{ V}$	I _{IO}		0.1	250	μΑ				
Logic high output current (1)	$I_F = 0 \text{ mA}, V_O = V_{CC} = 18 \text{ V}$	I _{IO}		0.05	100	μΑ				
Logic low supply current (1)	$I_F = 1.6 \text{ mA}, V_O = \text{OPEN}, V_{CC} = 18 \text{ V}$	I _{CCL}		0.2	1.5	mA				
Logic high supply current (1)	$I_F = 0$ mA, $V_O = OPEN$, $V_{CC} = 18$ V	I _{CCH}		0.01	10	μΑ				

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. Functional operation of the device is not
implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute
maximum ratings for extended periods of the time can adversely affect reliability.



ELECTRICAL CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)							
PARAMETER TEST CONDITION SYMBOL MIN. TYP. MA							
COUPLER							
Capacitance (input to output) (2)	f = 1 MHz	C _{IO}		0.6		pF	
Input capacitance	f = 1 MHz, V _F = 0	C _{IN}		25		pF	
Resistance (input to output) (2)	V _{IO} = 500 VDC, T _{amb} = 25 °C	R _{IO}		10 ¹²		Ω	
nesistance (input to output) (=)	V _{IO} = 500 VDC, T _{amb} = 100 °C	R _{IO}		10 ¹¹		Ω	

Notes

- Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.
 T_{amb} = 0 °C to 70 °C. Typical values are specified at T_{amb} = 25 °C.
- (1) Pin 7 open.
- (2) Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

CURRENT TRANSFER RATIO								
PARAMETER TEST CONDITION PART SYMBOL MIN. TYP. MAX. UNI								
Current transfer ratio	$I_F = 1.6 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V}$	SFH6318T	CTR	300	1600	2600	%	
	$I_F = 0.5 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V}$	SFH6319T	CTR	400	2000	3500	%	
	$I_F = 1.6 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V}$	SFH6319T	CTR	500	1600	2600	%	

Note

T_{amb} = 0 °C to 70 °C. Typical values are specified at T_{amb} = 25 °C.
 DC current transfer ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F times 100 %. Pin 7 open.

SWITCHING CHARACTERISTICS (T _{amb} = 25 °C, unless otherwise specified)								
PARAMETER	TEST CONDITION	PART	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Propagation delay time to logic low at output	$I_F = 1.6 \text{ mA}, R_L = 2.2 \text{ k}\Omega$	SFH6318T	t _{PHL}		2	10	μs	
Propagation delay time to logic low at output ⁽¹⁾	I_F = 0.5 mA, R_L = 4.7 k Ω	SFH6319T	t _{PHL}		6	25	μs	
Propagation delay time to logic low at output	$I_F = 12 \text{ mA}, R_L = 270 \Omega$	SFH6319T	t _{PHL}		0.6	1	μs	
Propagation delay time to logic high at output	I_F = 1.6 mA, R_L = 2.2 k Ω	SFH6318T	t _{PLH}		2	35	μs	
Propagation delay time to logic high at output ⁽¹⁾	I_F = 0.5 mA, R_L = 4.7 k Ω	SFH6319T	t _{PLH}		4	60	μs	
Propagation delay time to logic high at output	$I_F = 12 \text{ mA}, R_L = 270 \Omega$	SFH6319T	t _{PLH}		1.5	7	μs	

Note

(1) Pin 7 open. Using a resistor between pin 5 and 7 will decrease gain and delay time.

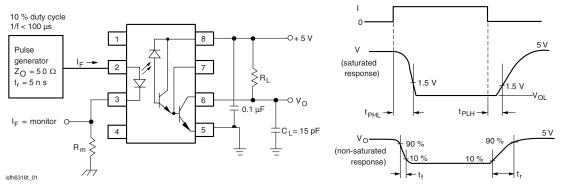


Fig. 1 - Switching Test Circuit



COMMON MODE TRANSIENT IMMUNITY								
PARAMETER TEST CONDITION SYMBOL MIN. TYP. MAX. UN								
Common mode transient immunity at logic high level output	$I_F = 0 \text{ mA}, R_L = 2.2 \text{ k}\Omega, V_{CM} = 10 V_{P-P}$	CM _H		1K		V/µs		
Common mode transient immunity at logic low level output	$I_F = 1.6 \text{ mA}, R_L = 2.2 \text{ k}\Omega, V_{CM} = 10 \text{ V}_{P-P}$	CM _H		1K		V/µs		

Note

Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a logic high state (i.e. V_O > 2 V) common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e. V_O < 0.8 V).

In applications where dv/dt may exceed 50,000 V/µs (such as state discharge) a series resistor, R_{CC} should be included to protect I_C from destructively high surge currents. The recommended value is refer to figure 2. $R_{CC} \cong [(IV)/0.15 \ I_F \ (mA)] \ k\Omega$.

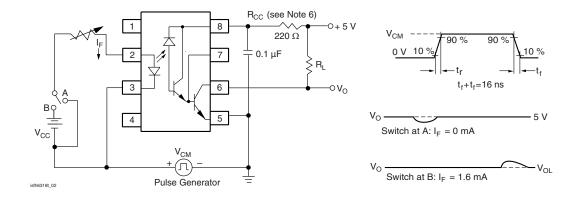


Fig. 2 - Test Circuit for Transient Immunity and Typical Waveforms

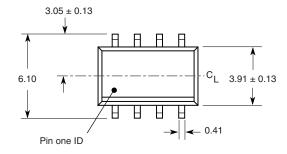
SAFETY AND INSULATION RATINGS								
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT		
Climatic Classification	according to IEC 68 part 1			55/100/21				
Comparative Tracking Index		CTI	175		399			
V _{IOTM}			6000			V		
V _{IORM}			560			V		
P _{SO}					350	mW		
I _{SI}					150	mA		
T _{SI}					165	°C		
Creepage distance			4			mm		
Clearance distance			4			mm		
Insulation thickness			0.2			mm		

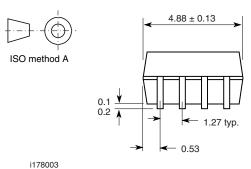
Note

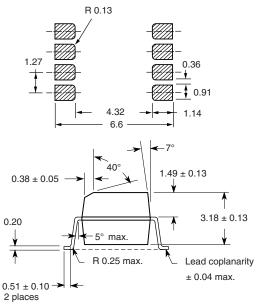
As per IEC 60747-5-5, §7.4.3.8.1, this optocoupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with
the safety ratings shall be ensured by means of protective circuits.



PACKAGE DIMENSIONS in millimeters







PACKAGE MARKING (example)





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