Panasonic

# AN32258A

http://www.semicon.panasonic.co.jp/en/

# INTEGRATED WIRELESS POWER SUPPLY RECEIVER, Qi (WIRELESS POWER CONSORTIUM) COMPLIANT

## FEATURES

- Integrated Wireless Power Receiver Solution
- WPC Ver. 1.1 Compliant
- Synchronous Full Bridge Rectifier Control
- Input Voltage Range : VRECT = 4.4 V to 19 V
- Selectable Output Voltage: 5, 7V
- Temperature Detecting Circuit
- Full Charge Detection with Adjustable Current Level
- Switching Control of External Power Supply
- Supports Under Voltage Lockout , Thermal Shutdown, Over Voltage Detection, and Over Current Detection.
- LED Indicator
- I²C Interface
- 3.16 mm X 3.16 mm WLCSP
  48 Pins with 0.4mm pitch

## DESCRIPTION

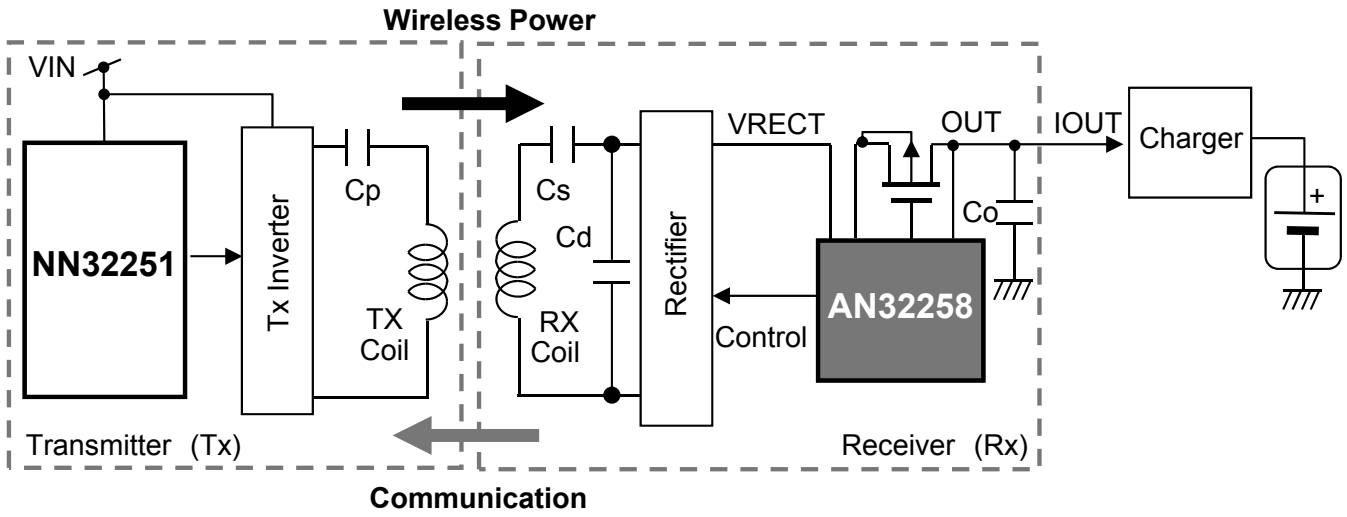
AN32258A is a wireless power system controller IC which is compliant with Qi version 1.1 of the System Description Wireless Power Transfer, Volume 1 for Low Power defined by Wireless Power Consortium. AN32258A is a controller IC of a power receiver (Rx) which can be used with any Qi-compliant wireless chargers.

Over 5W high power transfer is achievable with wireless chargers using Panasonic Tx IC NN32251A.

## APPLICATIONS

- WPC Compliant Receivers
- Cell Phones, Smartphones
- Headsets
- Digital Cameras
- Tablet Devices
- Portable Media Players etc.

## Wireless Power System



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## CONTENTS





Established : 2014-01-15
Revised : ####-##-##

## DELIVERY INFORMATION

| Order Number | Package | Output Supply | Minimum Quantity |
|---|---|---|---|
| AN32258A-PR | 48 pin WLCSP(3.2×3.2mm) | Embossed Taping | 5000pcs |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Notes |
|---|---|---|---|---|
| Supply voltage | $V_{RECT}$ | 20 | V | *1 |
| | $V_{EXT}$ | 6.9 | V | *1 |
| | $V_{IO}$ | 6 | V | *1 |
| Output current | $I_{RECT}$ | — | A | *1 |
| Operating ambient temperature | $T_{opr}$ | – 30 to + 85 | °C | *2 |
| Operating junction temperature | $T_j$ | -40 to +125 | °C | *2 |
| Storage temperature | $T_{stg}$ | – 50 to + 125 | °C | *2 |
| Input voltage range | $V_{DETIN}$, $V_{TD2}$, $V_{TD1}$, $V_{SC2}$, $V_{SC1}$ | – 0.3 to 20 | V | *1 |
| | $V_{OUT}$, $V_{LED}$ | – 0.3 to 12 | V | *1 |
| | $V_{SCL}$, $V_{SDA}$, $V_{EXTCLK}$ | – 0.3 to ($V_{IO}$ + 0.3) | V | *1 |
| | $V_{VTH}$, $V_{FCCNT}$, $V_{FODG}$, $V_{SELVER}$ $V_{FULLCH}$, $V_{FOD}$, $V_{SELHP}$ $V_{SELOSR}$, $V_{FODL}$, $V_{SELHV}$ | – 0.3 to ($V_{VREG34V}$ + 0.3) | V | *1 |
| Output voltage range | $V_{VPGATE}$ | – 0.3 to ($V_{RECT}$ + 0.3) | V | *1 |
| | $V_{DT1H}$ | – 0.3 to($V_{sc1}$ + $V_{VREG47V}$+ 0.3) | V | *1 |
| | $V_{DT2H}$ | – 0.3 to($V_{sc2}$ + $V_{VREG47V}$+ 0.3) | V | *1 |
| | $V_{DT2L}$, $V_{DT1L}$ | – 0.3 to ( $V_{VREG47V}$ + 0.3 ) | V | *1 |
| | $V_{EXTCNT}$ | – 0.3 to ( $V_{EXT}$ + 0.3 ) | V | *1 |
| | $V_{MEMBAT}$ | – 0.3 to ($V_{VREG34V}$ + 0.3) | V | *1 |
| | $V_{OUTHP}$, $V_{ENI2C}$ | – 0.3 to ($V_{IO}$ + 0.3) | V | *1 |
| ESD | TD2 | 1.0 | kV | — |
| | HBM (Human Body Model) ISENSE1, ISENSE2, ISENSE1-S, ISENSE1-S1 | 1.5 | kV | — |
| | HBM (Human Body Model) Except for pins above | 2 | kV | — |

Note) This product may sustain permanent damage if the actual condition is higher than the absolute maximum rating stated above. This rating is the maximum stress, and device will not be guaranteed to operate in case it is higher than our stated range. When exposed to the absolute maximum rating for a long time, the reliability of the product may be affected.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C.



Established : 2014-01-15
Revised : ####-##-##

## POWER DISSIPATION RATING

| PACKAGE | $\theta_{j-a}$ | $\theta_{j-C}$ | PD (Ta = 25 °C) | PD (Ta = 85 °C) | Notes |
|---|---|---|---|---|---|
| Wafer Level Chip Size Package (WLCSP type) | 631.4 °C / W | 7.2 °C /W | 0.158 W | 0.0632 W | *1 |

Note). *1 :For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, and follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

**CAUTION**

Although this device has limited built-in ESD protection circuit, permanent damage may occur on it. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Pin Name | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage range | $V_{RECT}$ | 4.4 | 8 | 19 | V | *2 |
| | $V_{EXT}$ | 4.4 | 5 | 6 | V | |
| | $V_{IO}$ | 1.74 | 3.3 | 5.5 | V | |

Note) *2 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

## ELECRTRICAL CHARACTERISTICS

Co = 10 µF, $V_{RECT}$ = 8 V, $T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Current Consumption** | | | | | | | |
| Quiescent current | $I_{STBY}$ | | 10 | 12 | 14 | mA | |
| **Under-voltage lock-out (UVLO)** | | | | | | | |
| Under-voltage lock-out | $V_{UVLO}$ | $V_{RECT}$ : 0V -> 5V | 3.29 | 3.5 | 3.71 | V | |
| Hysteresis on UVLO | $V_{UVLOHY}$ | $V_{RECT}$ : 5V -> 3V | - | 0.7 | - | V | *1 |
| **Over-voltage protection (OVP)** | | | | | | | |
| Input overvoltage threshold | $V_{OVP}$ | $V_{RECT}$ : 5V -> 19V | 17 | 18 | 19 | V | |
| Hysteresis on OVP | $V_{OVPOHY}$ | $V_{RECT}$ : 19V -> 5V | - | 4 | - | V | *1 |
| **$V_{RECT}$ (5W, LDO 5V mode )** | | | | | | | |
| $V_{RECT}$ Threshold1 | $V_{RECTTH1}$ | In increasing $I_{OUT}$ < 125mA<br>In decreasing I : $I_{OUT}$ <60mA | - | 8 | - | V | *1 |
| $V_{RECT}$ Threshold2 | $V_{RECTTH2}$ | In increasing<br>125mA<$I_{OUT}$<420mA<br>In decreasing<br>60mA<$I_{OUT}$<360mA | - | 5.4 | - | V | *1 |
| $V_{RECT}$ Threshold3 | $V_{RECTTH3}$ | In increasing $I_{OUT}$ > 420mA<br>In decreasing $I_{OUT}$ > 360mA | - | 5.1 | - | V | *1 |
| **$V_{RECT}$ (5W, LDO 7V mode )** | | | | | | | |
| $V_{RECT}$ Threshold7 | $V_{RECTTH7}$ | In increasing $I_{OUT}$ < 125mA<br>In decreasing $I_{OUT}$ < 60mA | - | 10 | - | V | *1 |
| $V_{RECT}$ Threshold8 | $V_{RECTTH8}$ | In increasing<br>125mA<$I_{OUT}$<420mA<br>In decreasing<br>60mA<$I_{OUT}$<360mA | - | 7.4 | - | V | *1 |
| $V_{RECT}$ Threshold9 | $V_{RECTTH9}$ | In increasing $I_{OUT}$>420mA<br>In decreasing $I_{OUT}$>360mA | - | 7.1 | - | V | *1 |
| **OUTPUT** | | | | | | | |
| $V_{OUT}$ (5W, LDO 5V mode ) | $V_{OUT1}$ | VRECT=8V ,$I_{OUT}$=10mA | 4.76 | 5 | 5.24 | V | |
| | $V_{OUT2}$ | VRECT=5.1V ,<br>$I_{OUT}$=1000mA | 4.76 | — | — | V | |
| $V_{OUT}$ (5W, LDO 7V mode ) | $V_{OUT4}$ | VRECT=10V ,$I_{OUT}$=10mA<br>Co = 10µF | 6.76 | 7 | 7.24 | V | |

Note) *1 : Designed typical values



Established : 2014-01-15
Revised : ####-##-##

## ELECRTRICAL CHARACTERISTICS (Continued)

Co = 10 µF, $V_{RECT}$ = 8 V, $T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Temperature Detection [Thermistor : ERTJ0EV104F]** | | | | | | | |
| Over-temperature Detection Voltage | $V_{TH}$ | 60 °C detection<br>VTHR:47 kohm (±1%) | 0.887 | 0.975 | 1.069 | V | |
| **Over-current protection (OCP)** | | | | | | | |
| Over-current threshold voltage 1 | $V_{OCPL}$ | SELHP=L | 1.25 | 1.5 | 1.75 | A | |
| Over-current threshold voltage 2 | $V_{OCPH}$ | SELHP=H<br>( With NN32251A for Tx) | 2.25 | 2.6 | 2.95 | A | |
| **Thermal protection** | | | | | | | |
| Thermal shutdown temperature | $T_j$ | — | — | 150 | — | □ | *1 |
| Thermal shutdown hysteresis | $T_{jhys}$ | — | — | 20 | — | □ | *1 |
| **External voltage detection** | | | | | | | |
| $V_{EXT}$ Rising threshold voltage | $V_{EXTTH}$ | — | 3.99 | 4.2 | 4.41 | V | |
| $V_{EXT}$ hysteresis | $V_{EXTHY}$ | — | — | 0.4 | — | V | *1 |
| **Terminal voltage (FULLCH)** | | | | | | | |
| High input threshold (Termination) | $V_{IH1}$ | — | 1.6 | — | — | V | |
| Low input threshold | $V_{IL1}$ | — | -0.2 | — | 0.2 | V | |
| **Terminal voltage (SELVER)** | | | | | | | |
| High input threshold (Termination) | $V_{IH1}$ | — | 1.6 | — | — | V | |
| Low input threshold | $V_{IL1}$ | — | -0.2 | — | 0.2 | V | |
| **Terminal voltage (SELHP)** | | | | | | | |
| High input threshold (Termination) | $V_{IH1}$ | — | 1.6 | — | — | V | |
| Low input threshold | $V_{IL1}$ | — | -0.2 | — | 0.2 | V | |
| **Terminal voltage (SELOSR)** | | | | | | | |
| High input threshold (Termination) | $V_{IH1}$ | — | 1.6 | — | — | V | |
| Low input threshold | $V_{IL1}$ | — | -0.2 | — | 0.2 | V | |
| **Terminal voltage (FODL)** | | | | | | | |
| High input threshold (Termination) | $V_{IH1}$ | — | 1.6 | — | — | V | |
| Low input threshold | $V_{IL1}$ | — | -0.2 | — | 0.2 | V | |
| **Terminal voltage (SELHV)** | | | | | | | |
| High input threshold (Termination) | $V_{IH1}$ | — | 2.9 | — | — | V | |
| Low input threshold | $V_{IL1}$ | — | -0.2 | — | 0.5 | V | |

Notes) *1 : Designed typical values



Established : 2014-01-15
Revised : ####-##-##

## ELECRTRICAL CHARACTERISTICS (Continued)

Co = 10 µF, $V_{RECT}$ = 8 V, $T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **Terminal voltage (EXTCLK)** | | | | | | | |
| High input threshold (Termination) | $V_{IH1}$ | $V_{IO}$ = 3.3V | $V_{IO}$ × 0.7 | — | — | V | — |
| Low input threshold | $V_{IL1}$ | $V_{IO}$ = 3.3V | -0.2 | — | $V_{IO}$ × 0.3 | V | — |
| **Terminal voltage (OUTHP)** | | | | | | | |
| Output High level | $V_{OH}$ | $V_{IO}$ = 3.3V<br>$I_{OUTHP}$ = -2mA | $V_{IO}$ × 0.8 | — | — | V | — |
| Output Low level | $V_{OL}$ | $V_{IO}$ = 3.3V<br>$I_{OUTHP}$ = +2mA | -0.2 | — | $V_{IO}$ × 0.2 | V | — |
| **Terminal voltage (ENI2C)** | | | | | | | |
| Output High level | $V_{OH}$ | $V_{IO}$ = 3.3V<br>$I_{ENI2C}$ = -2mA | $V_{IO}$ × 0.8 | — | — | V | — |
| Output Low level | $V_{OL}$ | $V_{IO}$ = 3.3V<br>$I_{ENI2C}$ = +2mA | -0.2 | — | $V_{IO}$ × 0.2 | V | — |
| **LEDCNT** | | | | | | | |
| LED Saturation voltage | $LED_{SAT}$ | $I_{LED}$ = 20mA | — | — | 0.5 | V | — |
| LED Leak current | $LED_{LEAK}$ | LED = 7.5V | — | — | 10 | µA | — |

## ELECRTRICAL CHARACTERISTICS (Continued)

Co = 10 µF, $V_{RECT}$ = 8 V, $T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **I2C bus (Internal I/O characteristics)** | | | | | | | |
| Low-level input voltage | VIL1 | Voltage which is recognized as SDA and SCL Low Level | –0.5 | — | 0.3 × $V_{IO}$ | V | *1 |
| High-level input voltage | VIH1 | Voltage which is recognized as SDA and SCL High Level | 0.7 × $V_{IO}$ | — | $V_{IOmax}$ + 0.5 | V | *1 |
| SDA Low-level output voltage 1 | VOL1 | $V_{IO}$ > 3 V SDA(sink current) = 3 mA | 0 | — | 0.4 | V | |
| SDA Low-level output voltage 2 | VOL2 | $V_{IO}$ < 3 V SDA(sink current) = 3 mA | 0 | — | 0.2 × $V_{IO}$ | V | |
| Input current each I/O pin | IL | SCL, SDA = 0.1 × $V_{IO}$ to 0.9 × $V_{IO}$ | –10 | — | 10 | mA | |
| SCL clock frequency | FOSC | — | 0 | — | 400 | kHz | |

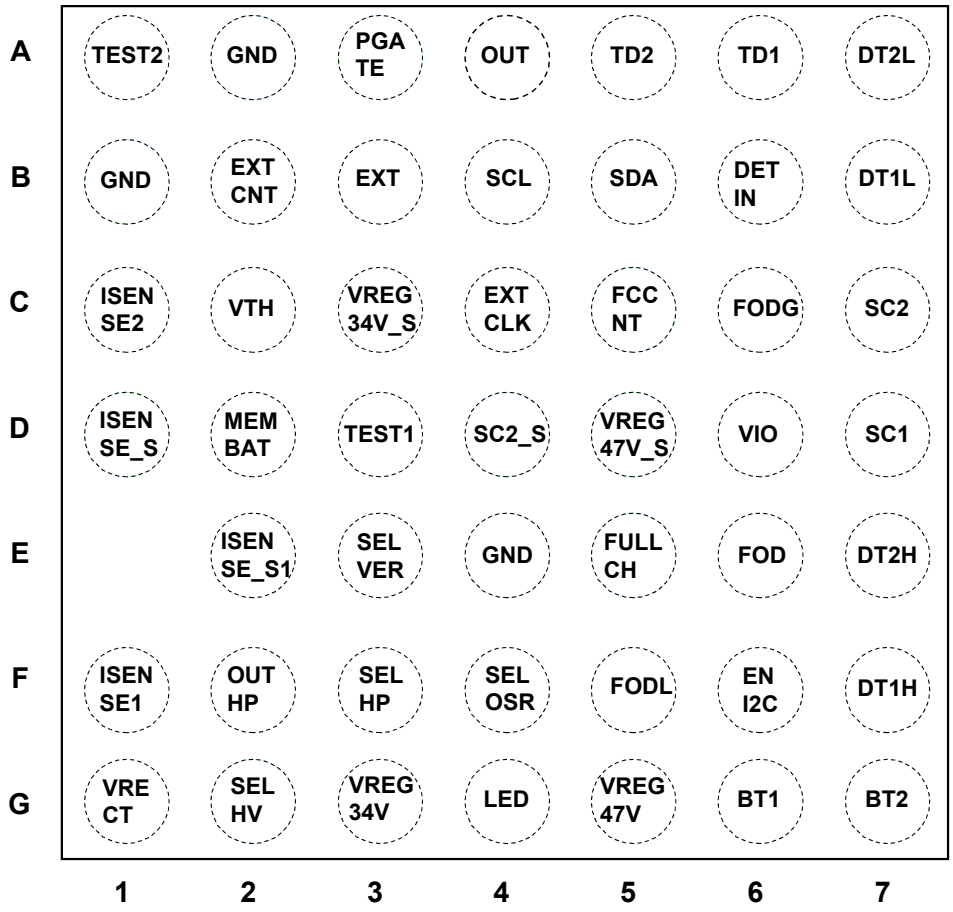
Note) *1 : The input threshold voltage of $I^2C$ bus (Vth) is linked to $V_{IO}$ ($I^2C$ bus I/O stage supply voltage).
In case the pull-up voltage is not $V_{IO}$, the threshold voltage (Vth) is fixed to (($V_{IO}$ / 2) ± (Schmitt width) / 2 ) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value ($V_{ILmax}$).
It is recommended that the pull-up voltage of $I^2C$ bus is set to the $I^2C$ bus I/O stage supply voltage ($V_{IO}$).



Established : 2014-01-15
Revised : ####-##-##

## Pin Layout

Top View



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Revised : ####-##-##

## PIN FUNCTIONS

| Pin | Name | I/O | Function | Description |
|---|---|---|---|---|
| A1 | TEST2 | I | Test pin 2 | Connect to GND. Panasonic uses this pin for test purposes only. |
| A2,B1, E4 | GND | GND | Ground | — |
| A3 | PGATE | O | LDO control | Controls the PMOS gate of the LDO |
| A4 | OUT | I | LDO feedback | Connects to the PMOS drain of the LDO |
| A5 | TD2 | O | Drive load to transmit 2 | Controls capacitive load modulation for Qi data |
| A6 | TD1 | O | Drive load to transmit 1 | Controls capacitive load modulation for Qi data |
| A7 | DT2L | O | Rectification low side switch gate control 2 | Controls the switching gate of the low side of the rectifier |
| B2 | EXTCNT | O | External PMOS control | Controls the switch to an external power supply. This pin is internally connected to the drain of NMOS to use under 2mA.<br>When EXT is larger than 4.2V, EXTCNT will become low and the external MOSFET will turn on. (Refer to the circuit diagram followed by Pin Functions.) |
| B3 | EXT | Power Supply | External power detection | Supplies power externally in direct.<br>When EXT becomes larger than 4.2V, EXTCNT will become low and the wireless power transmission will stop. The external power supply will then directly output, and the Tx will be stopped. (Refer to the circuit diagram followed by Pin Functions.) |
| B4 | SCL | I | I2C clock input | Connect to I2C clock of an MCU. |
| B5 | SDA | I/O | I2C data input / output | Connect to I2C data of an MCU. |
| B6 | DETIN | I | Communication detection | Input the signal from the Rx coil in order to establish communication with Tx of NN32251A to receive power over 5W.<br>Frequency of the power is counted at this pin, and for this to work, input an external clock from EXTCLK. If output is set to 7V (pin SELHV = GND), and frequency is counted, a resistor and a Zener diode need to be connected to this pin.<br>Leave the pin open when the high-power mode and frequency measurement are not needed. |

## PIN FUNCTIONS (Continued)

| Pin | Name | I/O | Function | Description |
|---|---|---|---|---|
| B7 | DT1L | O | Rectification Low side Switch Gate Control 1 | Controls the switching gate of the low side of the rectifier |
| C1 | ISENSE2 | I | Current sensor 2 | Detects the output current from LDO. Connect this pin to ISENSE1-S1(E2) for regular usage. In case of applying high-power mode with NN32251A, a sensing resistor is required. Refer to the circuit diagram followed by Pin Functions. |
| C2 | VTH | I | Thermistor voltage | Connect to a thermistor placed where temperature needs to be measured to prevent over heat. Connect to VREEG34V (G3) if themistors are not in use. |
| C3 | VREG34V_S | O | Internal regulator sense output | This pin is shorted internally to VREG34V(G3). |
| C4 | EXTCLK | I | External clock | Input a reference clock when transmission frequency of the received data at DETIN is measured. Use a clock with frequency from 4MHz to 19MHz. The results can be read from I2C. |
| C5 | FCCNT | I | Full charge control | Connect a pull-down resistor to set an automatic full-charge detecting current. For example, when a resistor of 100kohm is used, decreasing output current to less than 80mA will shutdown the LDO, and also data is sent to Tx to stop power transmission. The current detection starts 5 seconds after power transmission starts. Using this pin can also replace the full-charge control from FULLCH(E5). |

## PIN FUNCTIONS (Continued)

| Pin | Name | I/O | Function | Description |
|---|---|---|---|---|
| C6 | FODG | I | FOD gain control | Connect a pull-down resistor to adjust the gain level of Received Power Packet defined in WPC specification. The resistance can be varied from 10k ohms to 180k ohms. |
| C7 | SC2 | I | Synchronous rectifier control 2 | Connect to the rectifier to detect its voltage level. |
| D1 | ISENSE1_S | I | Sense pin for ISENSE1 | Connect to the source of the LDO's MOSFET to detect the output current. A sense resistor of 50mohms is connected to ISENSE1(F1) inside the IC. In case of applying the solution over 5W (high-power mode) with NN32251A, leave this pin open. Refer to the circuit diagram followed by Pin Functions. |
| D2 | MEMBAT | O | Random number memory adjustment | Connect a capacitor of 1uF to fix a memory time. |
| D3 | TEST1 | O | Test pin 1 | Leave this pin open. Panasonic uses this pin for test purposes only. |
| D4 | SC2_S | I | Synchronous rectifier sense pin | Leave this pin open. Panasonic uses this pin to sense SC2(C7) for test purposes only. |
| D5 | VREG47V_S | O | Internal regulator sense output | This pin in shorted internally to VREG47V(G5). |
| D6 | VIO | Power Supply | I2C power | Apply common power supply of the MCU. The voltage must not exceed 5.5V. |
| D7 | SC1 | I | Synchronous rectifier control 1 | Connect to the rectifier to detect its voltage level. |
| E2 | ISENSE1_S1 | I | Sense pin 1 for ISENSE1 | Connect to ISENSE2(C1) to detect the output current. In case of applying the solution over 5W (high-power mode) with NN32251A, leave this pin open. Refer to the circuit diagram followed by Pin Functions. |
| E3 | SELVER | I | Select a WPC version | Connect to GND to select ver1.1 of WPC Volume1 specification, and connecting to VREG34V(G3) enables to select ver.1.0. |

## PIN FUNCTIONS (Continued)

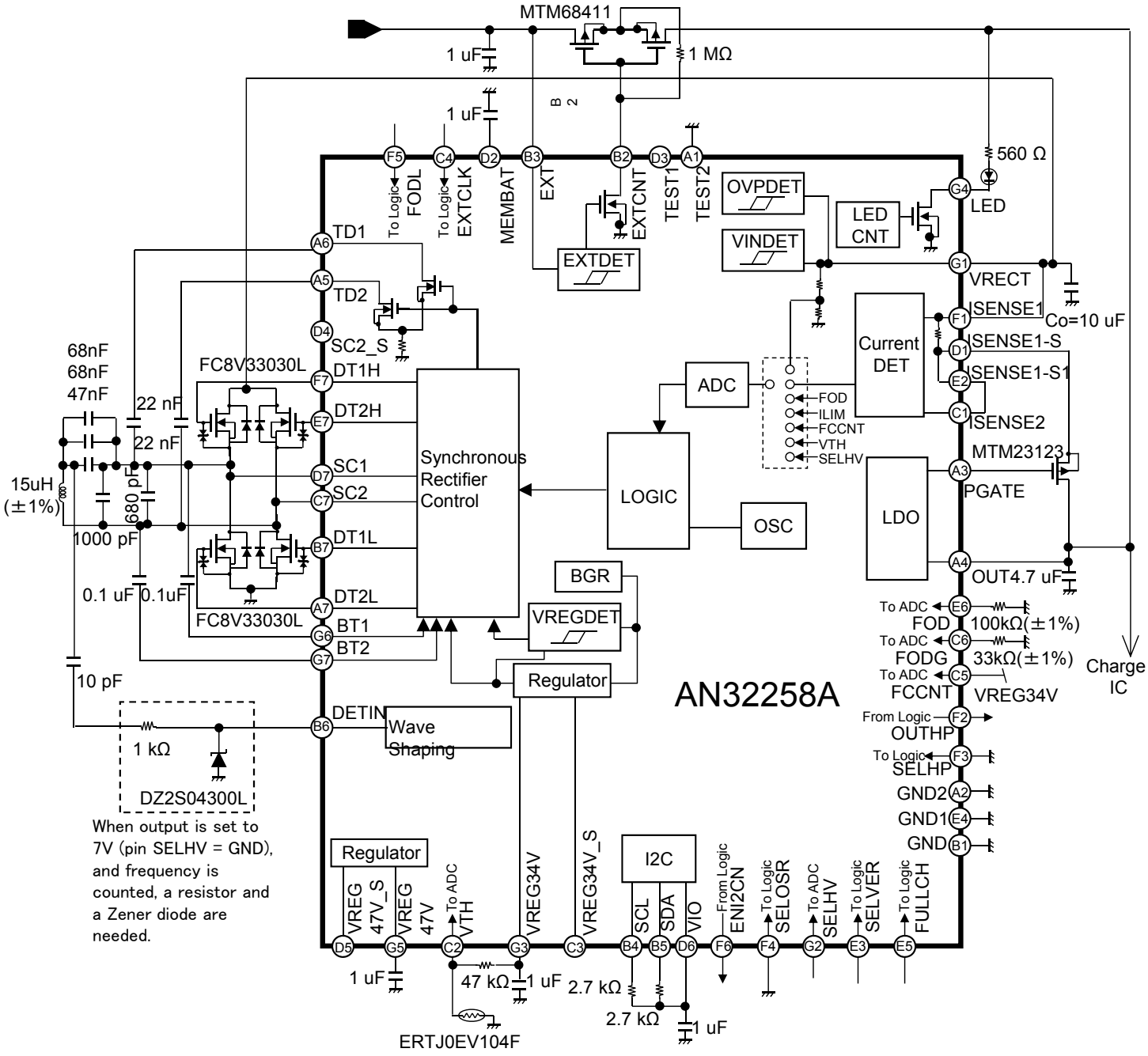
| Pin | Name | I/O | Function | Description |
|---|---|---|---|---|
| E5 | FULLCH | I | Full charge detection | This input controls the full charge detection externally such as from an MCU. When a high voltage level (over 1.6V) is inputted for over 50us, AN32258A will recognize it as full-charge and send packets to Tx to stop the power transmission. Right after the input becomes low, the power transmission can restart. |
| E6 | FOD | O | Foreign object detection offset | Connect a pull-down resistor to adjust the offset level of received power of WPC specification. For example, a pull-down resistor of 100kohm will set the offset to be zero. Refer to No.3 of the Functions section. |
| E7 | DT2H | O | Rectification high side switch gate control 2 | Controls the switching gate of the high side of the rectifier |
| F1 | ISENSE1 | I | Current sensor 1 | Connect to VRECT(G1) to detect the output current. A sense resistor of 50mohms is connected to ISENSE1-S(D1) inside the IC. An external resistor can also be connected. Refer to the circuit diagram followed by Pin Functions. |
| F2 | OUTHP | O | Output high power | Outputs logical high level ( Min. 1.6V ) when SELHP pin is connected to VREG34V. |
| F3 | SELHP | I | Select high-power mode | Connect to GND to output 5W at maximum from LDO. Connecting to VREG34V(G3 ) will activate the high-power output of over 5W ( high-power mode) with using NN32251A for Tx. |
| F4 | SELOSR | I | Select sense resistor | Connect to GND to use the internal sense resistor between ISENSE1(F1) and ISENSE1-S(D1).<br>Connect to VREG34V to use an external sense resistor. When SELHP is set to high-power mode, use an external sense resistor. |

## PIN FUNCTIONS (Continued)

| Pin | Name | I/O | Function | Description |
|---|---|---|---|---|
| F5 | FODL | I | Foreign object detection offset for low current | Inputting a logical high level ( over 1.6V ) will introduce an offset to Received Power Packet when IOUT is small. When GND is inputted, no offset will be added. |
| F6 | ENI2C | O | Enable I2C | Outputs a logical high level from this pin when registers are accessible. |
| F7 | DT1H | O | Rectification high side switch gate control 1 | Controls the switching gate of high side of the rectifier |
| G1 | VRECT | Power Supply | Voltage of rectifier | Voltage of the rectifier output becomes the power supply of AN32258A. |
| G2 | SELHV | I | Select output voltage | Set this pin to select the LDO output as follows;<br>OPEN : 5V<br>GND : 7V |
| G3 | VREG34V | O | Internal regulator output | Outputs a voltage level of 3.4V. |
| G4 | LED | O | LED control | This pin is internally connected to the drain of NMOS which turns on when the LDO outputs a voltage. |
| G5 | VREG47V | O | Internal regulator output | Outputs a voltage level of 4.7V. |
| G6 | BT1 | O | Boot strap 1 | Connect to the rectifier |
| G7 | BT2 | O | Boot strap 2 | Connect to the rectifier |

Panasonic AN32258A

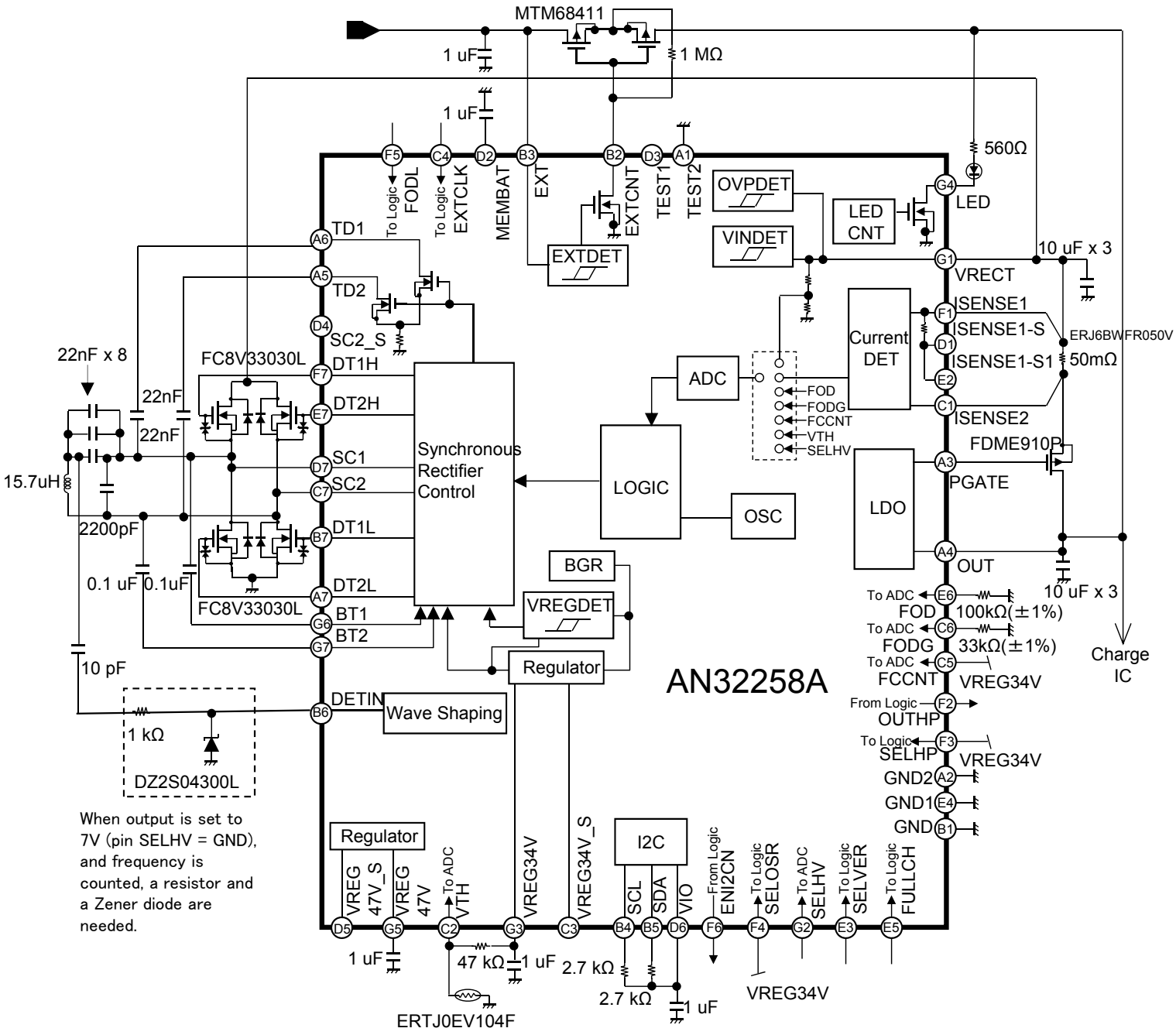
## CIRCUIT DIAGRAM
## (For 5V/5W Output)






Established : 2014-01-15
Revised : ####-##-##

## CIRCUIT DIAGRAM
## (For high-power mode)



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## FUNCTIONS

AN32258A has the following functions.

| No. | Function |
|---|---|
| 1 | Full charge control |
| 2 | Over current control |
| 3 | Foreign object detection |
| 4 | To select output power mode |
| 5 | To select the current sense resistor |
| 6 | Thermal shutdown |
| 7 | To select output voltage |
| 8 | VRECT voltage control |
| 9 | LED display |
| 10 | To select external voltage |
| 11 | Frequency counter of power transmission |
| 12 | To select WPC version |
| 13 | I2C bus interface |
| 14 | Register map |

### 1. Full Charge Control

AN32258A has two ways to detect full-charge.

#### 1-1. Switch ON/OFF externally : FULLCH (Pin E5)

AN32258A recognizes an input of high level to FULLCH as full-charge detected and an input of low level as full-charge not detected. When full-charge is detected, a Qi protocol of End Power Transfer Packet will be sent to Tx. The Tx will then stop the power transmission, and the output of AN32258A will shutdown.
Keep the high level to FULLCH for longer than 50µs for full-charge detection. Change it to low level to restart charging. When this function with FULLCH is not needed, connect the pin to GND.

*Time to resume power transmission depends on the Tx. When NN32251A is used, it will take an hour to restart power transmission after full-charge is detected. Notice that the charge may start and stop repeatedly, if the Tx does not have sufficient time to resume power transmission.

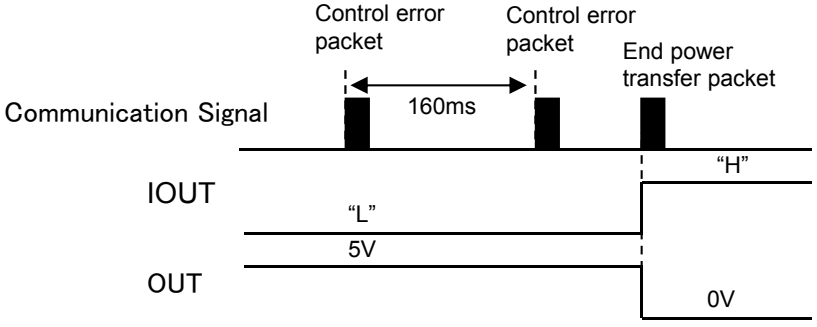



Figure A-1. Full Charge Detection by FULLCH



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

1-2. Control by output current: FCCNT (Pin C5)

When charging current becomes less than the value set at FCCNT (Pin C5), the power transmission stops as full charge. The threshold is determined by a pull-down resistor connected at this pin. For example, when a resistor of 100kohm is used, decreasing output current to less than 80mA will shutdown the LDO, and also data is sent to Tx to stop power transmission. The data to transmit is defined in Qi and called End Power Transfer packet. The current detection starts 5 seconds after power transmission starts.

Connect this pin to VREG34V, when this full-charge detection is not needed. When FULLCH pin is connected to high level to be activated, FCCNT will not control the full-charge detection. This function does not work for FCCNT voltage of over 3V. Also, note that the minimum threshold is 40mA.

*Time to resume power transmission depends on the Tx. When NN32251A is used, it will take an hour to restart power transmission after full-charge is detected. Notice that the charge may start and stop repeatedly, if the Tx does not have sufficient time to resume power transmission.

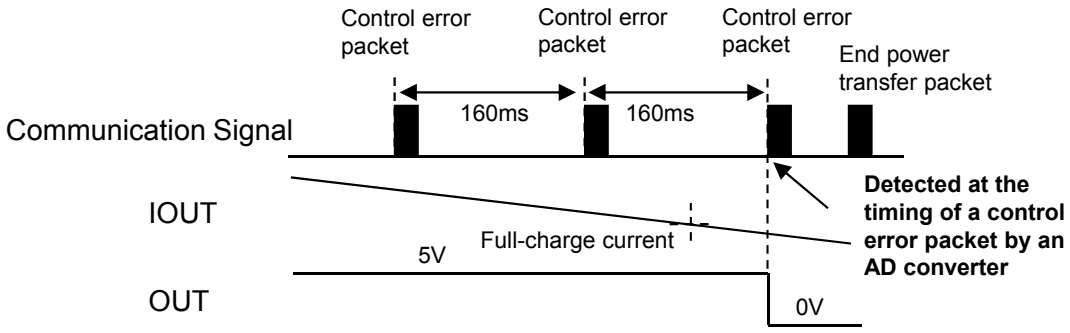
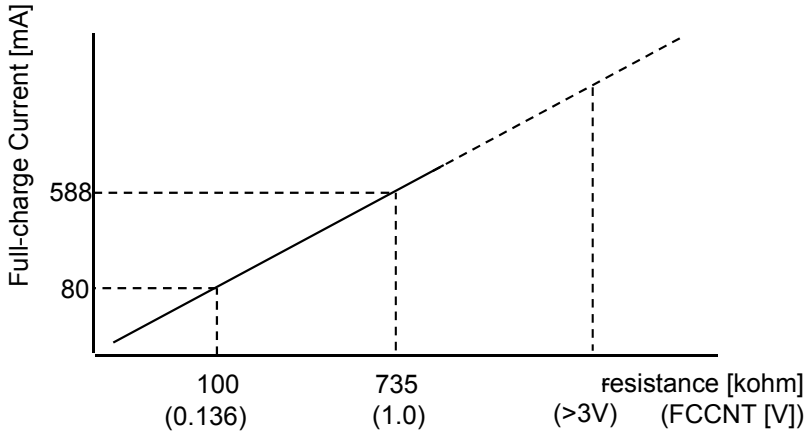



Figure A-2. Full Charge Detection by FCCNT




FigureA-3. Full charge detecting current is controlled by a resistor connected to FCCNT.

Full-charge Current [mA] = 2000/3.4 x 0.00000136 x R[Ω]



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

2.Current Limit Control

When the output current exceeds the threshold value, AN32258A will shutdown the output.

. When this over-current is detected, data is sent to Tx to stop power transmission. The data to transmit to Tx is End Power Transfer packet defined in Qi, and right after the Tx receives the data, it stops its power transmission. The threshold value is about 1.5A for the 5W solution and 2.6A for the high-power solution.

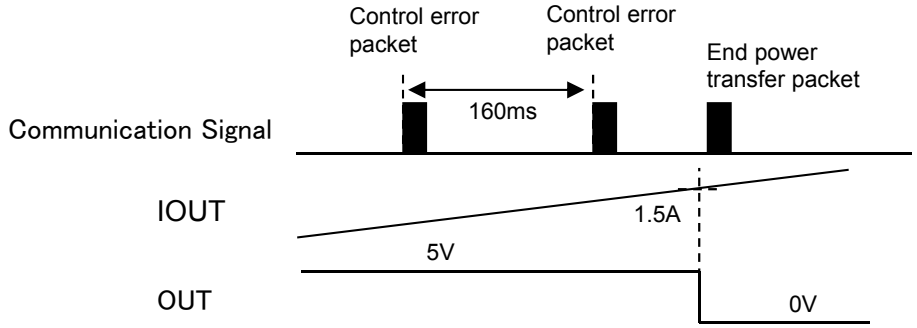



Figure A-4. Timing characteristics for current limit control

3.Foreign Object Detection

AN32258A has a foreign object detection complying with the WPC 1.1 specification. The specification defines a foreign object when the difference between transmitted power and received power is large. The Tx measures the power difference and stops power transmission when the difference is large.

The value of Received Power (address 04h) can be adjusted by the following three pins.

3-1. Offset Control : FOD (Pin E6)

Connect a pull-down resistor at FOD pin to adjust the offset level of received power sent to the Tx.

For example, a pull-down resistor of 100kohm will set the offset to be zero. This function does not work for FOD voltage of over 3V.

If this function is not needed, connect the FOD pin to VREG34V.

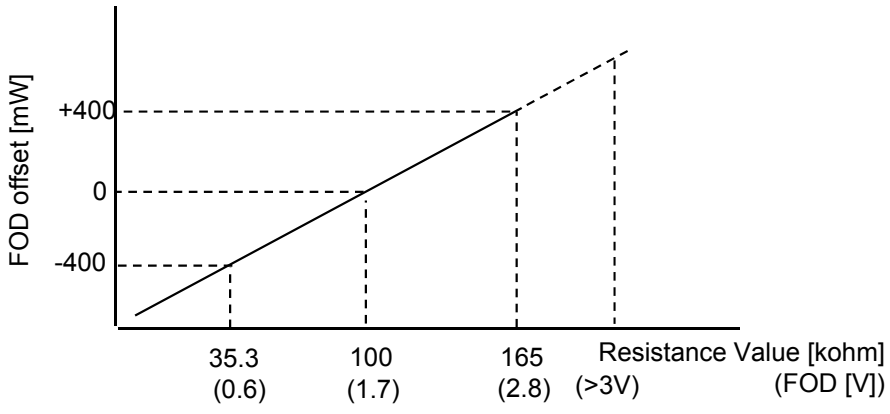



Figure A-5. FOD offset is controlled by a resistor connected to FOD pin



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

3.Foreign Object Detection (Continued)

3-2. Offset Control for low current : FOD (Pin F5)

An offset can be introduced to the received power for low current at IOUT.
Set the FODL pin to either logical high or low.

Low (GND) : No offset
High (over 1.6V) : Offset added (IOUT < ~125mA)

3-3. Gain control : FODG (Pin C6)

The gain of received power can be adjusted by a pull-down resistor connected at this pin. The resistance can be varied from 10k ohms to 180k ohms as the following figure shows.

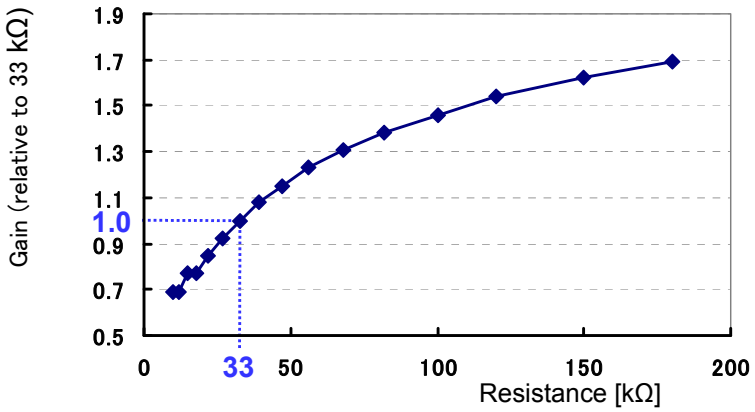



Figure A-5-1. The relationship between received power gain and pull-down resistance at FODG

4.Select High-Power mode : SELHP (Pin F3)

AN32258A can output power of 5W which is WPC 1.1 compliant, but, in addition, the output can be increased over 5W in high-power mode. Connect SELHP pin to GND to output 5W of WPC compliant and to VREG34V to output power over 5W. Note that the Tx must use NN32251A in order for high-power mode to work. If the Tx does not use NN32251A the high-power mode will output WPC compliant 5W.

## FUNCTIONS (Continued)

5. Select Sense Resistor : SELOSR (Pin F4)

Output current is detected by a sense resistor, and AN32258A has internal and external resistors to choose from.
Connect SELOSR pin to GND to use the internal resistor and to VREG34V to use the external resistor.
External components must be routed as the following figure shows.
* In the high-power mode, use an external resistor, otherwise internal heat becomes large.

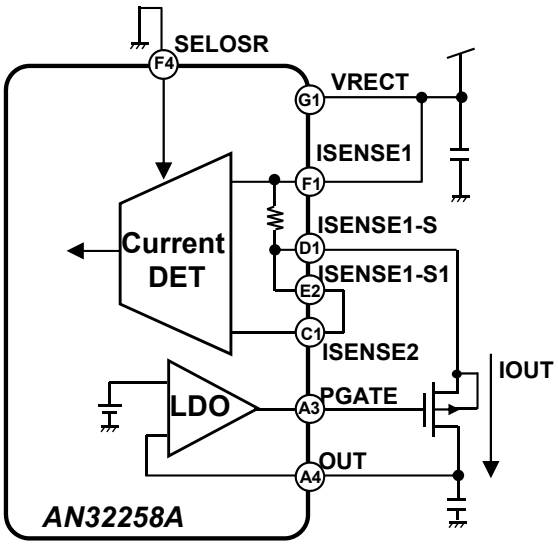



Figure A-6. Circuit when the internal resistor is used. (SELOSR pin is connected to GND)

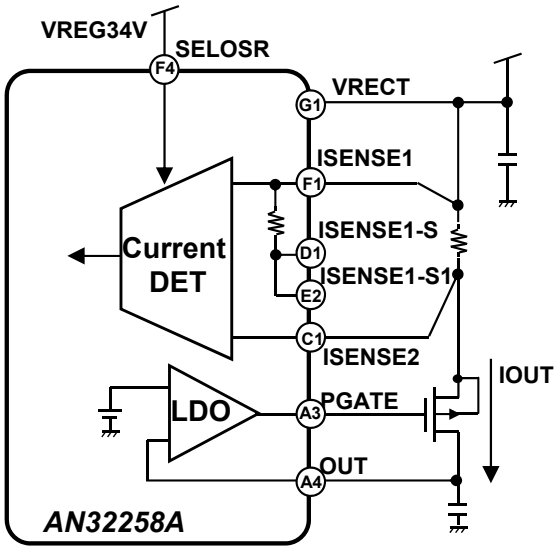



Figure A-7. Circuit when an external resistor is used. (SELOSR pin is connected to VREG34V)

6. Over Temperature Detection : VTH (Pin C2)

A thermistor, ERTJ0EV104F recommended, can be connected to VTH pin. Connecting a resistor from VTH to VREG34V will fix the threshold temperature. For example, a 47kΩ resistor yields a threshold of 60°C.
Refer to TYPICAL CHARACTERISTICS section for more detail.
Connect to VREEG34V (G3) if themistors are not in use.

## FUNCTIONS (Continued)

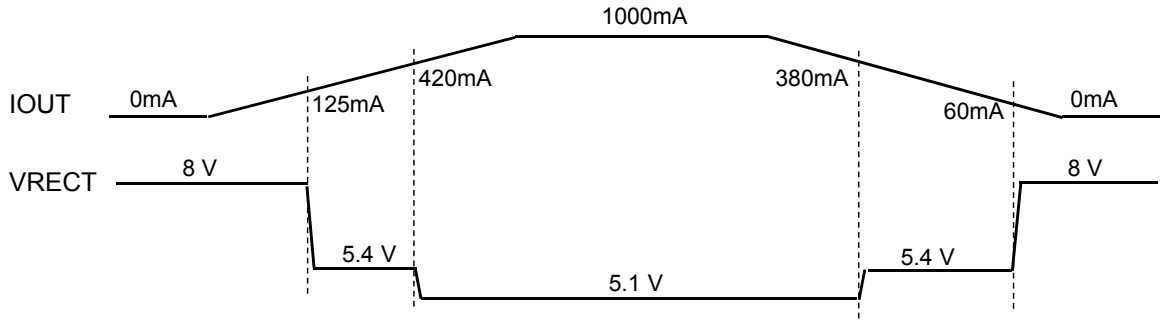
7. Select Output Voltage : SELHV (Pin G2)

The output voltage of AN32258A can be set to either 5V or 7V. When SELHV is open, the output will be 5V, and when SELHV is connected to GND, the output will be 7V. The coils will be different for 5V and 7V solutions.

8. Rectifier Voltage Control

AN32258A controls the rectifier output (VRECT) depending on the current value (IOUT). The following figure shows the change of VRECT due to IOUT. Note that the changed timing in increasing IOUT is different from that in decreasing IOUT.

8-1. OUT = 5V ( SELHV = open )




8-2. OUT=7V ( SELHV = GND )

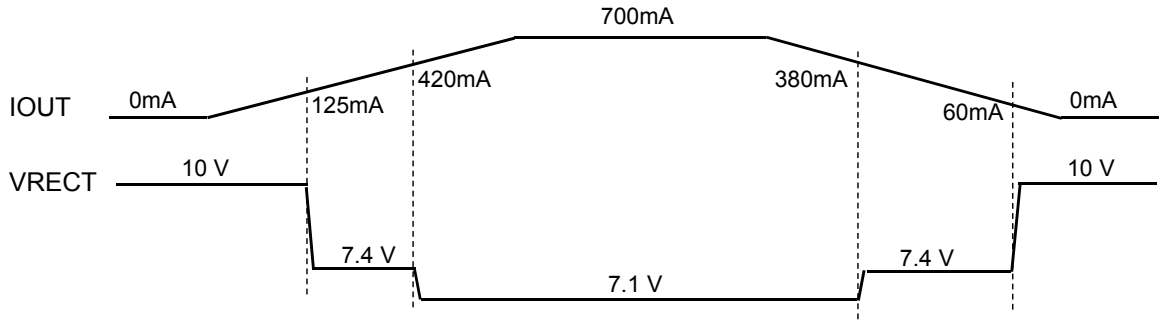



Figure A-8. VRECT changes by the value of output current.
(Values shown are for reference.)



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

9. LED Display：LED (Pin G4)

AN32258A has LED driver. Connect an LED and a resistor in series from OUT to LED pins.
The LED turns on and off as the following figure shows.

Table A-1. LED Display

| Status | Display |
|---|---|
| | LED |
| Standby | OFF |
| Charging | ON |
| Full-charge detected | OFF |
| External power supply detected | OFF |
| Over-current detected | OFF |
| Over-temperature detected | OFF |

10. External Voltage Supply Switch：EXT ( Pin B3 )、EXTCNT (Pin B2)

The voltage supply to a charger can be switched from AN32258A to some external voltage supply, such as USB. For this function to work, introduce an external voltage to EXT pin. When EXT becomes larger than 4.2V, the external MOSFET switch will turn on to output the external voltage in direct. Also, End Power Transfer Packet is sent to Tx to stop power transmission at the same time.
If the external voltage supply becomes lower than 3.8V, the external MOSFET switch will turn off. Then, Tx will resume power transmission, and AN32258A will start to output at the LDO. Refer to the circuit diagram before FUNCTIONS section for the configuration at EXT pin.

11. Power Frequency Detection：EXTCLK (Pin C4)

The frequency of received power is measured with a 4MHz to 19MHz clock inputted to EXTCLK pin. A measurement starts 3ms after the register at 0Ah is set to 01h. The results will be written into the register 09h, FREQCNT[7:0], and they can be read from I2C bus.

Frequency = Fextclk / FREQCNT[7:0]

If output is set to 7V (pin SELHV = GND), and frequency is counted, a resistor and a Zener diode need to be connected to DETIN (Pin B6).

12. Select WPC Version：SELVER (Pin E3)

Connect SELVER pin to GND to select ver1.1 of WPC Volume1 specification, and connecting to VREG34V(G3) enables to select ver.1.0. Note that ver. 1.0 of WPC will not be certified by the organization any more.

## FUNCTIONS (Continued)

13. I2C-bus interface

13-1. Basic Rules

・This IC, I2C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode(400 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the HS-mode (to 3.4 Mbps).

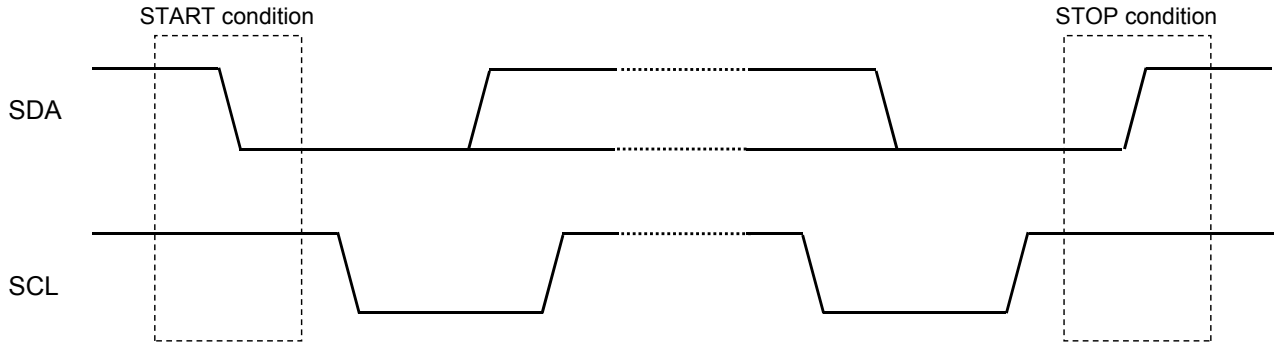
・This IC will be operated as a slave device in the I2C-bus system. This IC will not operate as a master device.

・The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm our company if it will be used in these mode systems.

・The I2C is the brand of NXP.

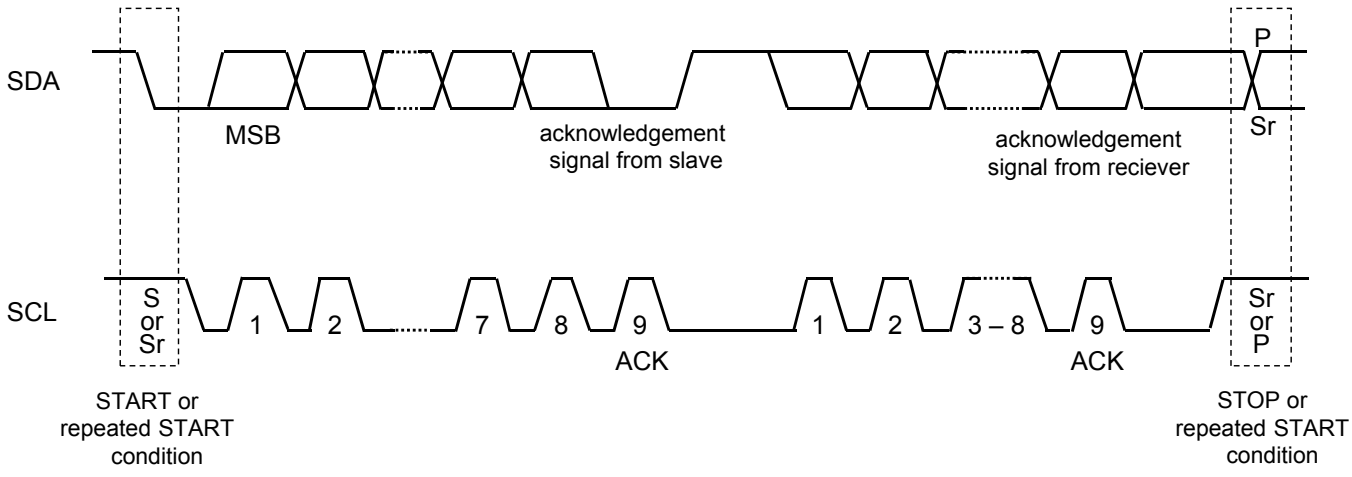
13-2. START and STOP conditions

A High to Low transition on the SDA line while SCLK is High is one such unique case. This situation indicates START condition. A Low to High transition on the SDA line while SCLK is High defines STOP condition.
START and STOP conditions are always generated by the master. After START condition occur, the bus will be busy.
The bus is considered to be free again a certain time after the STOP condition.




13-3. Transferring Data

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.






Established : 2014-01-15
Revised : ####-##-##

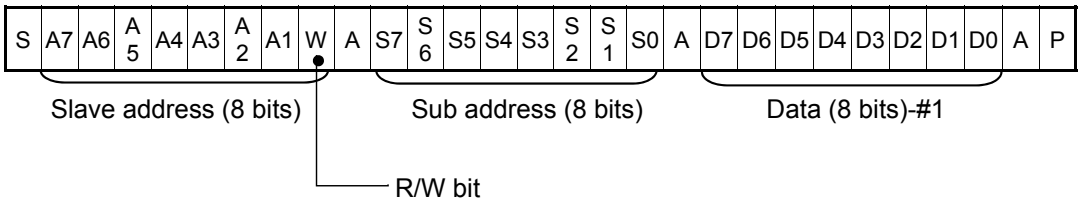
## FUNCTIONS (Continued)

13. I2C-bus interface (continued)

13-4. Data format

13-4-1. Write mode

A) Write mode

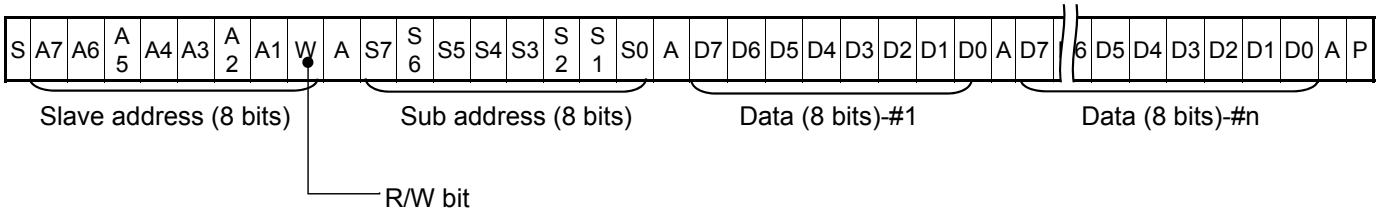



・LSB of slave address (8 bits) is definition bit for read/write. (This is I2C-bus specification.)

・Slave address

| A7 | A6 | A5 | A4 | A3 | A2 | A1 |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |

B) Auto increment mode




Auto increment mode : Master device writes to slave n-times while slave increments write address start from sub address. (n ≥ 1)

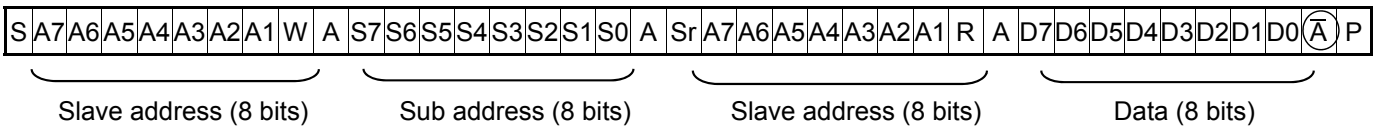
| | |
|---|---|
| S | START condition |
| P | STOP condition |
| A | Acknowledge (Slave -> Master) |



Established : 2014-01-15
Revised : ####-##-##

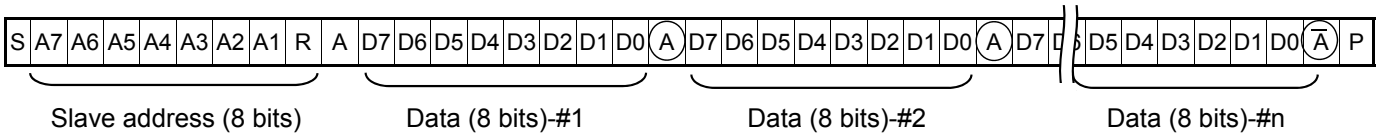
## FUNCTIONS (Continued)

13. I2C-bus inter face (continued)
13-4. Data format (continued)
13-4-2. Read mode
A) Random mode




・Random mode: Master device reads data in the address which sub address indicates.
・LSB of slave address (8 bits) is definition bit for read/write. (This is I2C bus specification.)

B) Sequential mode




・Sequential mode: Master device reads n-times while slave device increments write address. (n ≥ 1)
・In this example, sub address is omitted. Slave device has address pointer, and increments this pointer.
・LSB of slave address (8 bits) is definition bit for read/write. (This is I2C bus specification.)

| | |
|---|---|
| S | START condition |
| P | STOP condition |
| Sr | Repeated START condition |
| A | Acknowledge (Slave -> Master) |
| Ⓐ | Acknowledge (Master -> Slave) |
| Ⓐ̄ | Not acknowledge (Master -> Slave) |



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

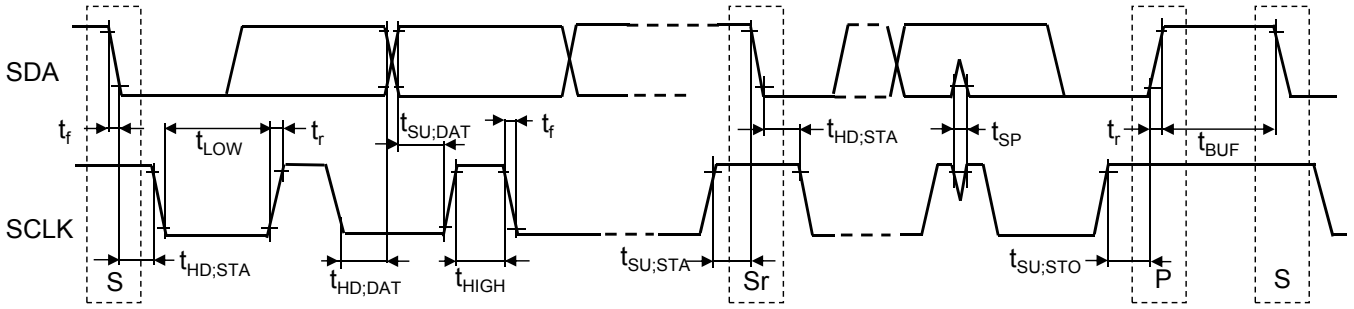
Co = 10 µF, $V_{RECT}$ = 8 V, $T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **I2C bus (I/O specifications)** | | | | | | | |
| Hysteresis of Schmitt trigger input 1 | Vhys1 | VIO > 2 V, Hysteresis 1 of SDA, SCLK | 0.05 × $V_{IO}$ | — | — | V | *1,2 |
| Hysteresis of Schmitt trigger input 2 | Vhys2 | VIO < 2 V, Hysteresis 2 of SDA, SCLK | 0.1 × $V_{IO}$ | — | — | V | *1,2 |
| Output fall time from VIHmin to VILmax | Tof | Bus capacitance : 10 pF to 400 pF<br>$I_P \leq 6$ mA ($V_{OLmax}$ = 0.6 V)<br>$I_P$ : Max. sink current | 20 + 0.1 × $C_b$ | — | 250 | ns | *1,2 |
| Pulse width of spikes which must be suppressed by the input filter | tsp | — | 0 | — | 50 | ns | *1,2 |
| Capacitance for each I/O pin | Ci | — | — | — | 10 | pF | *1,2 |

Note)

*1: Designed values, but not tested in shipping inspection

*2 : The timing of Fast-mode devices in I2C-bus is specified as the following.
All values referred to VIHmin and VILmax level.




S : START condition
Sr : Repeated START condition
P : STOP condition



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

Co = 10 µF, $V_{RECT}$ = 8 V, $T_a$ = 25 °C ± 2 °C unless otherwise noted.

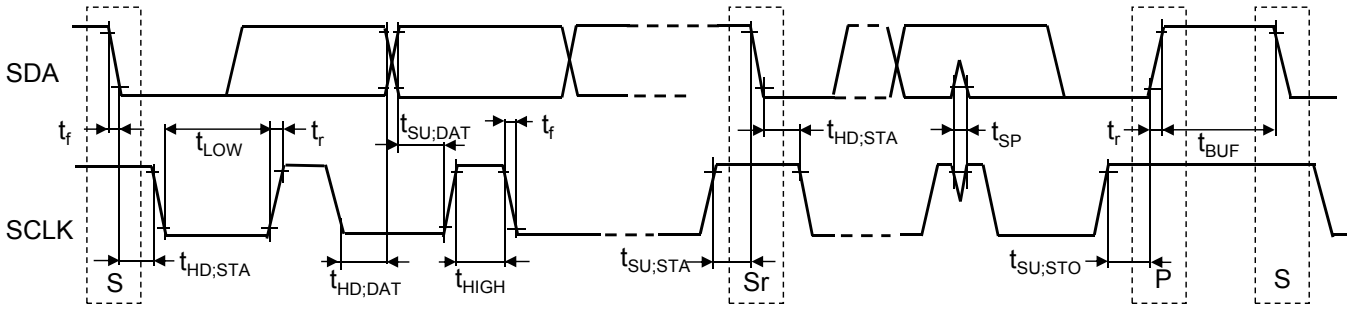
| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **I2C bus (Bus line specifications)** | | | | | | | |
| Hold time (repeated) START condition | $t_{HD:STA}$ | The first clock pulse is generated after tHD:STA. | 0.6 | — | — | ms | *1,2 |
| Low period of the SCLK clock | $t_{LOW}$ | — | 1.3 | — | — | ms | *1,2 |
| High period of the SCLK clock | $t_{HIGH}$ | — | 0.6 | — | — | ms | *1,2 |
| Set-up time for a repeat START condition | $t_{SU:STA}$ | — | 0.6 | — | — | ms | *1,2 |
| Data hold time | $t_{HD:DAT}$ | — | 0 | — | 0.9 | ms | *1,2 |
| Data set-up time | $t_{SU:DAT}$ | — | 100 | — | — | ns | *1,2 |
| Rise time of both SDA and SCLK signals | $t_r$ | — | 20 + 0.1 □ $C_b$ | — | 300 | ns | *1,2 |
| Fall time of both SDA and SCLK signals | $t_f$ | — | 20 + 0.1 □ $C_b$ | — | 300 | ns | *1,2 |
| Set-up time of STOP condition | $t_{SU:STO}$ | — | 0.6 | — | — | ms | *1,2 |
| Bus free time between STOP and START condition | $t_{BUF}$ | — | 1.3 | — | — | ms | *1,2 |

Note)

*1: Designed values, but not tested in shipping inspection

*2 : The timing of Fast-mode devices in I2C-bus is specified as the following.

All values referred to VIHmin and VILmax level.




S : START condition

Sr : Repeated START condition

P : STOP condition



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

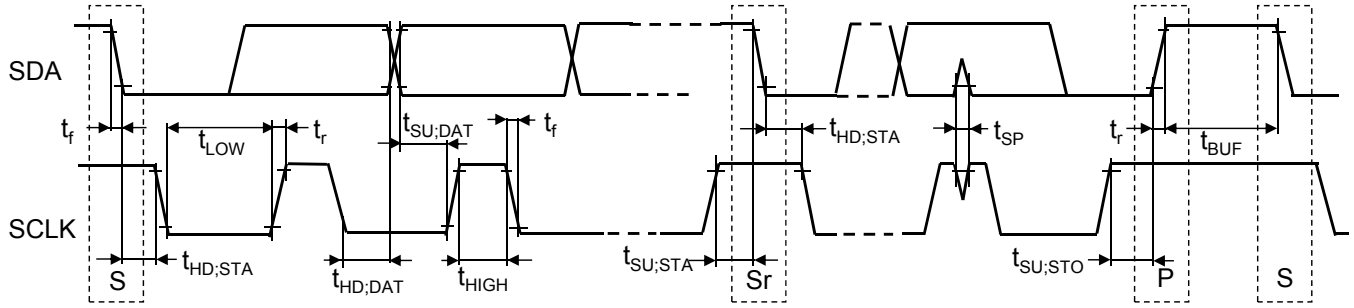
Co = 10 µF, $V_{RECT}$ = 8 V, $T_a$ = 25 °C ± 2 °C unless otherwise noted.

| Parameter | Symbol | Condition | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **I2C bus (Bus line specifications) (continued)** | | | | | | | |
| Capacitive load for each bus line | $C_b$ | — | — | — | 400 | pF | *1,2 |
| Noise margin at the Low-level for each connected device | $V_{nL}$ | — | 0.1 × $V_{IO}$ | — | — | V | *1,2 |
| Noise margin at the High-level for each connected device | $V_{nH}$ | — | 0.2 × $V_{IO}$ | — | — | V | *1,2 |

Note)

*1: Designed values, but not tested in shipping inspection

*2: The timing of Fast-mode devices in I2C-bus is specified as the following.
All values referred to VIHmin and VILmax level.




S : START condition
Sr : Repeated START condition
P : STOP condition



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

14. Register Map

Normal mode

| Address | R/W | RESET factor | attribute | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h | R | NRESET | SIGNALSTR | SSV[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h | R | NRESET | EPTP | EPTP[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 03h | R | NRESET | CONTROL ERROR | CERR[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04h | R | NRESET | RECEIVED POWER | RPWR[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20h | R/W | NRESET | CONTROL POINT A | CTLPOINTA[7:0] | | | | | | | |
| Initial | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 21h | R/W | NRESET | CONTROL POINT B | CTLPOINTB[7:0] | | | | | | | |
| Initial | | | | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 22h | R/W | NRESET | CONTROL POINT C | CTLPOINTC[7:0] | | | | | | | |
| Initial | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 23h | R/W | NRESET | CURRENT THRESH 1A | THRESH1A[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 24h | R/W | NRESET | CURRENT THRESH 1B | THRESH1B[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 25h | R/W | NRESET | CURRENT THRESH 2A | THRESH2A[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 26h | R/W | NRESET | CURRENT THRESH 2B | THRESH2B[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 27h | W | NRESET | TXEPTP | — | — | — | — | — | — | — | TXEPTP |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 40h | R/W | NRESET | USER MODE SELECT | — | — | — | — | — | — | — | PRIVILEGE |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 71h | R | NRESET | ID1 | MAJOR VER[3:0] | | | | MINOR VER[3:0] | | | |
| Initial | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 72h | R | NRESET | ID2 | MANUFACTURE CODE[15:8] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 73h | R | NRESET | ID3 | MANUFACTURE CODE[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 74h | R | NRESET | ID4 | EXTID | BASIC DEVICE ID[30:24] | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 75h | R | NRESET | ID5 | BASIC DEVICE ID[23:9] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 76h | R | NRESET | ID6 | BASIC DEVICE ID[15:8] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 77h | R | NRESET | ID7 | BASIC DEVICE ID[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 80h | R | NRESET | CHARGE MODE | — | — | — | — | — | — | — | HPMODE |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## FUNCTIONS (Continued)

14. Register Map (Continued)

Privilege registers

| Address | R/W | RESET factor | attribute | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 03h | R/W | PRIVILEGE | CONTROL ERROR | CERR7 | CERR6 | CERR5 | CERR4 | CERR3 | CERR2 | CERR1 | CERR0 |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04h | R/W | PRIVILEGE | RECEIVED POWER | RPWR7 | RPWR6 | RPWR5 | RPWR4 | RPWR3 | RPWR2 | RPWR1 | RPWR0 |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05h | R/W | PRIVILEGE | CHARGE STATUS | CHGSTATUS[7:0] | | | | | | | |
| Initial | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 07h | R | PRIVILEGE | VADC | VADC7 | VADC6 | VADC5 | VADC4 | VADC3 | VADC2 | VADC1 | VADC0 |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08h | R | PRIVILEGE | IADC | IADC7 | IADC6 | IADC5 | IADC4 | IADC3 | IADC2 | IADC1 | IADC0 |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09h | R | PRIVILEGE | FREQCNT | FREQCNT[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0Ah | R/W | PRIVILEGE | EXTCLK ENABLE | — | — | — | — | — | — | — | EXTCLKEN |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 30h | R/W | PRIVILEGE | CTLP HP VRECA | HPCTLPOINTA[7:0] | | | | | | | |
| Initial | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 31h | R/W | PRIVILEGE | CTLP HP VRECB | HPCTLPOINTB[7:0] | | | | | | | |
| Initial | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 32h | R/W | PRIVILEGE | CTLP HP VRECC | HPCTLPOINTC[7:0] | | | | | | | |
| Initial | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 33h | R/W | PRIVILEGE | CTLP KEY | — | — | — | — | — | — | — | CTLPKEY |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 41h | R/W | PRIVILEGE | FUNCTION SET | — | — | — | — | — | — | SETRPWR | SETCE |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 43h | R/W | NRESET | POWER PARAMETER 2 | KB[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 44h | R/W | NRESET | POWER PARAMETER 3 | KC[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 45h | R/W | NRESET | POWER OFFSET | OFFSET[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 51h | R | PRIVILEGE | CONFIG1 | PWR CLASS1 | PWR CLASS0 | MAXPWR5 | MAXPWR4 | MAXPWR3 | MAXPWR2 | MAXPWR1 | MAXPWR0 |
| Initial | | | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 53h | R/W | PRIVILEGE | CONFIG3 | — | — | — | — | — | COUNT2 | COUNT1 | COUNT0 |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 54h | R/W | PRIVILEGE | CONFIG4 | WINDOW SIZE | | | | | WINDOW OFFSET | | |
| Initial | | | | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 60h | W | AUTORST | OPTREQ | — | — | — | — | — | — | — | OPTREQ |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 61h | R/W | PRIVILEGE | OPTCNT | — | — | — | OPTCNT4 | OPTCNT3 | OPTCNT2 | OPTCNT1 | OPTCNT0 |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 62h | R/W | PRIVILEGE | OPTADR | OPTADR[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 63h | R/W | PRIVILEGE | OPTDATA1 | OPTDATA1[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 64h | R/W | PRIVILEGE | OPTDATA2 | OPTDATA2[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 65h | R/W | PRIVILEGE | OPTDATA3 | OPTDATA3[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 66h | R/W | PRIVILEGE | OPTDATA4 | OPTDATA4[7:0] | | | | | | | |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 67h | R | PRIVILEGE | OPTDATTX | — | — | — | — | OPT4TXWAIT | OPT3TXWAIT | OPT2TXWAIT | OPT1TXWAIT |
| Initial | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 71h | R/W | PRIVILEGE | ID1 | MAJOR VER3 | MAJOR VER2 | MAJOR VER1 | MAJOR VER0 | MINOR VER | MINOR VER | MINOR VER | MINOR VER |
| Initial | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

14. Register Map (Continued)

| Register Name | | SIGNALSTR | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01h | R | SSV7 | SSV6 | SSV5 | SSV4 | SSV3 | SSV2 | SSV1 | SSV0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0：Signal Strength Value (0-255)

It shows the coupling of a transmitter coil and a receiver coil.

AN32258A shows the rate to the maximum of rectification voltage.

Signal Strength Value = VRECT Voltage / 20 ×255

| Register Name | | EPTP | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02h | R | EPTP7 | EPTP6 | EPTP5 | EPTP4 | EPTP3 | EPTP2 | EPTP1 | EPTP0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0： End Power Transfer packet

The message contained in a "End Power Transfer packet" is shown.

0x00：EXT input detection

0x01：Full charge

0x02：Internal Fault ** This can be set by writing 01h to register 27h.

0x03：Over temperature detection

0x04：Over voltage detection

0x05：Over current detection

| Register Name | | CONTROLERROR | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03h | R | CERR7 | CERR6 | CERR5 | CERR4 | CERR3 | CERR2 | CERR1 | CERR0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0：Control Error Value (-128 - +127)

The contents of Control Error packet are shown.

It is a signed integer of -128 to +127 in the complement form of 2.

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

| Register Name | | RECEIVEDPOWER | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04h | R | RPWR7 | RPWR6 | RPWR5 | RPWR4 | RPWR3 | RPWR2 | RPWR1 | RPWR0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0：Received Power Value(0-255)

This register shows the average of total power in received side within the time range of defined configuration packet.

It is an unsigned integer of 0 to 255.

Receiving Power's total amount is calculated below.

Received Power = (RPWR[7:0] / 128) × (Maximum Power / 2) ×$10^{\text{Power Class}}$ W

* The Configuration packet defines Maximum Power and Power Class.

| Register Name | | CONTROLPOINT A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 20h | R/W | CTLPOINTA7 | CTLPOINTA6 | CTLPOINTA5 | CTLPOINTA4 | CTLPOINTA3 | CTLPOINTA2 | CTLPOINTA1 | CTLPOINTA0 |
| Default | 66h | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

D7-D0：Control Point A(0-255)

The target value of VRECT voltage when current is less than 125mA is shown.

VRECT voltage is calculated below.

VRECT voltage = CTLPOINTA[7:0] / 255×20 V

*Initial value ：8.0 V

| Register Name | | CONTROLPOINT B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 21h | R/W | CTLPOINTB7 | CTLPOINTB6 | CTLPOINTB5 | CTLPOINTB4 | CTLPOINTB3 | CTLPOINTB2 | CTLPOINTB1 | CTLPOINTB0 |
| Default | 45h | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |

D7-D0：Control Point B(0-255)

The target value of VRECT voltage in case current is settled in the range of 125mA to 420mA is shown.

VRECT voltage is calculated below.

VRECT voltage = CTLPOINTB[7:0] / 255×20 V

* Initial value ：5.4 V

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

| Register Name | | CONTROLPOINT C | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 22h | R/W | CTLPOINT C7 | CTLPOINT C6 | CTLPOINT C5 | CTLPOINT C4 | CTLPOINT C3 | CTLPOINT C2 | CTLPOINT C1 | CTLPOINT C0 |
| Default | 41h | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

D7-D0：Control Point C(0-255)

The target value of VRECT voltage in case current is more than 420mA is shown.

VRECT voltage is calculated below.

VRECT voltage = CTLPOINTC[7:0] / 255×20 V

*Initial value：5.1 V

| Register Name | | CURRENTTHRESH 1A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 23h | R/W | THRESH1 A7 | THRESH1 A6 | THRESH1 A5 | THRESH1 A4 | THRESH1 A3 | THRESH1 A2 | THRESH1 A1 | THRESH1 A0 |
| Default | 10h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

D7-D0：Current thresh 1A(0-255)

It is a setting register of a Control Point A/B switch current threshold value (higher).

A current threshold value is calculated below.

Current threshold = THRESH1A[7:0] / 255×2 A

* Initial value ：125mA

| Register Name | | CURRENTTHRESH 1B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 24h | R/W | THRESH1 B7 | THRESH1 B6 | THRESH1 B5 | THRESH1 B4 | THRESH1 B3 | THRESH1 B2 | THRESH1 B1 | THRESH1 B0 |
| Default | 08h | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

D7-D0：Current thresh 1B(0-255)

It is a setting register of a Control Point A/B switch current threshold value (lower).

A current threshold value is calculated below.

Current threshold = THRESH1B[7:0] / 255×2 A

* Initial value ：60mA

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

| Register Name | | CURRENTTHRESH 2A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 25h | R/W | THRESH2A7 | THRESH2A6 | THRESH2A5 | THRESH2A4 | THRESH2A3 | THRESH2A2 | THRESH2A1 | THRESH2A0 |
| Default | 36h | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

D7-D0：Current thresh 2A(0-255)

It is a setting register of a Control Point B/C switch current threshold value (higher).

A current threshold value is calculated below.

Current threshold = THRESH2A[7:0] / 255×2 A

* Initial value：420mA

| Register Name | | CURRENTTHRESH 2B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 26h | R/W | THRESH2B7 | THRESH2B6 | THRESH2B5 | THRESH2B4 | THRESH2B3 | THRESH2B2 | THRESH2B1 | THRESH2B0 |
| Default | 30h | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

D7-D0：Current thresh 2B(0-255)

It is a setting register of a Control Point B/C switch current threshold value (lower).

A current threshold value is calculated below.

Current threshold = THRESH2B[7:0] / 255×2 A

* Initial value：380mA

| Register Name | | TXEPTP | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 27h | W | - | - | - | - | - | - | - | TXEPTP |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0：TXEPTP

It is a compulsive transmitting register of an End Power Transfer packet.

0：Normal operation (default)

1：End Power Transfer packet transmission

* After transmitting End Power Transfer packet, a Transmitter side will be in a power-off state, and this register returns to a default value by resetting this IC.

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

| Register Name | | USER MORE SELECT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 40h | R/W | - | - | - | - | - | - | - | PRIVILEGE |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0：PRIVILEGE

This register controls the access to privilege register.

0：Normal register map access only.（default)

1：Access to privilege register and normal register.

| Register Name | | ID1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 71h | R | MAJOR VER[3:0] | | | | MINOR VER[3:0] | | | |
| Default | 00h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

D7-D4：MAJOR VER[3:0]

Major Version of Volume I of the System Description Wireless Power Transfer of the WPC standard to which this IC corresponds is shown.

0001：Major Version (default)

D3-D0：MINOR VER[3:0]

Minor Version of Volume I of the System Description Wireless Power Transfer of the WPC standard to which this IC corresponds is shown.

0001：Minor Version (default)

| Register Name | | ID2 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 72h | R | MANUFACTURE CODE[15:8] | | | | | | | |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Register Name | | ID3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 73h | R | MANUFACTURE CODE[7:0] | | | | | | | |
| Default | 25h | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |

REGISTER 72h-73h[7:0] ：MANUFACTURE CODE

Manufacture Code of Panasonic is shown.

0025： Manufacture Code of Panasonic (default)

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

| Register Name | | ID 4 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 74h | R | EXTID | BASIC DEVICE ID[30:24] | | | | | | |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Register Name | | ID 5 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 75h | R | BASIC DEVICE ID[23:16] | | | | | | | |
| Default | 0Xh | 0 | 0 | 0 | 0 | X | X | X | X |

| Register Name | | ID6 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 76h | R | BASIC DEVICE ID[15:8] | | | | | | | |
| Default | XXh | X | X | X | X | X | X | X | X |

| Register Name | | ID7 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 77h | R | BASIC DEVICE ID[7:0] | | | | | | | |
| Default | XXh | X | X | X | X | X | X | X | X |

REGISTER 74h[7] : Extended ID

The identification bit sequence of this IC is chosen.

0 : Manufacturer Code || Basic Device ID (default)

1 : Manufacturer Code || Basic Device ID || Extended Device Identifier

REGISTER 74h-77h Basic Device ID[30:0]

Basic Device ID of this IC is shown.

A random number is set to BASIC DEVICE ID [19:0].

| Register Name | | CHRGE MODE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 80h | R | - | - | - | - | - | - | - | HPMODE |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 : High Power MODE

It is a register which shows the High Power mode.

By setup of SELHP=H, when the Transmitter side corresponds (NN32251A), it becomes “H”.

0 : 5W mode (default)

1 : High Power mode

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

| Register Name | | CONTROLERROR | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 03h | R/W | CERR7 | CERR6 | CERR5 | CERR4 | CERR3 | CERR2 | CERR1 | CERR0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0：Control Error Value (-128 - +127)

The contents of the Control Error packet are shown.

It is a signed integer of -128 to +127 in the complement form of 2.

By set up SETCE（Address41h, bit0）="H", the Control Error value written in this address is transmit.

| Register Name | | RECEIVEDPOWER | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04h | R/W | RPWR7 | RPWR6 | RPWR5 | RPWR4 | RPWR3 | RPWR2 | RPWR1 | RPWR0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0：Received Power Value(0-255)

This register shows the average of total power in received side within the time range of defined configuration packet.

It is an unsigned integer of 0 to 255.

The total amount of receiving power is calculated below.

Received Power = (RPWR[7:0] / 128) × (Maximum Power / 2) $\times 10^{\text{Power Class}}$ W

By set up SETRPWR（Address41h, bit1）="H", the Received Power value written in this address is transmit.

* The Configuration packet defines Maximum Power and Power Class.

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

| Register Name | | CHARGE STATUS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 05h | R/W | CHGSTATUS7 | CHGSTATUS6 | CHGSTATUS5 | CHGSTATUS4 | CHGSTATUS3 | CHGSTATUS2 | CHGSTATUS1 | CHGSTATUS0 |
| Default | FFh | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

D7-D0 : Charge Status Value(0-100, 255)

The rate to a full charge level is shown.

00000000 : Battery Empty

:

01100100 : Full charge

11111111 : Charge information cannot be given. (default)

* Writing other values is prohibited.

| Register Name | | VADC | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 07h | R | VADC7 | VADC6 | VADC5 | VADC4 | VADC3 | VADC2 | VADC1 | VADC0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0 : VRECT Value (0 - +255)

The voltage level of VRECT is shown.

It is set to VADC[7:0] = FFh at the time of VRECT = 20V.

| Register Name | | IADC | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 08h | R | IADC7 | IADC6 | IADC5 | IADC4 | IADC3 | IADC2 | IADC1 | IADC0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0 : ISENSE Value (0 - +255)

The current level of ISENSE is shown.

It is set to IADC[7:0] = FFh at the time of ISENSE current = 2A.

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | FREQCNT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 09h | R | FREQCNT 7 | FREQCNT 6 | FREQCNT 5 | FREQCNT 4 | FREQCNT 3 | FREQCNT 2 | FREQCNT 1 | FREQCNT 0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D7-D0：Coil Frequency (0-100, 255)

The value (average of 256 cycles) which counted the coil frequency Fcoil with the EXTCLK_IN clock is shown.

If frequency of EXTCLK_IN is made into Fext Hz, the coil frequency Fcoil will be calculated below.

Fcoil = Fext / FREQCNT[7:0] Hz

| Register Name | | EXTCLK ENABLE | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0Ah | R | - | - | - | - | - | - | - | EXTCLKEN |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0：EXTCLKEN

It is the clock input enabling register from EXTCLK_IN.

0：EXTCLK_IN is invalid （default)

1：EXTCLK_IN is effective

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | CTLP HP VREC A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 30h | R/W | HPCTLPOINTA7 | HPCTLPOINTA6 | HPCTLPOINTA5 | HPCTLPOINTA4 | HPCTLPOINTA3 | HPCTLPOINTA2 | HPCTLPOINTA1 | HPCTLPOINTA0 |
| Default | 66h | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

D7-D0：High Power Control Point A(0-255)

The target value of VRECT voltage for the current less than 125mA at High Power mode is shown.

VRECT voltage is calculated below.

VRECT voltage = HPCTLPOINTA[7:0] / 255×20 V

*Initial value : 8.0 V

| Register Name | | CTLP HP VREC B | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 31h | R/W | HPCTLPOINTB7 | HPCTLPOINTB6 | HPCTLPOINTB5 | HPCTLPOINTB4 | HPCTLPOINTB3 | HPCTLPOINTB2 | HPCTLPOINTB1 | HPCTLPOINTB0 |
| Default | 66h | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

D7-D0： High Power Control Point B(0-255)

The target value of VRECT voltage for the current from 125mA to 420mA at High Power mode is shown.

VRECT voltage is calculated below.

VRECT voltage = HPCTLPOINTB[7:0] / 255×20 V

*Initial value : 5.4 V

| Register Name | | CTLP HP VREC C | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 32h | R/W | HPCTLPOINTC7 | HPCTLPOINTC6 | HPCTLPOINTC5 | HPCTLPOINTC4 | HPCTLPOINTC3 | HPCTLPOINTC2 | HPCTLPOINTC1 | HPCTLPOINTC0 |
| Default | 41h | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

D7-D0： High Power Control Point C(0-255)

The target value of VRECT voltage for the current larger than 420mA at High Power mode is shown.

VRECT voltage is calculated below.

VRECT voltage = HPCTLPOINTC[7:0] / 255×20 V

*Initial value : 5.1 V

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | CTLP KEY | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 33h | R/W | - | - | - | - | - | - | - | CTLPKEY |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 : CTLPKEY

A setup of Control Point in the High Power mode is chosen as a default, or it can be changed by a register (Address 30h, 31h, 32h).

0 : Register invalid (default)

1 : Register effective

| Register Name | | FUNCTION SET | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 41h | R/W | - | - | - | - | - | - | SETRPWR | SETCE |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D1 : SETRPWR

It is a register which transmits the Received Power value set as RPWR [7:0] (Address 04h).

0 : Normal operation (default)

1 : The Received Power value set as RPWR [7:0] is transmit.

* This register is not cleared by itself.

D0 : SETCE

It is a register which transmits the Control Error value set as CERR [7:0] (Address 03h).

0 : Normal operation (default)

1 : The Control Error value set as CERR [7:0] is transmit.

* This register is not cleared by itself.



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | POWER PARAMETER 2 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 43h | R/W | KB[7:0] | | | | | | | |
| Default | 01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Register Name | | POWER PARAMETER 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 44h | R/W | KC [7:0] | | | | | | | |
| Default | 0Fh | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

| Register Name | | POWER OFFSET | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 45h | R/W | OFFSET[7:0] | | | | | | | |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

REGISTER 43h, 44h, 45h：Power Parameter

These are coefficients to correct the Received Power to be sent to a Tx.

43h, 44h：The default values are for 5V (SELHV = Open). Refer to Application Note for more detail.

45h：The value of offset which is defined at FOD pin can be read.

If other values are written in this register, the offset will be over written.

The Received Power can be adjusted also by pins FOD, FODL, and FODG. Refer to “3. Foreign Object Detection” in Functions section for more detail.

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | CONFIG1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 51h | R | PWRCLASS1 | PWRCLASS0 | MAXPWR5 | MAXPWR4 | MAXPWR3 | MAXPWR2 | MAXPWR1 | MAXPWR0 |
| Default | 0Ah | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

D7-D6：Power Class

It is a register which shows Power Class.

In WPC Version 1.1, it is set as "0".

D5-D0：Maximum Power

It is a register which shows the maximum power supplied to the output of the rectifier which a secondary side expects.

The maximum power is calculated as follows.

Maximum Power = (MAXPWR[5:0] / 2)×$10^{PWRCLASS[1:0]}$ W

By this IC, MAXPWR [5:0] is one of the two following values.

001010： Maximum Power = 5W (default)

010100： Maximum Power = 10W (High Power mode)

| Register Name | | CONFIG 3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 53h | R/W | - | - | - | - | - | COUNT2 | COUNT1 | COUNT0 |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D2-D0：Count

It is a register which shows the number of the Optional packets (Power Control Hold-off time) to transmit in the Identification & configuration phase.

Before Identification packet transmission, when numerical values other than "000" are set to this register, the Power Control Hold-off time packet to transmit will be the number of times to set up.

000： Optional packet does not transmit. (default)

001： Power Control Hold-off time packet is transmitted once.

010： Power Control Hold-off time packet is transmitted twice.

: :

111： Power Control Hold-off time packet is transmitted 7 times.

*The Power Control Hold-off time value to transmit is fixed as 05h.

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | CONFIG 4 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 54h | R/W | WINDOWSIZE[4:0] | | | | | WINDOWOFFSET[2:0] | | |
| Default | 84h | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

D7-D3 : Window Size

It is a register showing the section which takes the average of Received Power.

00000 : 0ms
00001 : 4ms
00010 : 8ms
: :
10000 : 64ms (default)
: :
11110 : 120ms
11111 : 124ms

D2-D0 : Window Offset

It is a register showing the interval of the section and the Received Power packet which take the average of Received Power.

000 : 0ms
001 : 4ms
010 : 8ms
: :
100 : 16ms (default)
: :
110 : 24ms
111 : 28ms



Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | OPTREQ | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 60h | W | - | - | - | - | - | - | - | OPTREQ |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D0 : OPTREQ

It is a request to send the Optional packet (Address 61h, 62 h, 63 h, 64 h, 65 h, and 66 h) to transmit in the Power Transfer phase.

0 : Optional packet is not transmitted. (default)

1 : Optional packet is transmitted.

*This register is cleared by itself.

| Register Name | | OPTCNT | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 61h | R/W | - | - | - | OPTCNT4 | OPTCNT3 | OPTCNT2 | OPTCNT1 | OPTCNT0 |
| Default | 84h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

D4-D0 : OPTCNT

It is a register showing the size of the Optional packet to transmit in the Power Transfer phase.

Please set up message size +2 of a packet.

00000 : Don't set up.

00001 : Don't set up.

00010 : Don't set up.

00011 : Message size = 1 (default)

00100 : Message size = 2

: :

11110 : Message size = 28

11111 : Message size = 29

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | OPTADR | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 62h | R/W | OPTADR[7:0] | | | | | | | |
| Default | 06h | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

D7-D0 : OPTADR

It is a register showing the header of the Optional packet to transmit in a Power Transfer phase.

| Register Name | | OPTDATA1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 63h | R/W | OPTDATA1[7:0] | | | | | | | |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Register Name | | OPTDATA2 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 64h | R/W | OPTDATA2[7:0] | | | | | | | |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Register Name | | OPTDATA3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 65h | R/W | OPTDATA3[7:0] | | | | | | | |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Register Name | | OPTDATA4 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 66h | R/W | OPTDATA4[7:0] | | | | | | | |
| Default | 00h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

REGISTER 63h, 64h, 65h, 66h : OPTDATA

It is a register showing the message of the Optional packet to transmit in a Power Transfer phase.

## FUNCTIONS (Continued)

14. Register Map (Continued)

Description (Continued)

**Privilege register**

| Register Name | | OPTDATTX | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 51h | R | - | - | - | - | OPT4TXWAIT | OPT3TXWAIT | OPT2TXWAIT | OPT1TXWAIT |
| Default | 0Ah | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

D3-D0 : OPTDATTX

It is a register showing the transmitting state of the message of the Optional packet to transmit in a Power Transfer phase.

0 : Transmission is completed. (default)

1 : Transmission is not completed.

*Please do not write data in OPTDATA1 [7:0] at the time of OPT1TXWAIT = 1.

*Please do not write data in OPTDATA2 [7:0] at the time of OPT2TXWAIT = 1.

*Please do not write data in OPTDATA3 [7:0] at the time of OPT3TXWAIT = 1.

*Please do not write data in OPTDATA4 [7:0] at the time of OPT4TXWAIT = 1.

| Register Name | | OPTREQ | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Sub Address | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 71h | R/W | MAJORVER3 | MAJORVER2 | MAJORVER1 | MAJORVER0 | MINORVER3 | MINORVER2 | MINORVER1 | MINORVER0 |
| Default | 00h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

D7-D4 : MAJOR VER[3:0]

Major Version of Volume I of the System Description Wireless Power Transfer of the WPC standard to which this IC corresponds is shown.

0001 : Major Version (default)

D3-D0 : MINOR VER[3:0]

Minor Version of Volume I of the System Description Wireless Power Transfer of the WPC standard to which this IC corresponds is shown.

0001 : Minor Version (default)



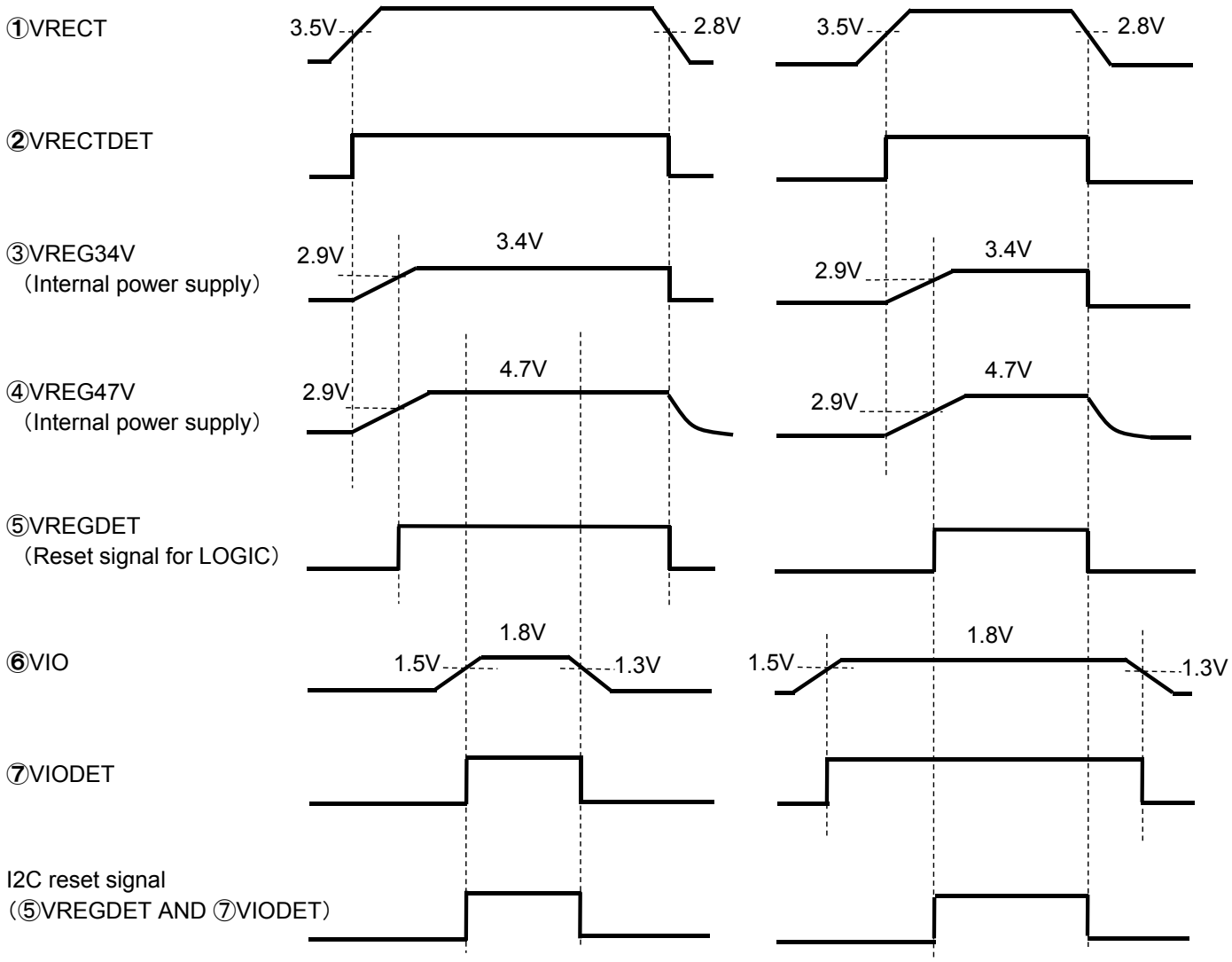
Established : 2014-01-15
Revised : ####-##-##

## FUNCTIONS (Continued)

15. Power supply sequence

(a) In the case of Power on in order VRECT→VIO and Power off VIO→VRECT

(b) In the case of Power on in order VIO→VRECT and Power off VRECT→VIO






Established : 2014-01-15
Revised : ####-##-##

## EVALUATION RESULTS

Evaluation Circuit Diagram (5W)

Conditions :

EXT (B3) : 5V input

FCCNT (C5) : Pulled down with a 100kΩresistor for section 3, and connected to REG34V for other evaluations.

FULLCH (E5) : Voltage swept for section 3, and connected to GND for other evaluations.

SELHV (G2) : Opened

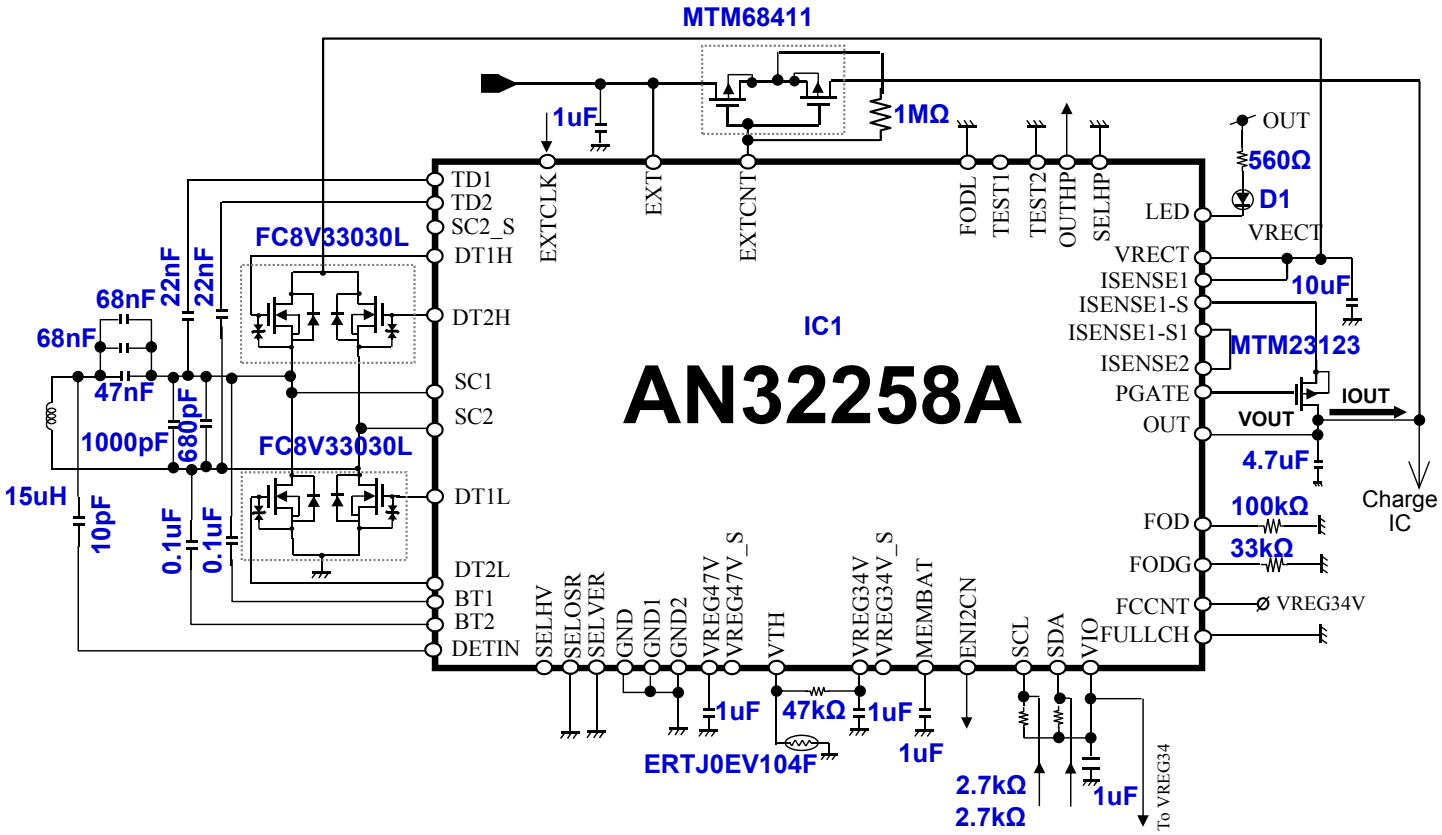



**Figure B-1. AN32258A Evaluation Circuit**



Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS

1.Output Voltage Characteristics

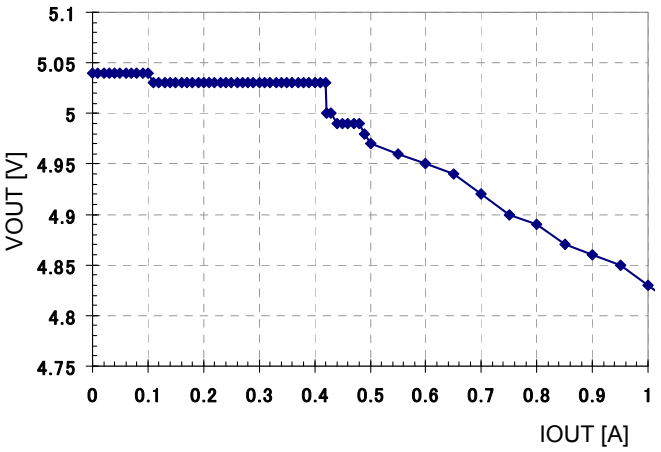



**Figure B-2 Output Voltage vs Output Current**

2. $V_{RECT}$ Voltage Characteristics

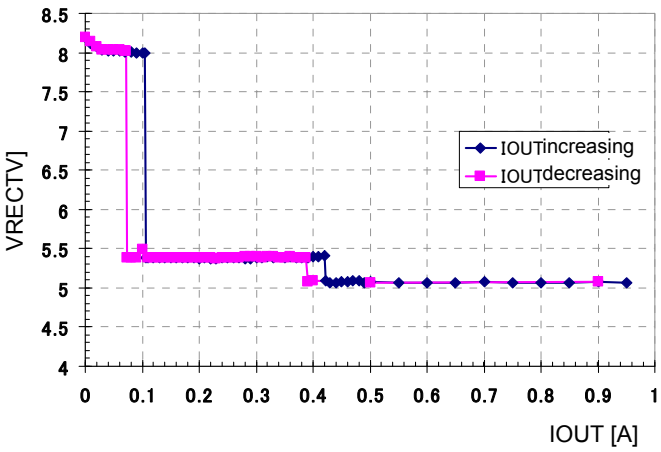



**Figure B-3 VRECT Voltage vs Output Current**

3. Full-Charge Characteristics

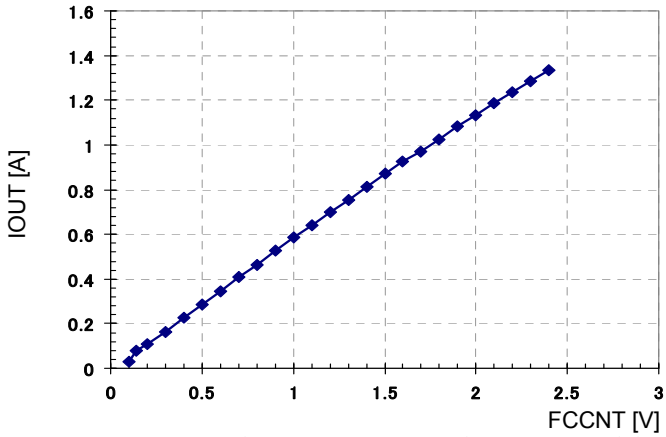



**Figure B-4 Full-Charge Detecting Current vs FCCNT Voltage with a 100kΩResistor Connected**

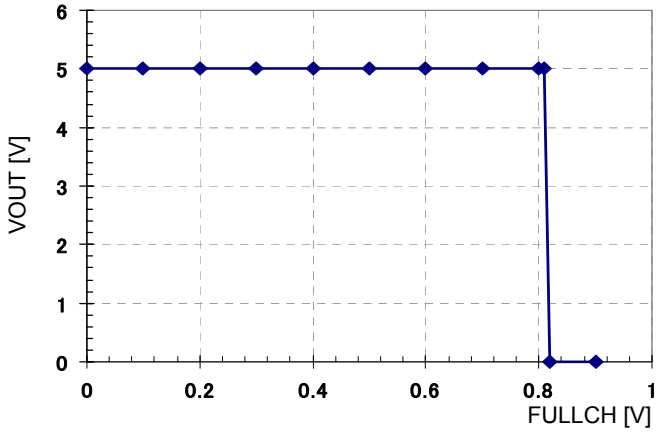



**Figure B-5 Output Voltage vs FULLCH Level**

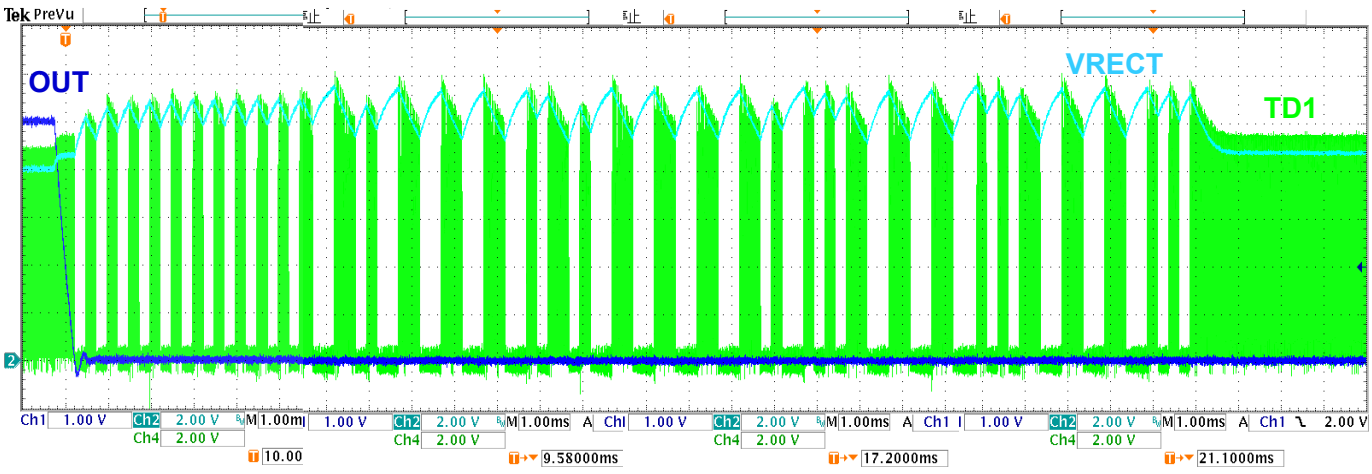



**Figure B-6 Received Signal Characteristics after a Full-Charge Detection**

*After the output voltage becomes zero, an End Power Transfer Packet is sent.



Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS (Continued)

4. Over Current Protection Characteristics

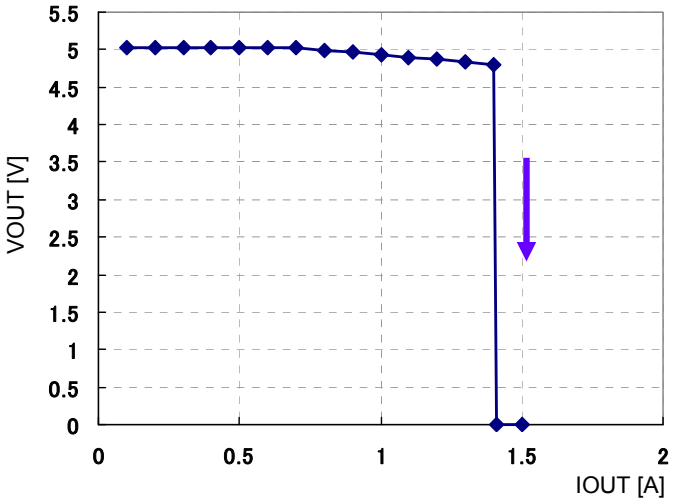



**Figure B-7 VOUT vs IOUT**

5. Temperature Detection Characteristics

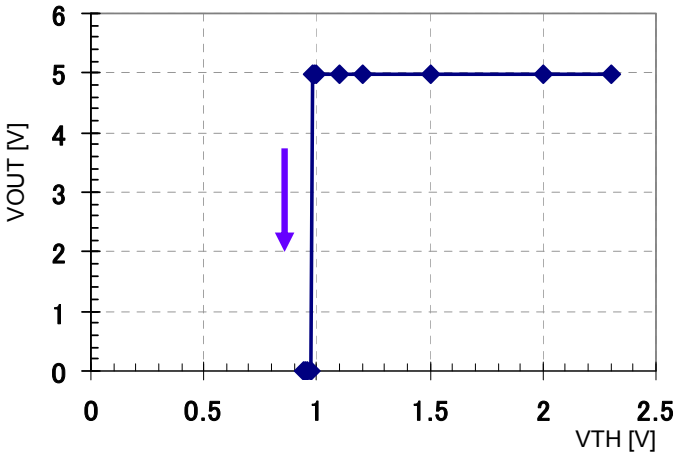



**Figure B-8 Output Voltage vs VTH**

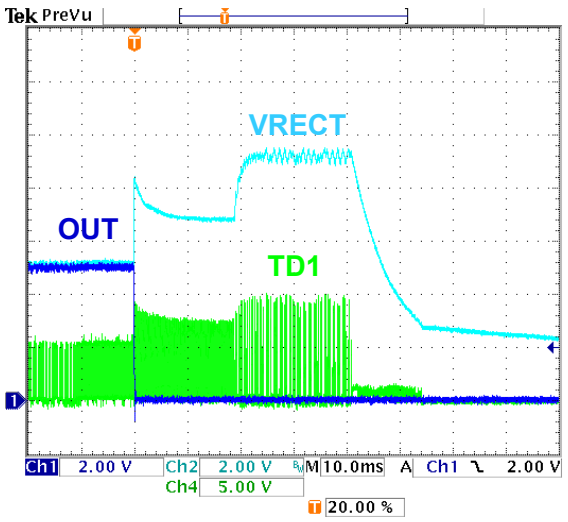



**Figure B-9 Received Signal Characteristics after a Temperature Detection**

*Conditions : IOUT =500mA
The power transmission from Tx stops due to temperature detection (VTH).



Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS (Continued)

6. Over Voltage Protection Characteristics

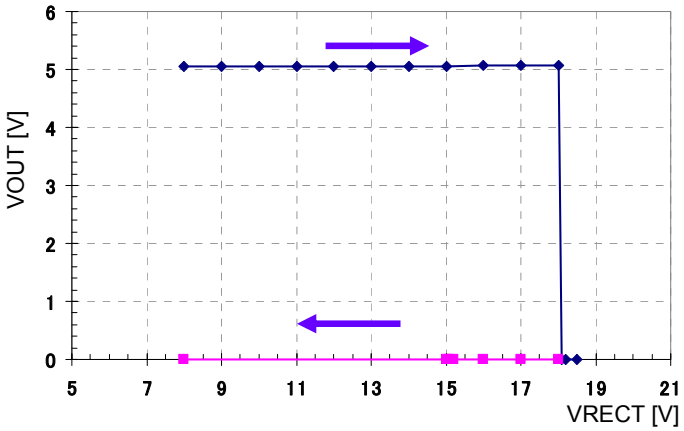



Figure B-10 VOUT vs VRECT by OVP

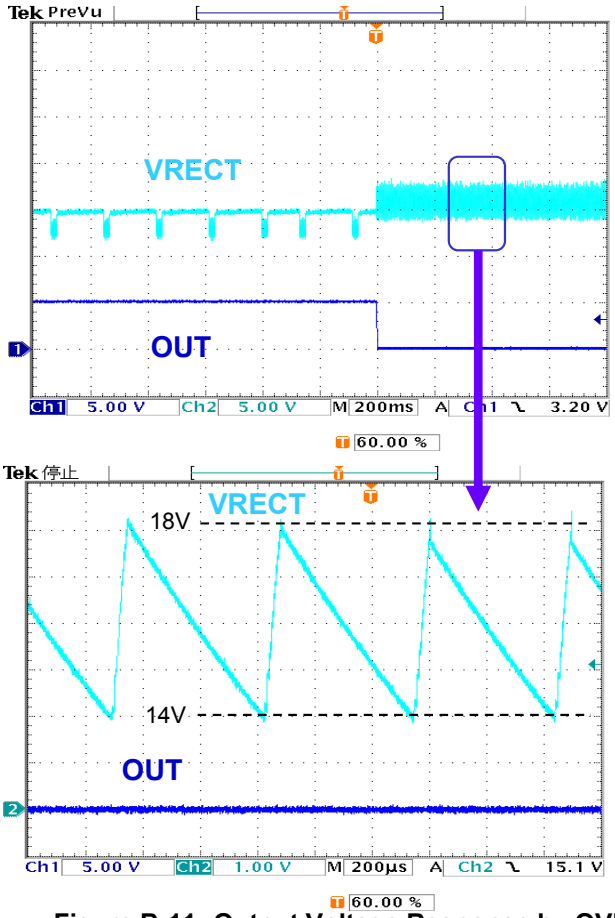



Figure B-11 Output Voltage Response by OVP

7. Foreign Object Detection Characteristics

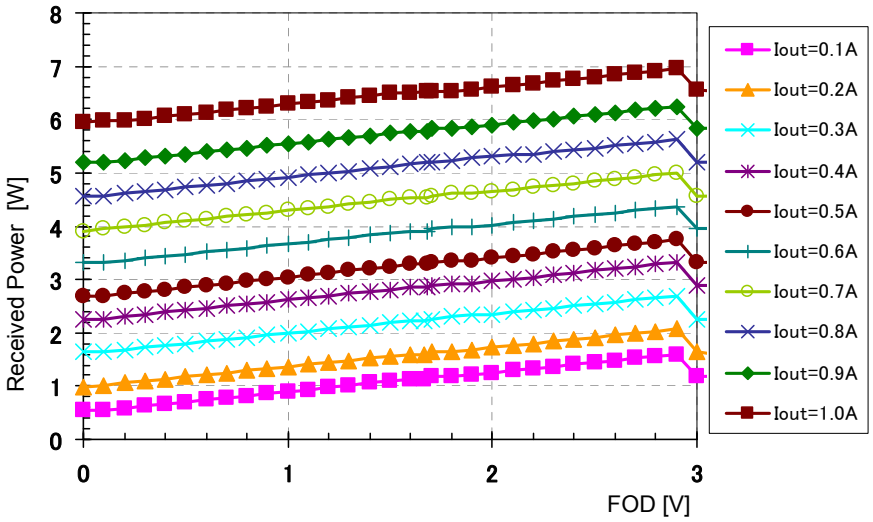



Figure B-12 Received Power vs FOD Voltage

*Received Power = (RPWR[7:0] / 128) × (Maximum Power / 2) ×10Power Class W

## TYPICAL CHARACTERISTICS (Continued)

8. External Power Supply Switch Characteristics

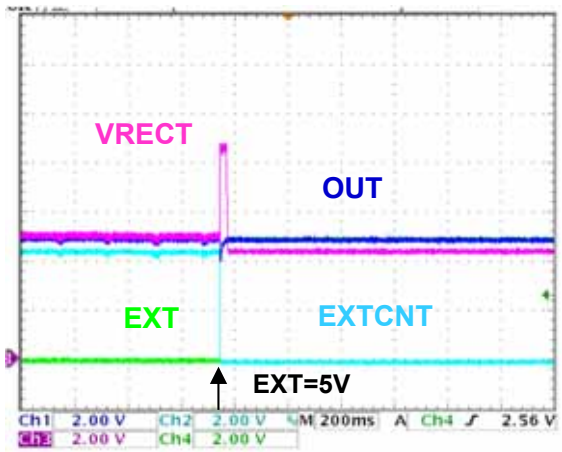



**Figure B-13 Voltage when an External Power is Inputted during Normal Wireless Power Transmission**

*Condition : IOUT=500mA

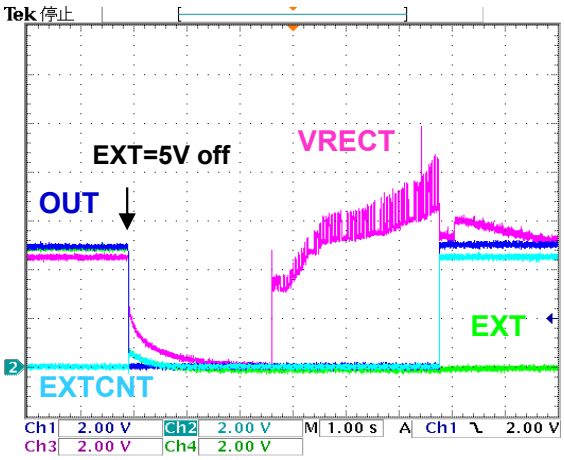



**Figure B-14 Normal Power Transmission Resumes after the External Power Turns Off.**

*Condition : IOUT=500mA

9. Start-up Characteristics

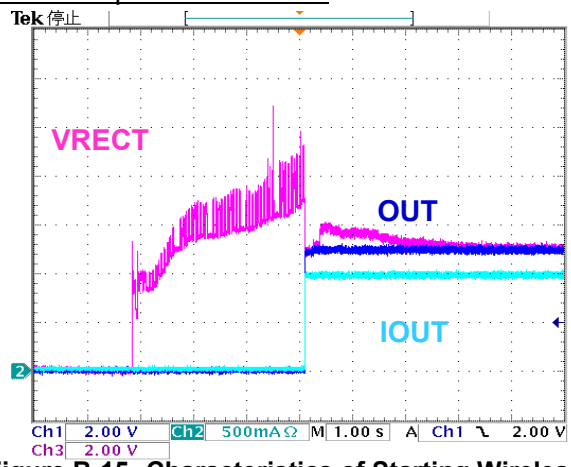



**Figure B-15 Characteristics of Starting Wireless Power Transmission**

*Condition : IOUT=500mA

10. Communication Packet Configuration

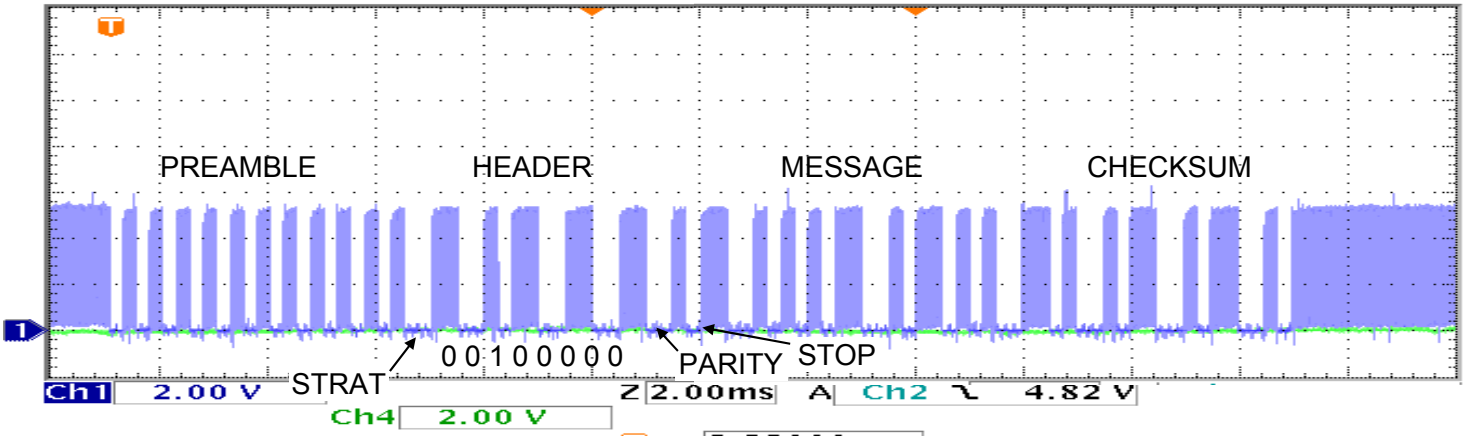



**Figure B-16 Rx Communication Packet Structure**

## TYPICAL CHARACTERISTICS (Continued)

11. LED Display Characteristics

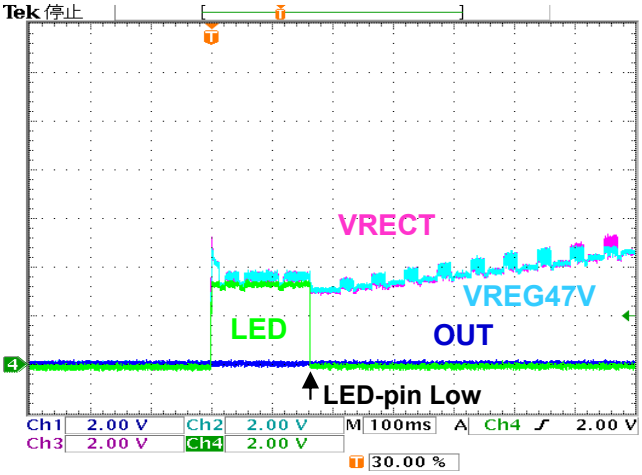



**Figure B-17 LED Characteristics 1**

*Condition : LED is pulled up to VREG34V first

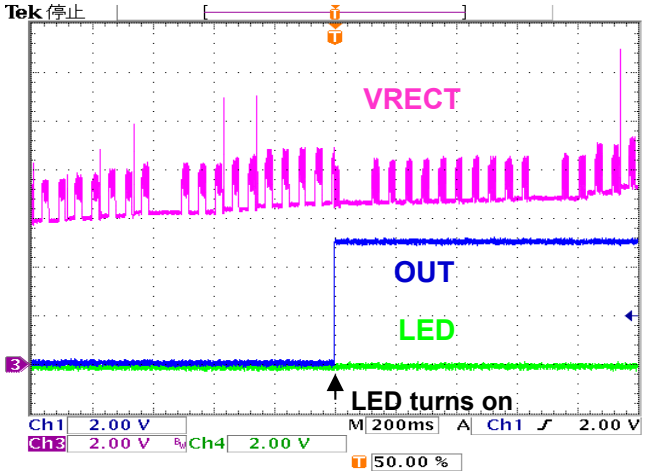



**Figure B-18 LED Characteristics 2**

*LED lights up when the output starts.

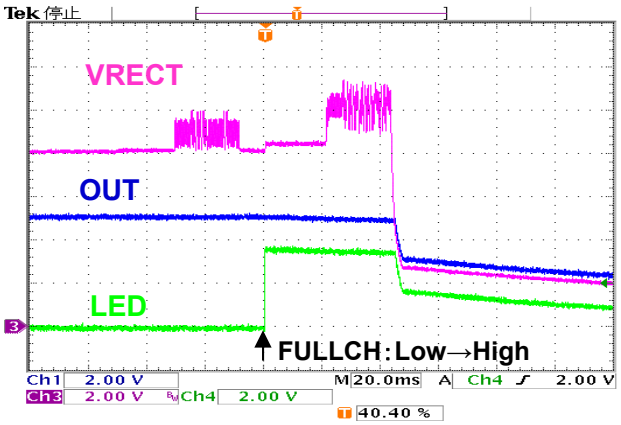



**Figure B-19 LED Turned off by a Full Charge**

*FULLCH detects a full-charge, and LED turns off when the output goes down.

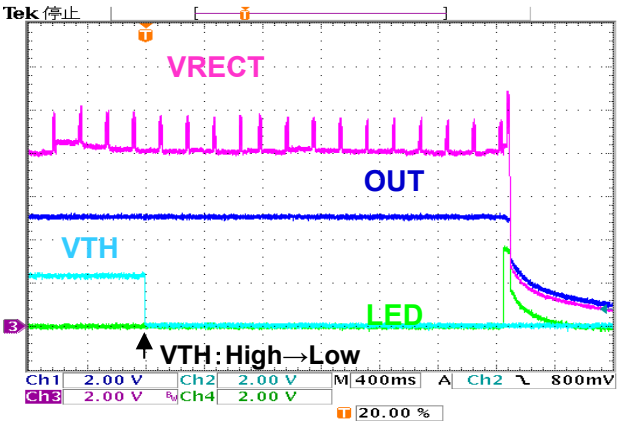



**Figure B-20 LED Turned off by an over temperature**

*VTH detects an over temperature, and LED turns off when the output goes down.

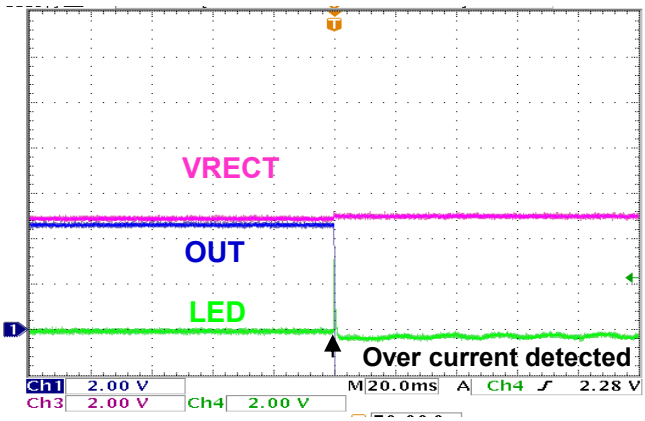



**Figure B-21 LED Turned off by an over current**

After an over current is detected, LED turns off when the output goes down.



Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS (Continued)

12. Power Efficiency

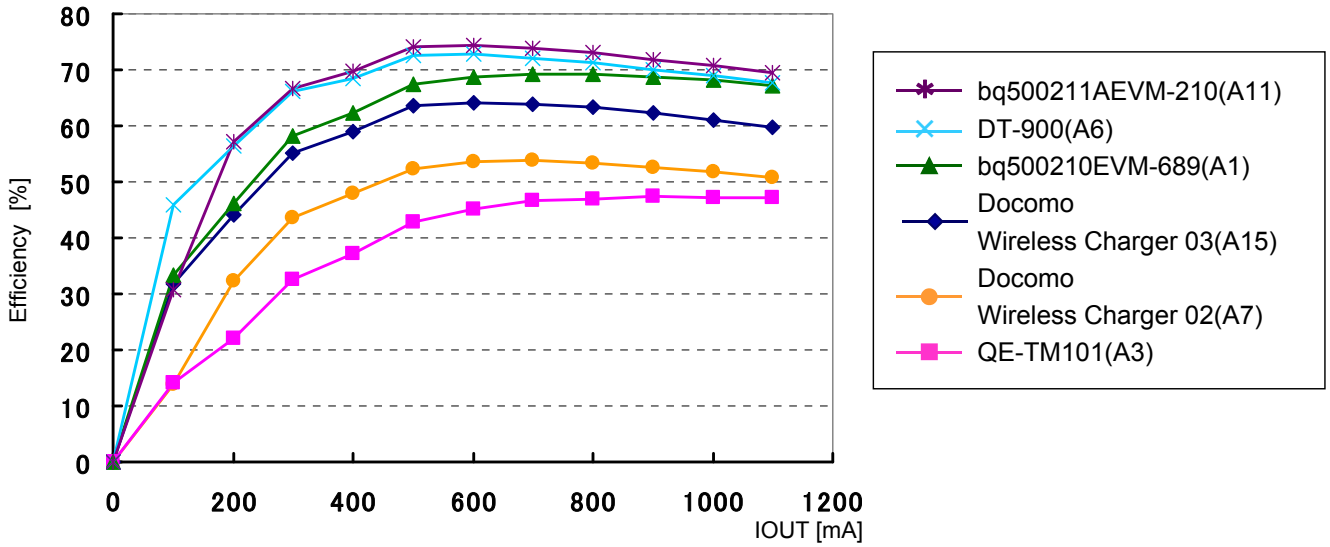



**Figure B-22. Power Efficiency**

13. Transient Characteristics

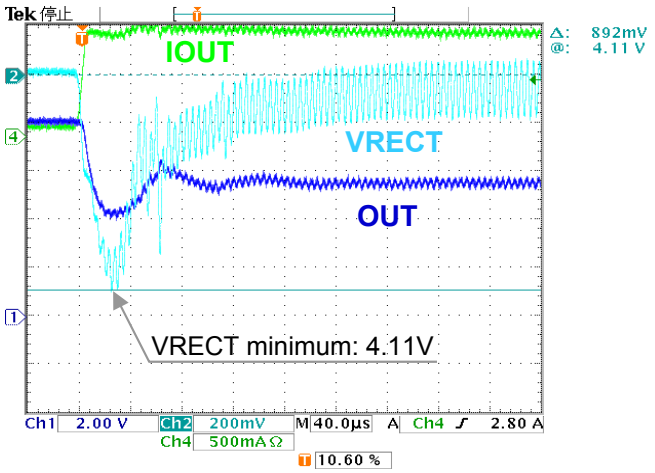



**Figure B-23. Load current changed 0mA→1000mA**

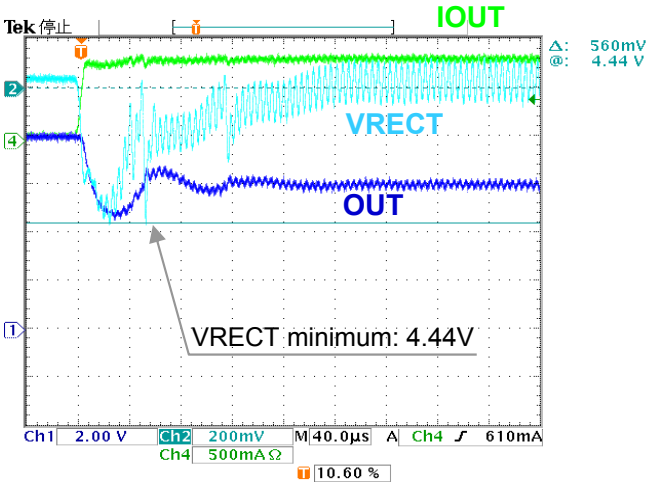



**Figure B-24. Load Current Changed 0mA→800mA**

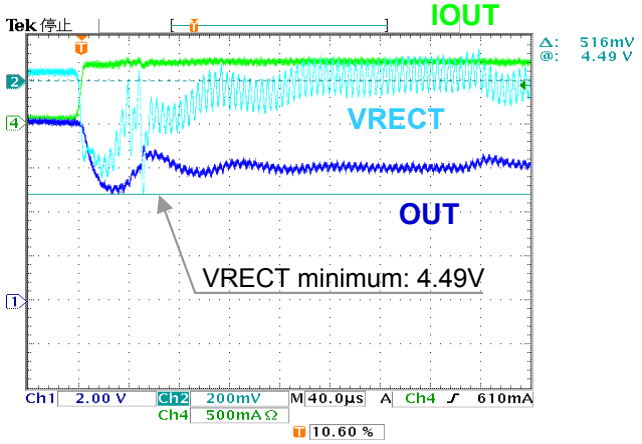



**Figure B-25. Load current changed 0mA→600mA**

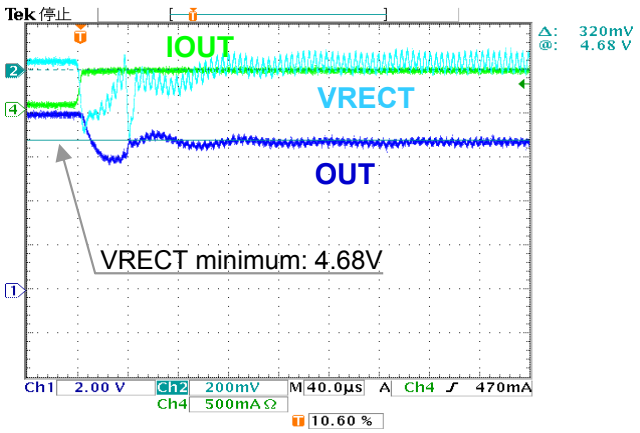


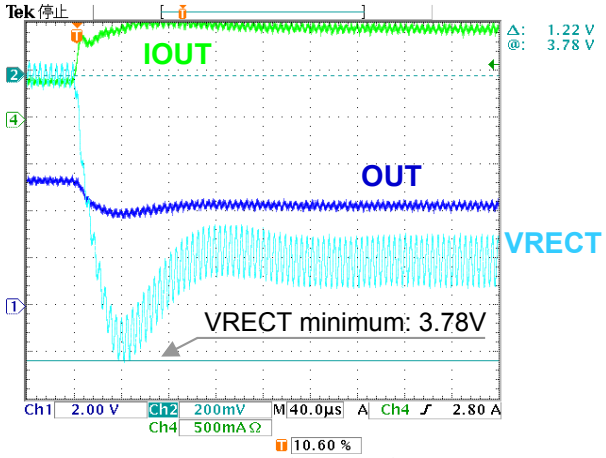

**Figure B-26. Load current changed 0mA→400mA**



Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS (Continued)

13. Transient Characteristics (Continued)




FigureB-27. Load Current Changed (400mA→1000mA)

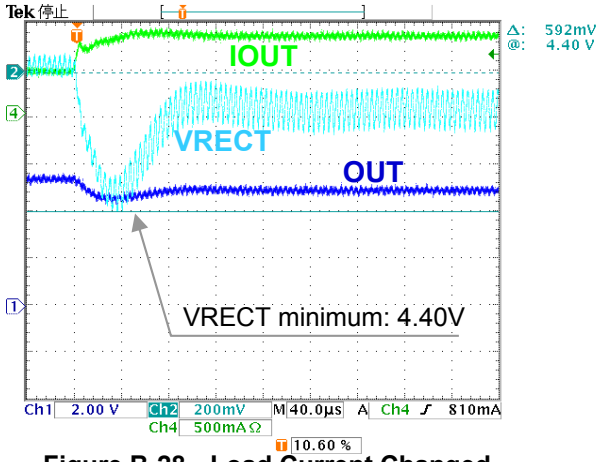



Figure B-28. Load Current Changed (400mA→800mA)

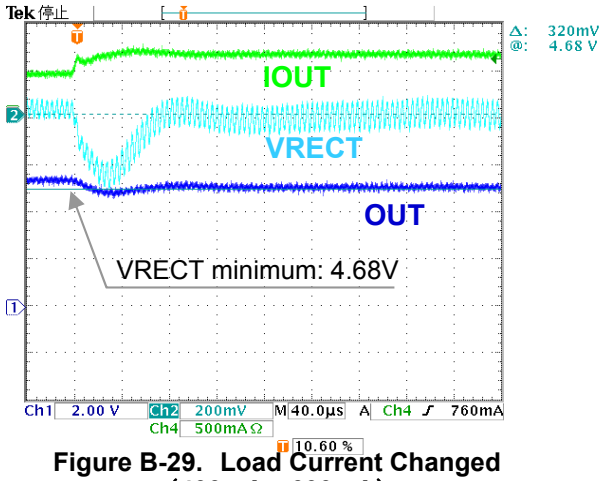
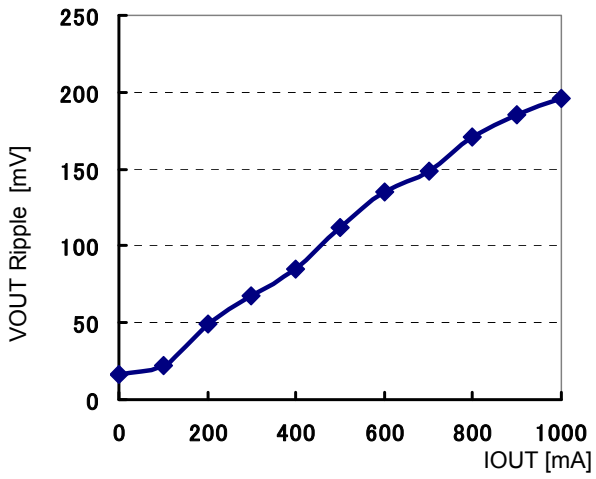



Figure B-29. Load Current Changed (400mA→600mA)

14. VOUT Ripple Voltage




FigureB-30. VOUT Ripple Characteristics



Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS (Continued)

Evaluation Circuit Diagram (High-Power)

Conditions :

FCCNT (C5):Pulled down with a 100kΩresistor for section 17, and connected to REG34V for other evaluations.
FULLCH (E5): Voltage swept for section 17, and connected to GND for other evaluations.
SELHV (G2): Opened
SELHP(F3): VREG34V (high-power mode)
SELOSR(F4): VREG34V (external sense resistor)
Coil (L1): 15.7uH
Tx: NN32251A (Type A6 with 3 coils), or varied for section 20

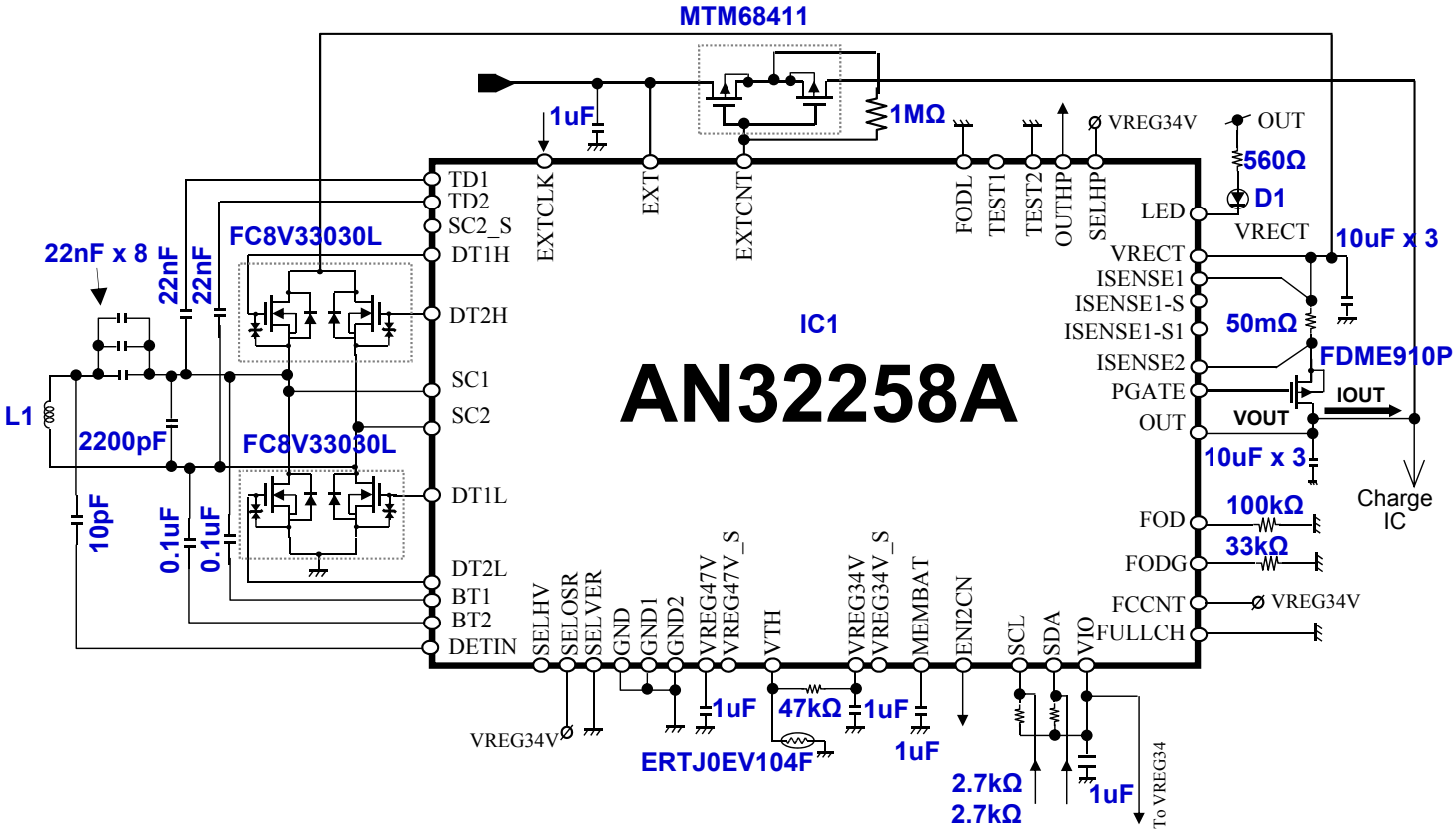


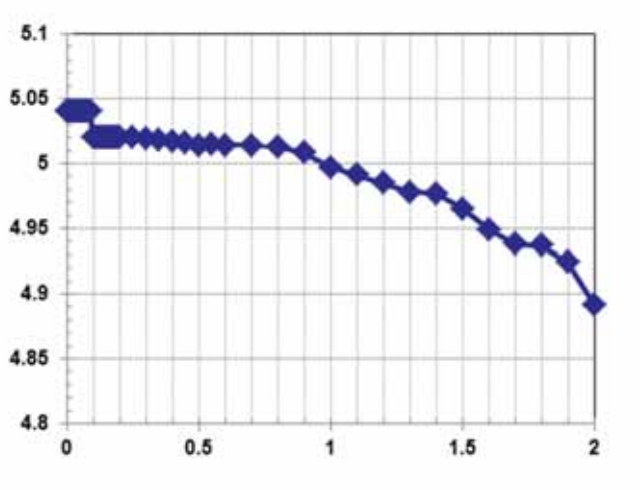

**Figure C-1. AN32258 Evaluation Circuit**



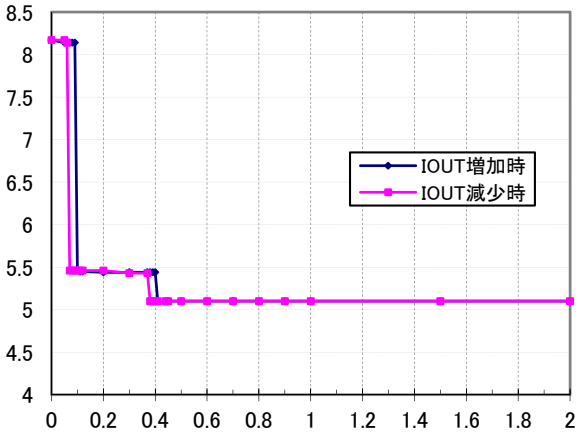
Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS

15. Voltage Output Characteristics




16. $V_{RECT}$- Voltage Characteristics




17. Full-Charge Characteristics

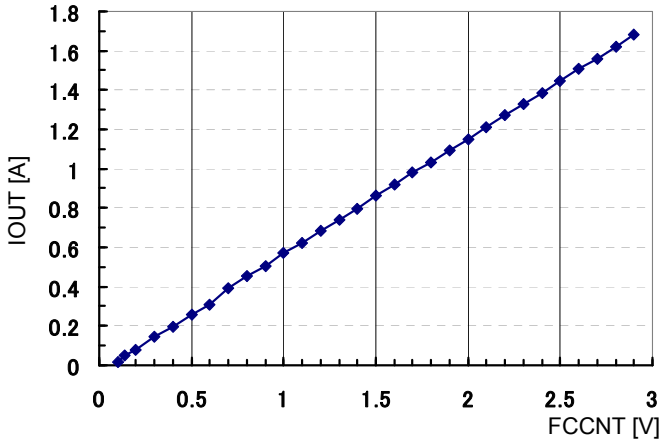



**Figure C-4. Full-Charge Detecting Current vs FCCNT**

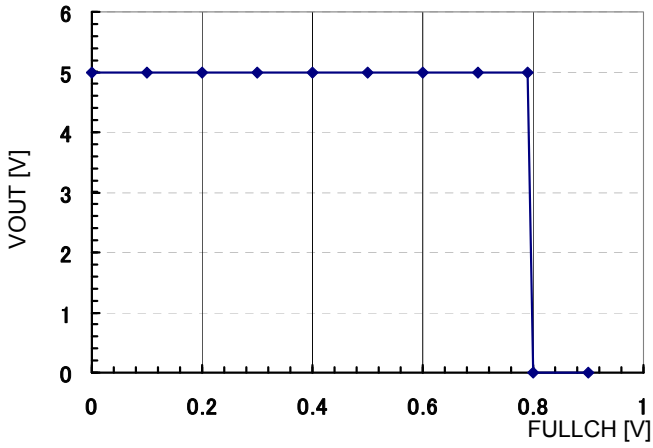



**Figure C-5. Output Voltage vs FULLCH Level**

18. Over Current Protection Characteristics

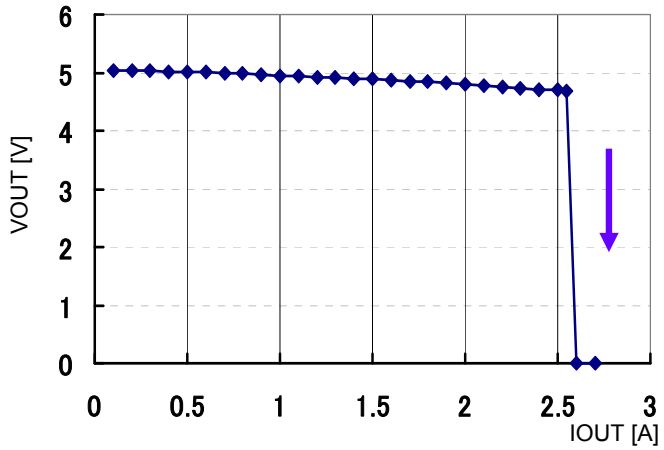



**Figure C-6. VOUT vs IOUT with Internal OCP**

## TYPICAL CHARACTERISTICS (Continued)

19. Foreign Object Detection Characteristics

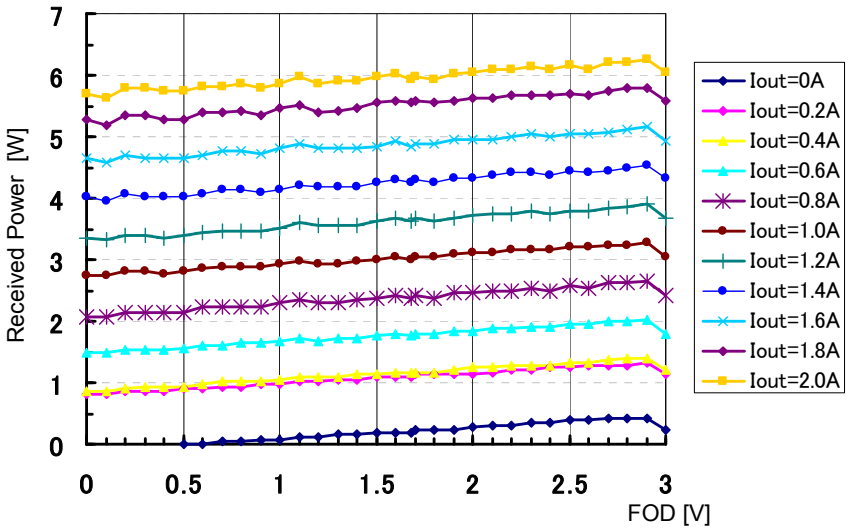



**Figure C-7. Received Power vs FOD Voltage**

※ Received Power = (RPWR[7:0] / 128) × (Maximum Power / 2) × 10Power Class W

20-1. Power Efficiency

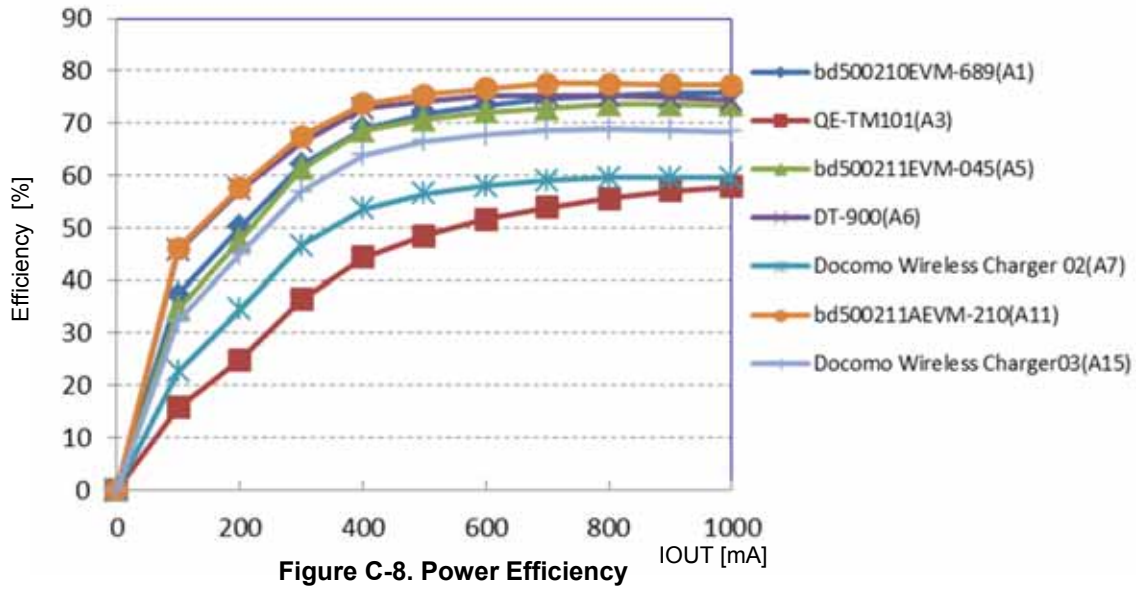



**Figure C-8. Power Efficiency**



Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS (Continued)

20-2. Power Efficiency with NN32251A

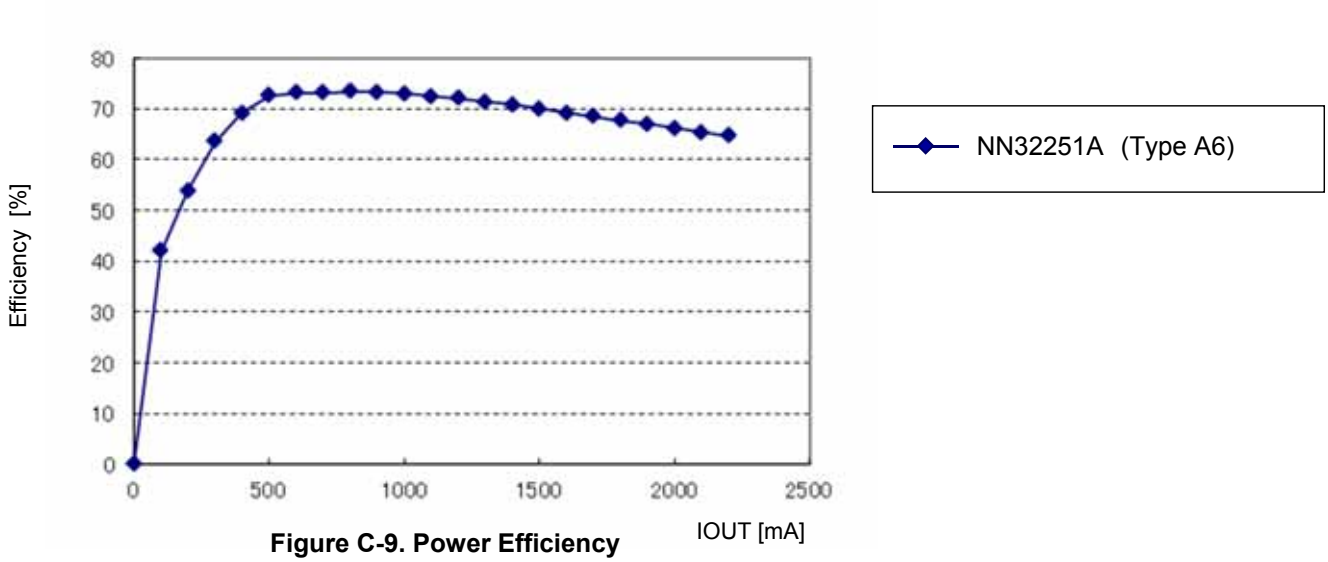



**Figure C-9. Power Efficiency**

21. Transient Characteristics with NN32251A Type A6

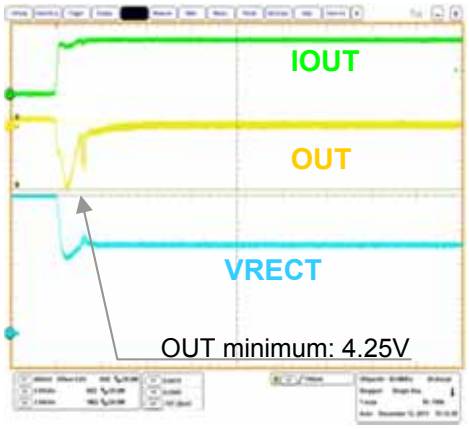



**Figure C-10. Load Current Changed (0mA→1500mA)**

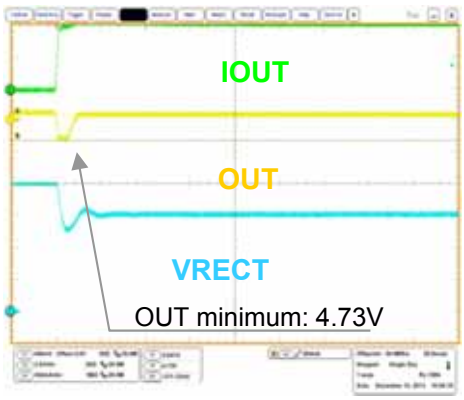



**Figure C-11. Load Current Changed (0mA→1000mA)**

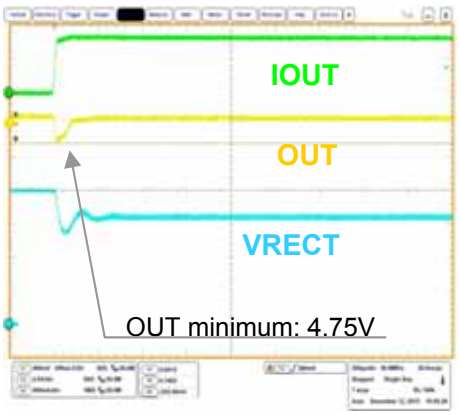



**Figure C-12. Load Current Changed (0mA→800mA)**

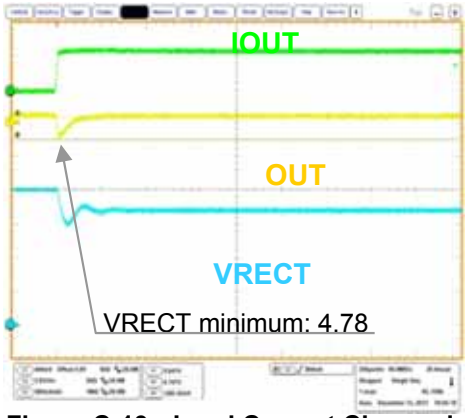



**Figure C-13. Load Current Changed (0mA→600mA)**



Established : 2014-01-15
Revised : ####-##-##

## TYPICAL CHARACTERISTICS (Continued)

21. Transient Characteristics with NN32251A Type A6 (Continued)

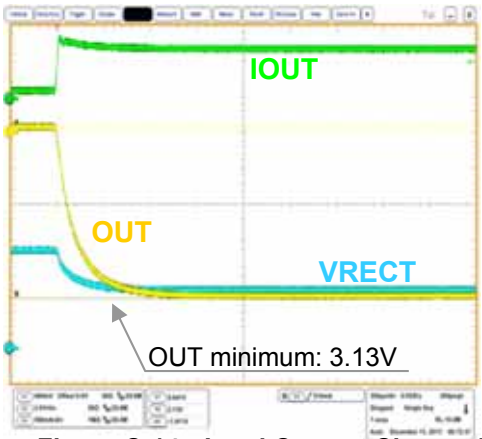
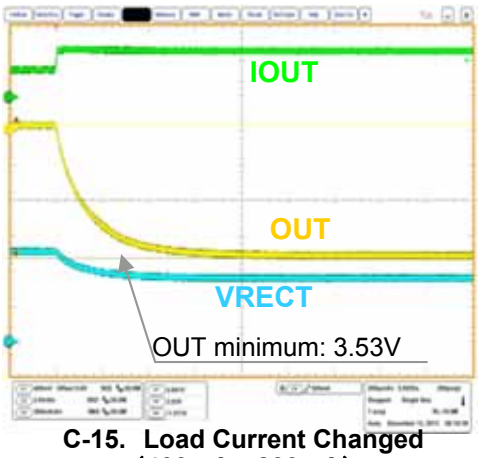



Figure C-14. Load Current Changed (120mA→1000mA)




C-15. Load Current Changed (400mA→800mA)

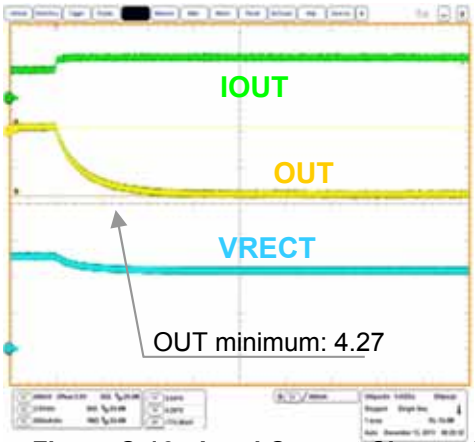
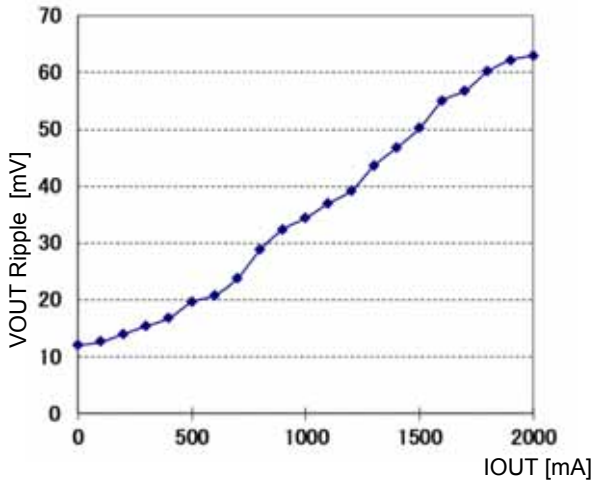



Figure C-16. Load Current Changed (400mA→600mA)

22. VOUT Ripple Voltage




FigureC-17. VOUT Ripple Characteristics

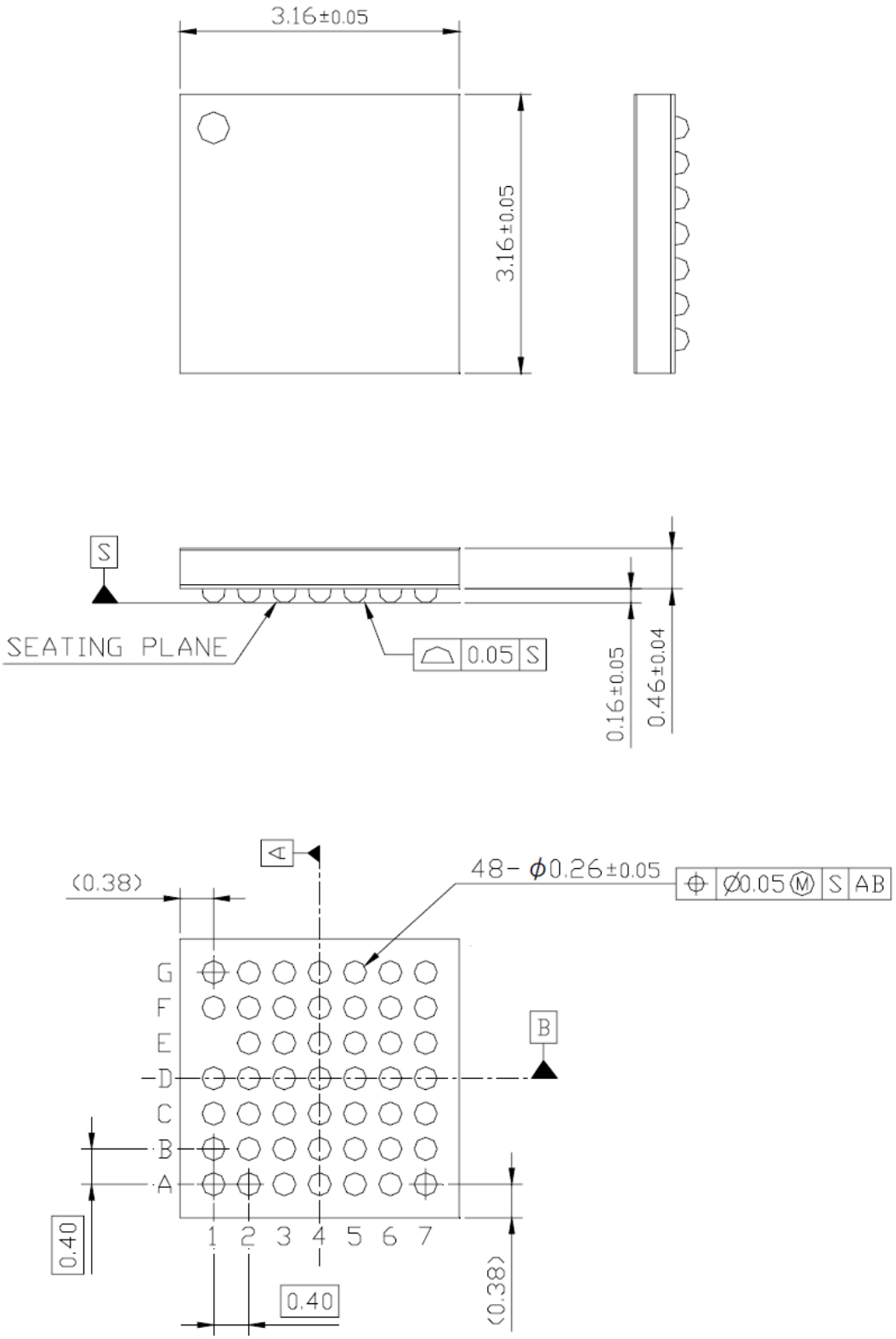


Established : 2014-01-15
Revised : ####-##-##

## Package Information

**Package Code : XBGA048-W-3232AML**

Unit: mm






Established : 2014-01-15
Revised : ####-##-##

## IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.



Established : 2014-01-15
Revised : ####-##-##

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Consult our sales staff in advance for information on the following applications:
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(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.



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