Si53154

PCI-EXPRESS GEN 1, GEN 2, & GEN 3 QUAD FANOUT BUFFER

Features

- PCI-Express Gen 1,Gen 2, and Gen 3 compliant
- Supports Serial ATA (SATA) at 100 MHz
- 100–210 MHz operation
- Low power, push pull, differential output buffers
- Internal termination for maximum integration
- Dedicated output enable pin for each output
- Four PCI-Express buffered clock outputs
- Clock input spread tolerable
- Supports LVDS outputs
- I^2C support with readback capabilities
- Extended temperature: –40 to 85 ^oC
- 3.3 V power supply
- 24-pin QFN package

Ordering Information:
See page 17.

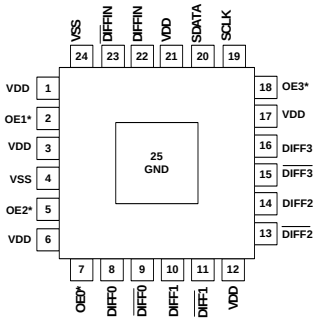
Applications

- Network attached storage
- Multi-function printers
- Wireless access point
- Routers

Description

The Si53154 is a spread tolerable PCIe clock buffer that can source four PCIe clocks simultaneously. The device has four hardware output enable control inputs for enabling the respective differential outputs on the fly. The device also features output enable control through I^2C communication. I^2C programmability is also available to dynamically control skew, edge rate and amplitude on the true, compliment, or both differential signals on the clock outputs. This control feature enables optimal signal integrity as well as optimal EMI signature on the clock outputs.

Pin Assignments



***Note:** Internal 100 kohm pull-up.

Patents pending

Functional Block Diagram

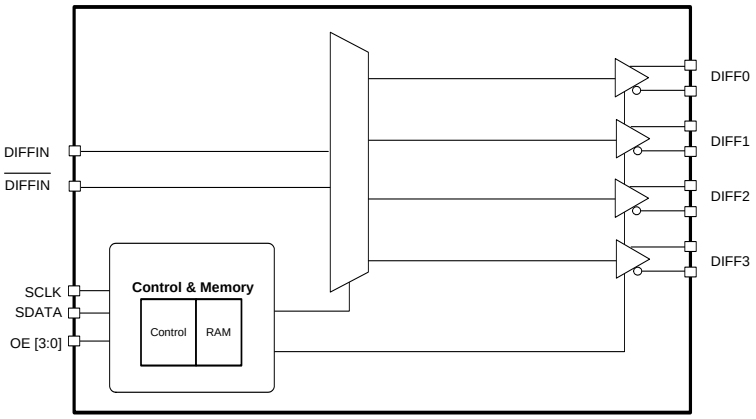


TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Operating Voltage	VDD core	3.3 ± 5%	3.135	—	3.465	V
3.3 V Input High Voltage	V_{IH}	Control input pins	2.0	—	V_{DD} + 0.3	V
3.3 V Input Low Voltage	V_{IL}	Control input pins	V_{SS} – 0.3	—	0.8	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	2.2	—	–	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	—	1.0	V
Input High Leakage Current	I_{IH}	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	—	—	5	µA
Input Low Leakage Current	I_{IL}	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	—	—	µA
3.3 V Output High Voltage (Single-Ended Outputs)	V_{OH}	I_{OH} = –1 mA	2.4	—	—	V
3.3 V Output Low Voltage (Single-Ended Outputs)	V_{OL}	I_{OL} = 1 mA	—	—	0.4	V
High-impedance Output Current	I_{OZ}		–10	—	10	µA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	L_{IN}		—	—	7	nH
Dynamic Supply Current in Fanout Mode	$I_{DD\_3.3V}$	Differential clocks with 5” traces and 2 pF load, frequency at 100 MHz	—	—	35	mA

Table 2. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DIFFIN at 0.7 V						
Input Frequency Range	f_{in}		100	—	210	MHz
Rising and Falling Slew Rates for Each Clock Output Signal in a Given Differential Pair	T_R / T_F	Single ended measurement: V_{OL} = 0.175 to V_{OH} = 0.525 V (Averaged)	0.6	—	4	V/ns
Differential Input High Voltage	V_{IH}		150	—	—	mV
Differential Input Low Voltage	V_{IL}		—	—	–150	mV
Crossing Point Voltage at 0.7 V Swing	V_{OX}	Single-ended measurement	250	—	550	mV
Vcross Variation over all Edges	ΔV_{OX}	Single-ended measurement	—	—	140	mV
Differential Ringback Voltage	V_{RB}		–100	—	100	mV
Time before Ringback Allowed	T_{STABLE}		500	—	—	ps
Absolute Maximum Input Voltage	V_{MAX}		—	—	1.15	V
Absolute Minimum Input Voltage	V_{MIN}		–0.3	—	—	V
Duty Cycle for Each Clock Output Signal in a Given Differential Pair	T_{DC}	Measured at crossing point V_{OX}	45	—	55	%
Rise/Fall Matching	T_{RFM}	Determined as a fraction of 2 x (T_R – T_F)/(T_R + T_F)	—	—	20	%
DIFF at 0.7 V						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Clock Skew	T_{SKEW}	Measured at 0 V differential	—	—	50	ps
Additive Peak Jitter	Pk-Pk		0	—	10	ps
Additive PCIe Gen 2 Phase Jitter	RMS_{GEN2}	10 kHz < F < 1.5 MHz	0	—	0.5	ps
		1.5 MHz< F < Nyquist Rate	0	—	0.5	ps
Additive PCIe Gen 3 Phase Jitter	RMS_{GEN3}	Includes PLL BW 2–4 MHz (CDR = 10 MHz)	0	—	0.10	ps
Additive Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	20	50	ps
Long-term Accuracy	L_{ACC}	Measured at 0 V differential	—	—	100	ppm

Table 2. AC Electrical Specifications (Continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Rising/Falling Slew rate	T_R/T_F	Measured differentially from ±150 mV	2.5	—	8	V/ns
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV
Enable/Disable and Setup						
Clock Stabilization from Power-Up	T_{STABLE}		—	—	5	ms
Stopclock Set-up Time	T_{SS}		10.0	—	—	ns

Table 3. Absolute Maximum Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$	Functional	—	—	4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	4.6	V_{DC}
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Industrial Temperature, Operating Ambient	T_A	Functional	–40	—	85	°C
Commercial Temperature, Operating Ambient	T_A	Functional	0	—	85	°C
Temperature, Junction	T_J	Functional	—	—	150	°C
Dissipation, Junction to Case	$Ø_{JC}$	JEDEC (JESD 51)	—	—	35	°C/W
Dissipation, Junction to Ambient	$Ø_{JA}$	JEDEC (JESD 51)	—	—	37	°C/W
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000	—	–	V
Flammability Rating	UL-94	UL (Class)		V–0		

Note: **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

2. Functional Description

2.1. OE Pin Definition

The OE pins are active high inputs used to enable and disable the output clocks. To enable the output clock, the OE pin needs to be logic high and the I^2C output enable bit needs to be logic high. There are two methods to disable the output clocks: the OE is pulled to a logic low, or the I^2C enable bit is set to a logic low. The OE pins is required to be driven at all time and even though it has an internal 100 kΩ resistor.

2.2. OE Assertion

The OE signals are active high inputs used for synchronous stopping and starting the DIFF output clocks respectively while the rest of the clock generator continues to function. The assertion of the OE signal by making it logic high causes stopped respective DIFF outputs to resume normal operation. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

2.3. OE Deassertion

When the OE pin is deasserted by making it logic low, the corresponding DIFF output is stopped, and the final output state is driven low.

3. Test and Measurement Setup

Figures 1–3 show the test load configuration for differential clock signals.

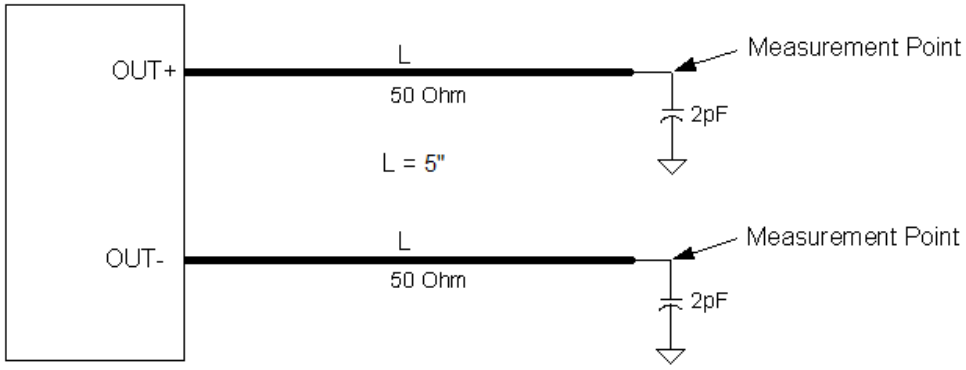


Figure 1. 0.7 V Differential Load Configuration

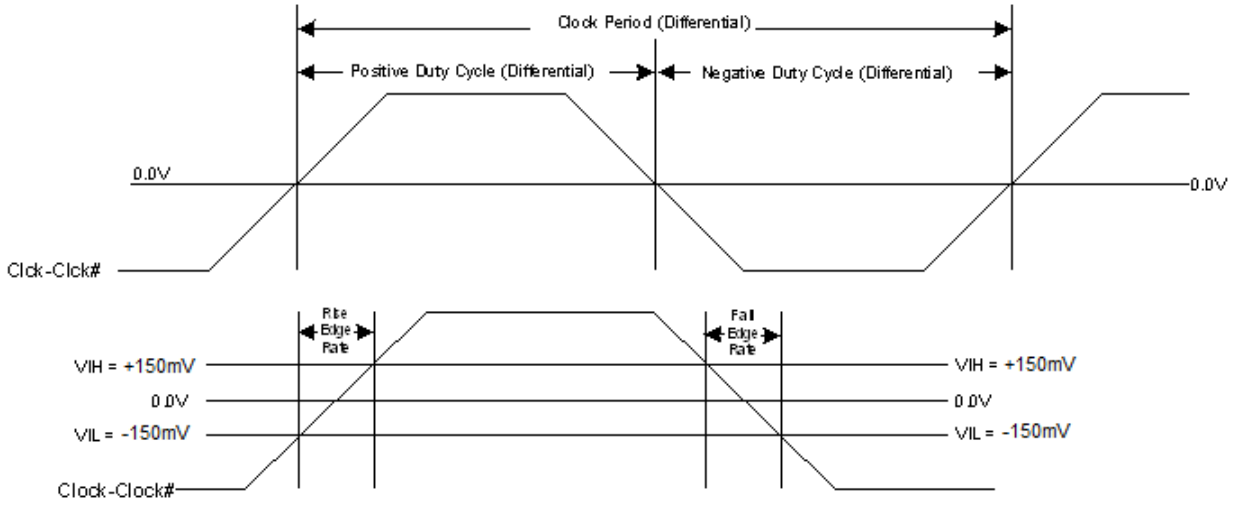


Figure 2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

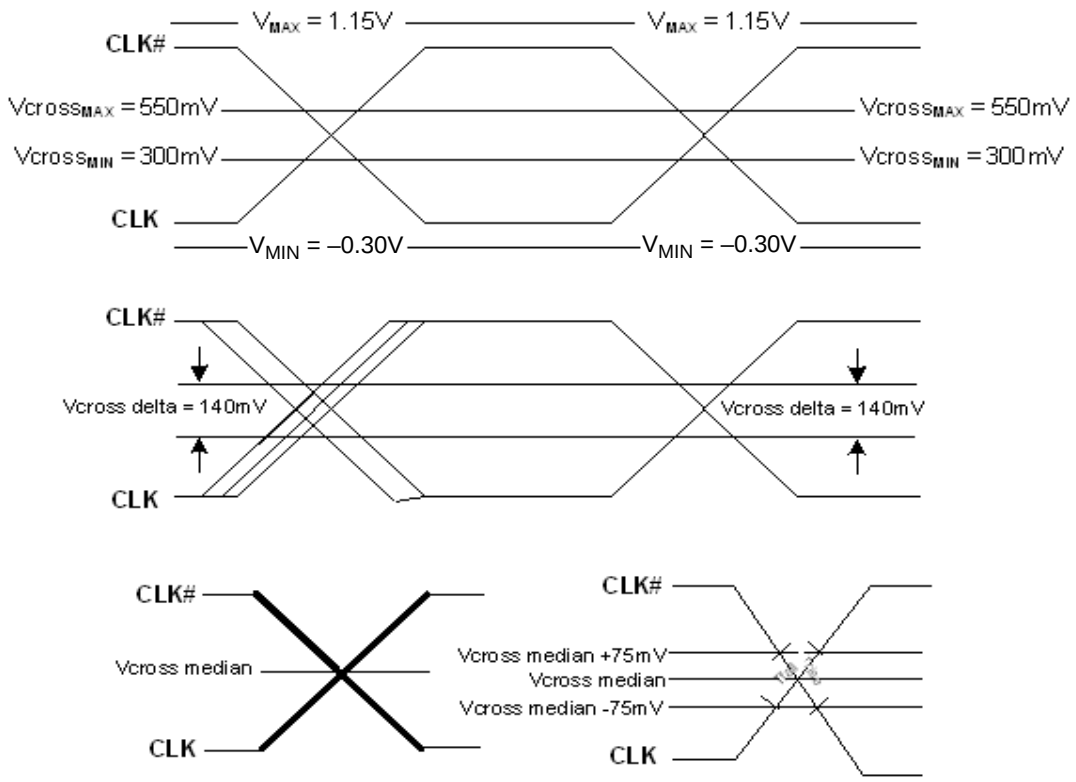


Figure 3. Single-Ended Measurement for Differential Output Signals (for AC Parameters Measurement)

4. Control Registers

4.1. I²C Interface

To enhance the flexibility and function of the clock buffer, an I²C interface is provided. Through the I²C Interface, various device functions are available, such as individual clock output enable. The registers associated with the I²C Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. Power management functions can only be programed in program mode and not in normal operation modes.

4.2. Data Protocol

The I²C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes.

The block write and block read protocol is outlined in Table 4 while Table 5 outlines byte write and byte read protocol. The slave receiver address is 11010110 (D6h).

Table 4. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Register 0. Byte 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000000

Bit	Name	Function
7:0	Reserved	

Control Register 1. Byte 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						DIFF0_OE		DIFF1_OE
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000101

Bit	Name	Function
7:3	Reserved	
2	DIFF0_OE	**Output Enable for DIFF0.** 0: Output disabled. 1: Output enabled.
1	Reserved	
0	DIFF1_OE	**Output Enable for DIFF1.** 0: Output disabled. 1: Output enabled.

Control Register 2. Byte 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF2_OE	DIFF3_OE						
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11000000

Bit	Name	Function
7	DIFF2_OE	**Output Enable for DIFF2.** 0: Output disabled. 1: Output enabled.
6	DIFF3_OE	**Output Enable for DIFF3.** 0: Output disabled. 1: Output enabled.
5:0	Reserved	

Control Register 3. Byte 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Rev Code Bit 3	Rev Code Bit 2	Rev Code Bit 1	Rev Code Bit 0	Vendor ID bit 3	Vendor ID bit 2	Vendor ID bit 1	Vendor ID bit 0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00001000

Bit	Name	Function
7:4	Rev Code Bit 3:0	**Program Revision Code.**
3:0	Vendor ID bit 3:0	**Vendor Identification Code.**

Control Register 4. Byte 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BC7	BC7	BC5	BC4	BC3	BC2	BC1	BC0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000110

Bit	Name	Function
7:0	BC7:0	**Byte Count Register.**

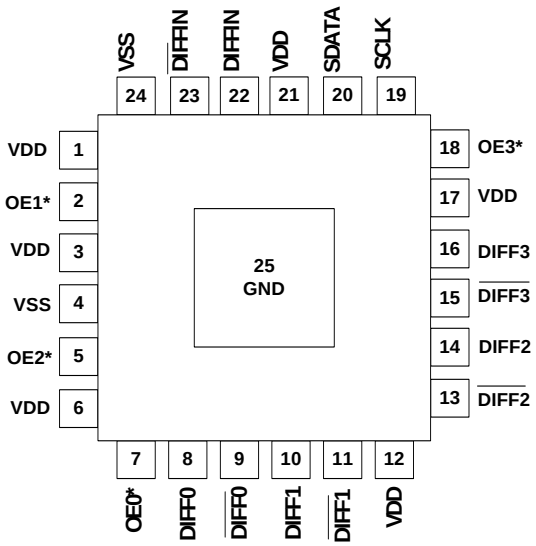
Control Register 5. Byte 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF_Amp_Sel	DIFF_Amp_Cntl[2]	DIFF_Amp_Cntl[1]	DIFF_Amp_Cntl[0]				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11011000

Bit	Name	Function
7	DIFF_Amp_Sel	**Amplitude Control for DIFF Differential Outputs.** 0: Differential outputs with Default amplitude. 1: Differential outputs amplitude is set by Byte 5[6:4].
6	DIFF_Amp_Cntl[2]	**DIFF Differential Outputs Amplitude Adjustment.** 000: 300 mV 001: 400 mV 010: 500 mV 011: 600 mV 100: 700 mV 101: 800 mV 110: 900 mV 111: 1000 mV
5	DIFF_Amp_Cntl[1]	
4	DIFF_Amp_Cntl[0]	
3:0	Reserved	

5. Pin Descriptions: 24-Pin QFN



***Note:** Internal 100 kohm pull-up.

Figure 4. 24-Pin QFN

Table 6. Si53154 24-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V power supply.
2	OE1	I,PU	Active high input pin enables DIFF1 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications.
3	VDD	PWR	3.3 V power supply.
4	VSS	GND	Ground.
5	OE2	I,PU	Active high input pin enables DIFF2 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications.
6	VDD	PWR	3.3 V power supply.
7	OE0	I,PU	Active high input pin enables DIFF0 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications.
8	DIFF0	O, DIF	0.7 V, differential clock output.
9	$\overline{\text{DIFF0}}$	O, DIF	0.7 V, differential clock output.
10	DIFF1	O, DIF	0.7 V, differential clock output.
11	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, differential clock output.
12	VDD	PWR	3.3 V power supply.
13	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, differential clock output.

Table 6. Si53154 24-Pin QFN Descriptions

Pin #	Name	Type	Description
14	DIFF2	O, DIF	0.7 V, differential clock output.
15	$\overline{\text{DIFF3}}$	O, DIF	0.7 V, differential clock output.
16	DIFF3	O, DIF	0.7 V, differential clock output.
17	VDD	PWR	3.3 V power supply.
18	OE3	I,PU	Active high input pin enables DIFF3 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications.
19	SCLK	I	SMBus compatible SCLOCK.
20	SDATA	I/O	SMBus compatible SDATA.
21	VDD	PWR	3.3 V power supply.
22	DIFFIN	I	0.7 V Differential True Input, typically 100 MHz. Input frequency range 100 to 210 MHz.
23	$\overline{\text{DIFFIN}}$	O	0.7 V Differential Complement Input, typically 100 MHz. Input frequency range 100 to 210 MHz.
24	VSS	GND	Ground.
25	GND	GND	Ground for bottom pad of the IC.

6. Ordering Guide

Part Number	Package Type	Temperature
Lead-free		
Si53154-A01AGM	24-pin QFN	Extended, –40 to 85 °C
Si53154-A01AGMR	24-pin QFN—Tape and Reel	Extended, –40 to 85 °C

7. Package Outline

Figure 5 illustrates the package details for the Si53154. Table 7 lists the values for the dimensions shown in the illustration.

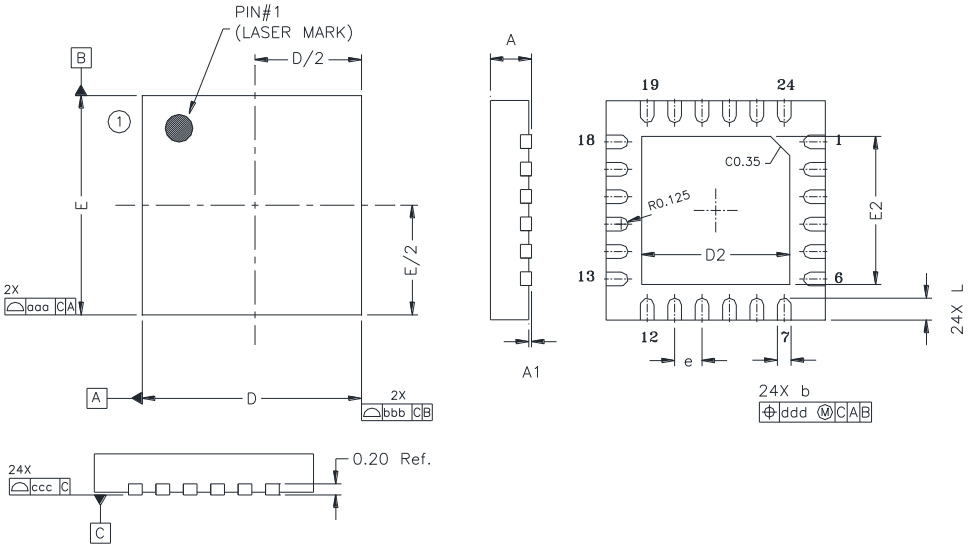


Figure 5. 24-Pin Quad Flat No Lead (QFN) Package

Table 7. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.60	2.70	2.80
e		0.50 BSC	
E		4.00 BSC	
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.07	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 1.0

- Updated Features and Description.
- Updated Table 2.
- Updated Table 3.
- Updated Section 4.1.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

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