Si53325

Dual 1:5 Low Jitter LVPECL Clock Buffer (<1.25 GHz)

Features

- 2 banks of LVPECL outputs
- Ultra-low additive jitter: 100 fs rms
- Wide frequency range: 1 MHz to 1.25 GHz
- Input compatible with LVPECL, LVDS, CML, HCSL, LVCMOS
- Low output-output skew: <50 ps
- Low propagation delay variation: <400 ps
- V_{REF} reference voltage for single-ended input clocking
- RoHS compliant, Pb-free
- 32-QFN, 32-eLQFP
- Industrial temperature range: –40 to +85°C
- Footprint-compatible with MC100LVEP210

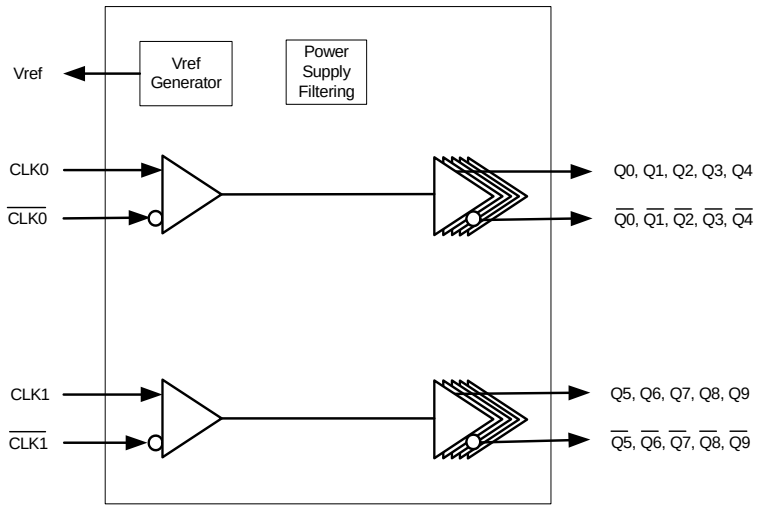
Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

Description

The Si53325 is an ultra low jitter dual 1:5 LVPECL buffer. The Si53325 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from 1 MHz to 1.25 GHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53325 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments.

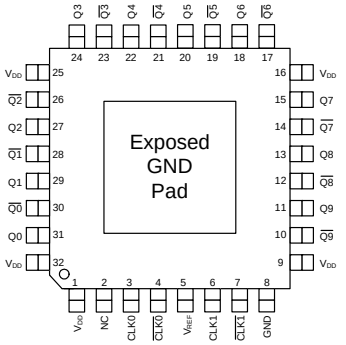
Functional Block Diagram

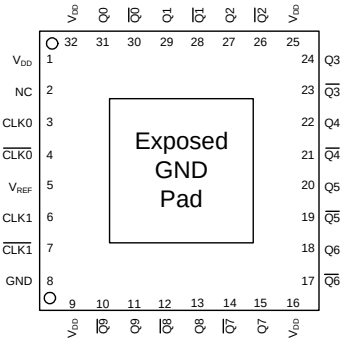


Ordering Information:
See page 17.

Pin Assignments

Si53325





Patents pending

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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A		–40	—	85	°C
Supply Voltage Range*	V_{DD}	LVPECL	2.38	2.5	2.63	V
			2.97	3.3	3.63	V

Table 2. Input Clock Specifications

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	V_{CM}	VDD = 2.5 V± 5%, 3.3 V± 10%	0.05	—	—	V
Input Swing (single-ended, peak-to-peak)	V_{IN}		0.1	—	1.1	V
Input Voltage High	V_{IH}		VDD x 0.7	—	—	V
Input Voltage Low	V_{IL}		—	—	VDD x 0.3	V
Input Capacitance	C_{IN}		—	5	—	pF

Table 3. DC Common Characteristics

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	TBD	450	mA
Leakage Current	I_L	Input leakage at all inputs except CLKIN, V_{IN} = 0 V	—	—	TBD	µA
		Input leakage at CLKIN V_{IN} = 0 V	—	—	TBD	µA
Voltage Reference	V_{REF}	V_{REF} pin	—	VDD/2	—	V

Table 4. DC Characteristics—LVPECL

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High	V_{OH}	R_L = 50 Ω to V_{DDOX} – 2 V	V_{DDOX} – 1.145	—	V_{DDOX} – 0.895	V
Output Voltage Low	V_{OL}	R_L = 50 Ω to V_{DDOX} – 2 V	V_{DDOX} – 1.945	—	V_{DDOX} – 1.695	V
Output DC Common Mode Voltage	V_{COM}		V_{DDOX} – 1.895	—	V_{DDOX} – 1.425	V
Single-Ended Output Swing	V_{SE}	Terminate unused outputs to R_L = 50 Ω to V_{DDOX} – 2 V	0.25	0.60	0.85	V

Table 5. AC Characteristics

(V_{DD} = 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	LVPECL	1	—	1250	MHz
Duty Cycle **Note:** 50% input duty cycle.	D_C	20/80% T_R/T_F<10% of period (Differential)	48	50	52	%
Minimum Input Clock Slew Rate[1]	SR	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns
Output Rise/Fall Time	T_R/T_F	LVPECL, 20/80%			350	ps
Minimum Input Pulse Width	T_W		500	—	—	ps
Additive Jitter (Differential Clock Input)	J	V_{DD} = 2.5/3.3 V, LVPECL, F = 725 MHz, 0.75 V/ns input slew rate	—	60	80	fs
Propagation Delay	T_{PLH}, T_{PHL}	Low to high, high to low Single-ended	TBD	—	TBD	ns
		Low to high, high to low Differential	TBD	—	TBD	ns
Output to Output Skew	T_{SK}	Identical Configuration, Single-ended (Q_N to Q_M)	—	—	100	ps
		Identical Configuration, Differential (Q_N to Q_M)	—	—	50	ps
Part to Part Skew[3]	T_{PS}	Identical configuration	—	50	—	ps

Notes:

1. For clock division applications, a minimum input clock slew rate of 30 mV/ns is required.
2. See Figure 4.
3. Defined as skew between outputs on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} (1.8 V = 50 mV_{PP}, 2.5/3.3 V = 100 mV_{PP}) and noise spur amplitude measured. See AN491 for further details.

Table 6. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
32-eLQFP Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	54.9	°C/W
32-eLQFP Thermal Resistance, Junction to Case	θ_{JC}	Still air	38.0	°C/W
32-QFN Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	49.6	°C/W
32-QFN Thermal Resistance, Junction to Case	θ_{JC}	Still air	32.3	°C/W

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	T_S		–55	—	150	°C
Supply Voltage	VDD		–0.5	—	3.8	V
Input Voltage	V_{IN}		–0.5	—	VDD+ 0.3	V
Output Voltage	V_{OUT}		—	—	VDD+ 0.3	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	2000	—	—	V
ESD Sensitivity	CDM		500	—	—	V
Peak Soldering Reflow Temperature	T_{PEAK}	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	T_J		—	—	125	°C

Note: Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. Functional Description

The Si53325 is an ultra low jitter dual 1:5 LVPECL buffer. The device has a universal input that accepts most common differential or LVCMOS input signals.

2.1. Universal, Any-Format Input

The Si53325 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 8 and 9 summarize the various input ac- and dc-coupling options supported by the device. Figures 1 and 2 show the recommended input clock termination options.

Table 8. LVPECL, LVCMOS, and LVDS

	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	No	Yes	Yes	No
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

Table 9. HCSL and CML

	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	No	No	Yes	No
2.5/3.3 V	No	Yes (3.3 V)	Yes	No

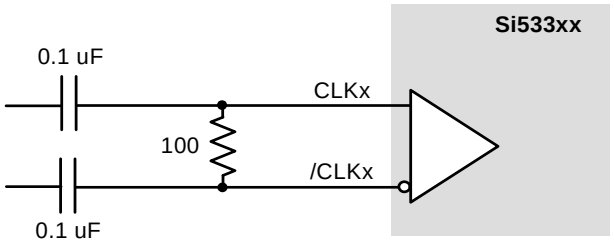


Figure 1. Differential LVPECL, LVDS, CML AC-Coupled Input Termination

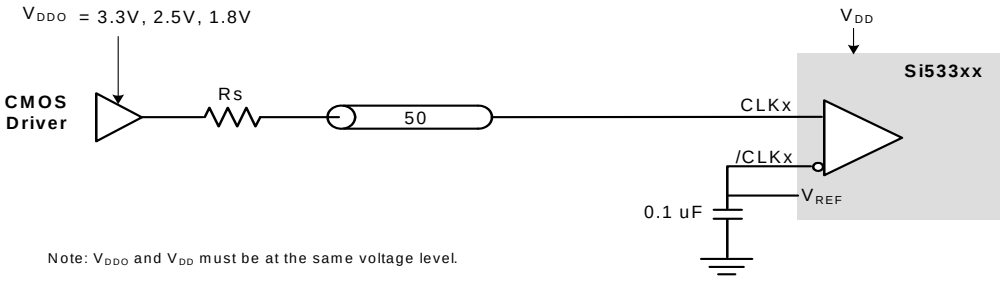
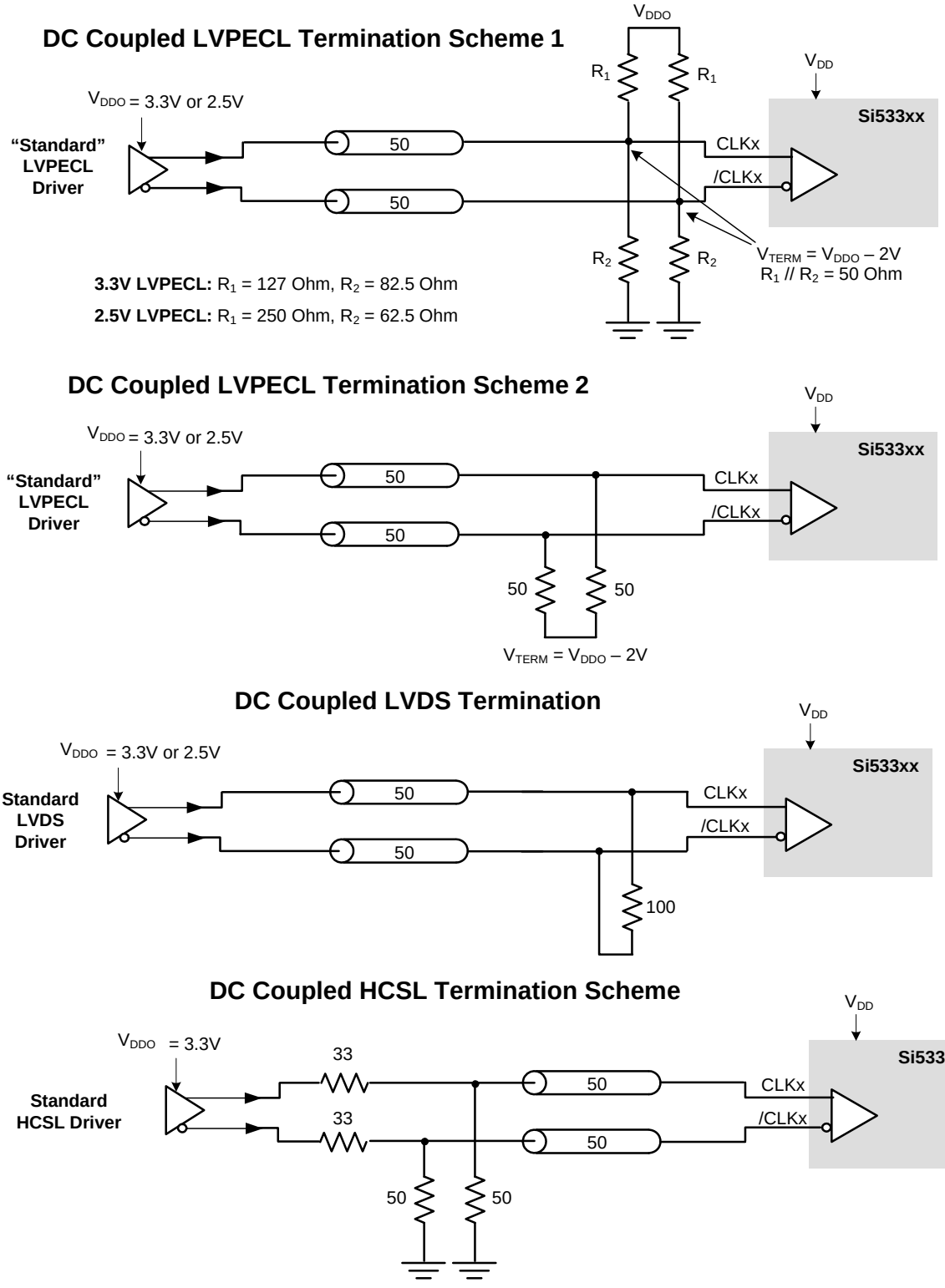


Figure 2. LVCMOS DC-Coupled Input Termination



Note: 33 Ohm series termination is optional depending on the location of the receiver.

Figure 3. Differential DC-Coupled Input Terminations

2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The noninverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to V_{DD}. The inverting input is biased with a 75 kΩ pullup to V_{DD}.

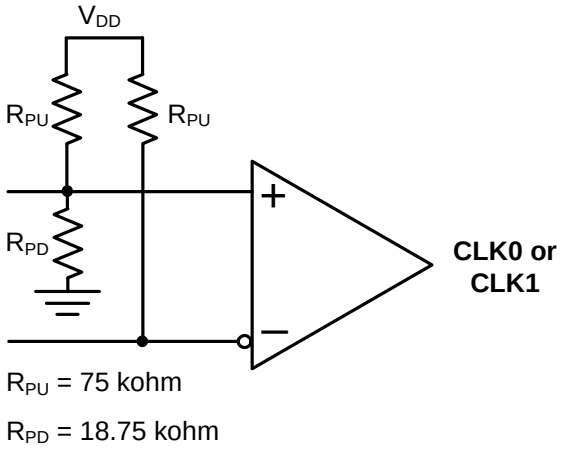
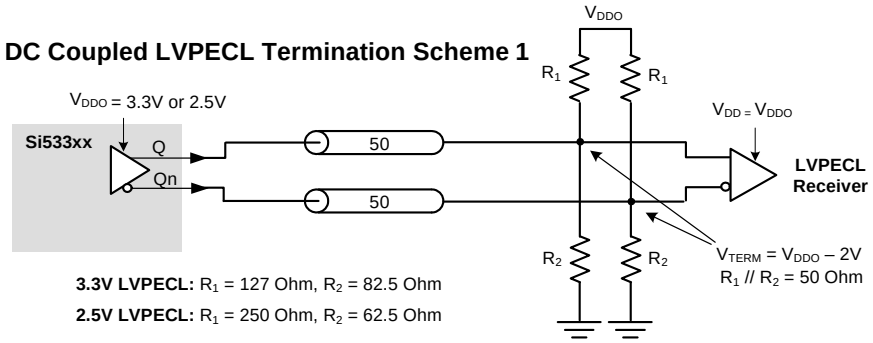
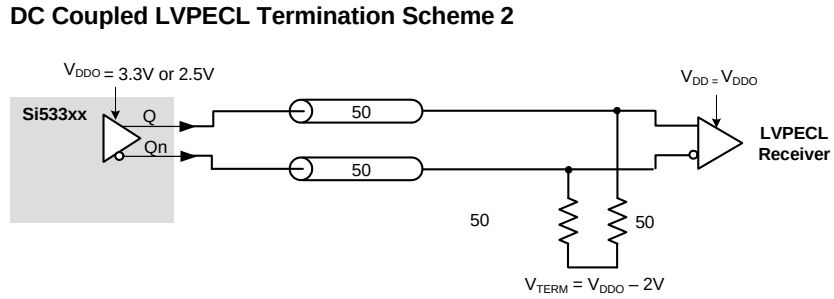


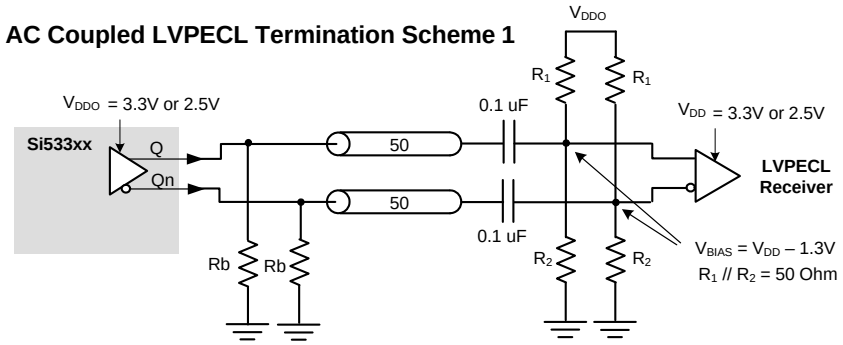
Figure 4. Input Bias Resistors

2.3. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused output clocks should be left floating.







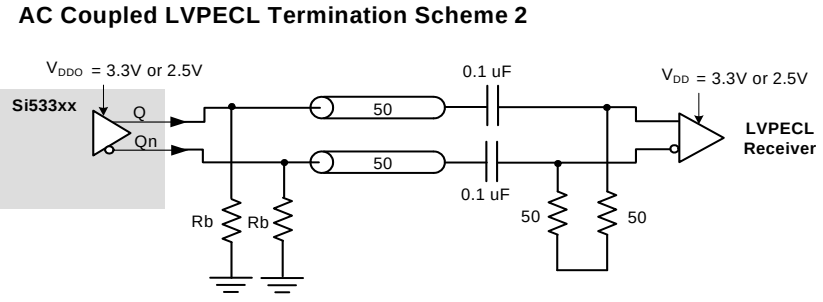


Figure 5. LVPECL Output Termination

2.4. AC Timing Waveforms

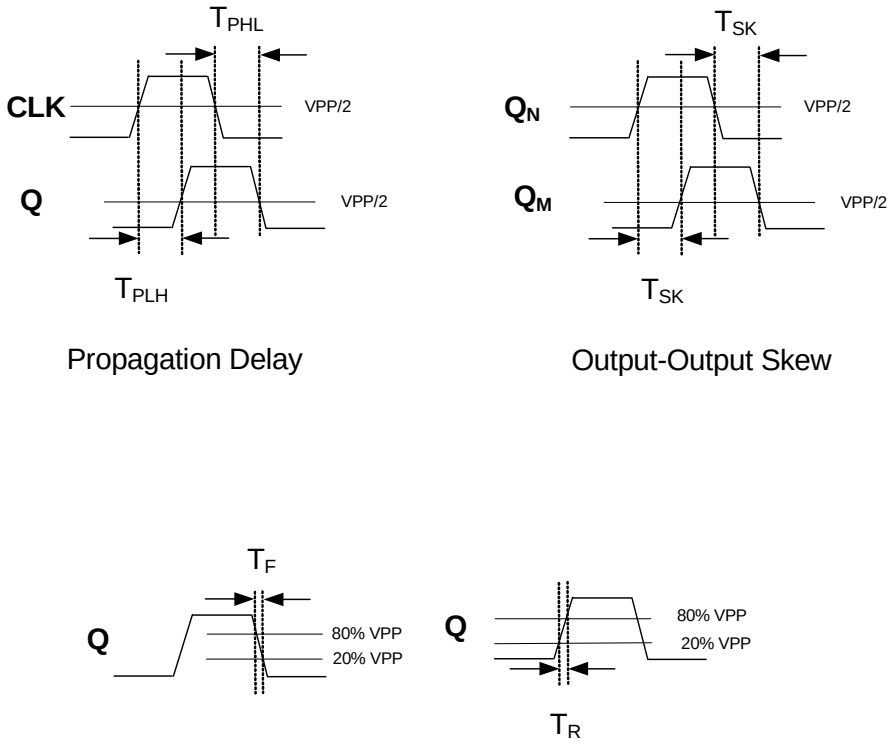
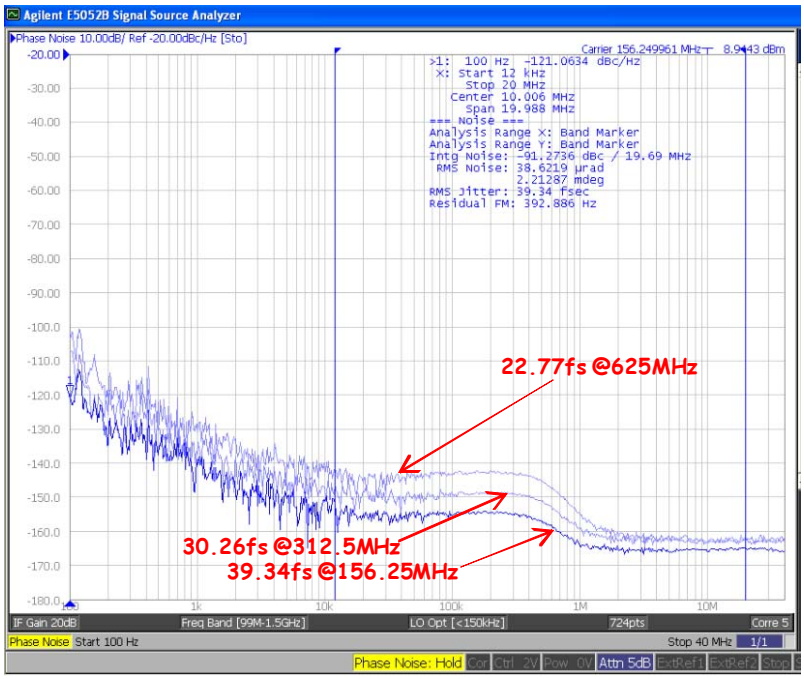
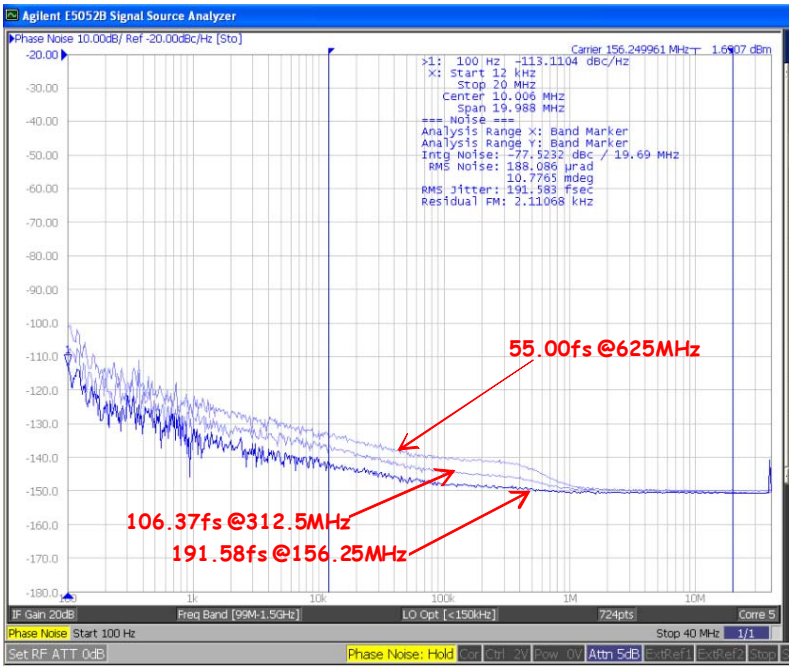


Figure 6. AC Waveforms

2.5. Typical Phase Noise Performance



Source Jitter



Total Jitter

Figure 7. Si53325 Phase Noise

Note: Measured single-endedly.

Table 10. Si53325 Additive Jitter

Frequency (MHz)	Source Jitter (fs)	Total Jitter (fs)	Additive Jitter (fs)
156.25	39.34	191.58	187.50
312.5	30.26	106.37	101.98
625	22.77	55.00	50.07

3. Pin Description: 32-eLQFP, 32-QFN

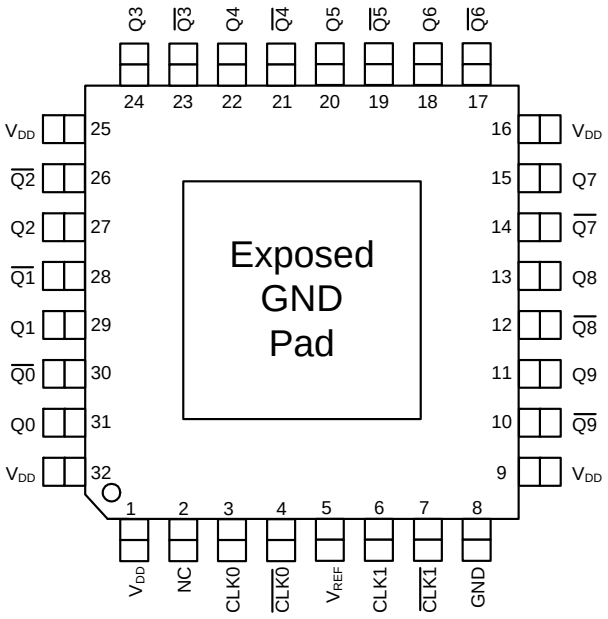


Figure 8. 32-eLQFP Pin Diagram

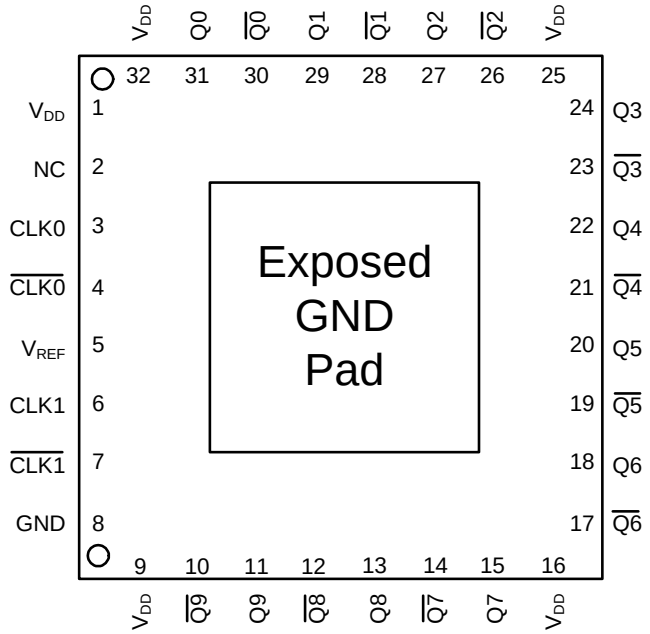


Figure 9. 32-QFN Pin Diagram

Table 11. Si53325 32-eLQFP and 32-QFN Pin Descriptions

Pin #	Name	Description
1	V_{DD}	Core voltage supply. Bypass with 1.0 μF capacitor and place as close to the V_{DD} pin as possible.
2	NC	No connect.
3	CLK0	Input clock 0.
4	$\overline{CLK0}$	Input clock 0 (complement).
5	V_{REF}	Input reference voltage. When driven by a LVCMOS clock input, connect the unused clock input to V_{REF} and a 0.1 μF cap to ground. When driven by a differential clock, do not connect the V_{REF} pin.
6	CLK1	Input clock 1.
7	$\overline{CLK1}$	Input clock 1 (complement).
8	GND	Ground.
9	V_{DD}	Core voltage supply. Bypass with 1.0 μF capacitor and place as close to the V_{DD} pin as possible.
10	$\overline{Q9}$	Output clock 9 (complement).
11	Q9	Output clock 9.
12	$\overline{Q8}$	Output clock 8 (complement).
13	Q8	Output clock 8.
14	$\overline{Q7}$	Output clock 7 (complement).
15	Q7	Output clock 7.
16	V_{DD}	Core voltage supply. Bypass with 1.0 μF capacitor and place as close to the V_{DD} pin as possible.
17	$\overline{Q6}$	Output clock 6 (complement).
18	Q6	Output clock 6.
19	$\overline{Q5}$	Output clock 5 (complement).
20	Q5	Output clock 5.
21	$\overline{Q4}$	Output clock 4 (complement).
22	Q4	Output clock 4.
23	$\overline{Q3}$	Output clock 3 (complement).
24	Q3	Output clock 3.
25	V_{DD}	Core voltage supply. Bypass with 1.0 μF capacitor and place as close to the V_{DD} pin as possible.

Table 11. Si53325 32-eLQFP and 32-QFN Pin Descriptions (Continued)

Pin #	Name	Description
26	$\overline{Q2}$	Output clock 2 (complement).
27	Q2	Output clock 2.
28	$\overline{Q1}$	Output clock 1 (complement).
29	Q1	Output clock 1.
30	$\overline{Q0}$	Output clock 0 (complement).
31	Q0	Output clock 0.
32	V_{DD}	Core voltage supply. Bypass with 1.0 µF capacitor and place as close to the V_{DD} pin as possible.
33	Exposed ground pad	Ground Pad. The exposed ground pad is thermally connected to the die to improve the heat transfer out of the package. The ground pad must be connected to GND to ensure device specifications are met.

4. Ordering Guide

Part Number	Package	PB-Free, ROHS-6	Temperature
Si53325-B-GQ	32-eLQFP	Yes	–40 to 85 °C
Si53325-B-GM	32-QFN	Yes	–40 to 85 °C

5. Package Outline

5.1. 32-eLQFP Package Diagram

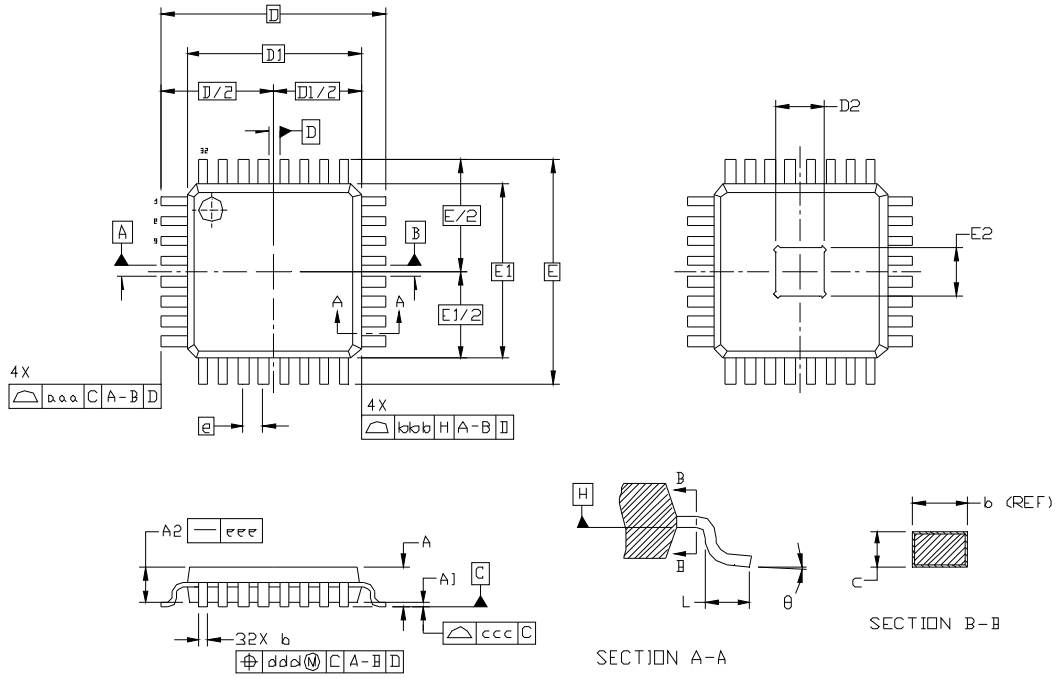


Figure 10. Si53325 32-eLQFP Package Diagram

Table 12. Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
D2	1.87	1.92	1.97
e	0.80 BSC		
E	9.00 BSC		

Dimension	Min	Nom	Max
E1	7.00 BSC		
E2	1.87	1.92	1.97
L	0.45	0.60	0.75
Θ	0°	3.5°	7°
aaa	0.20		
bb	0.20		
ccc	0.10		
dddd	0.20		
eee	0.05		

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC MS-026.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5.2. 32-QFN Package Diagram

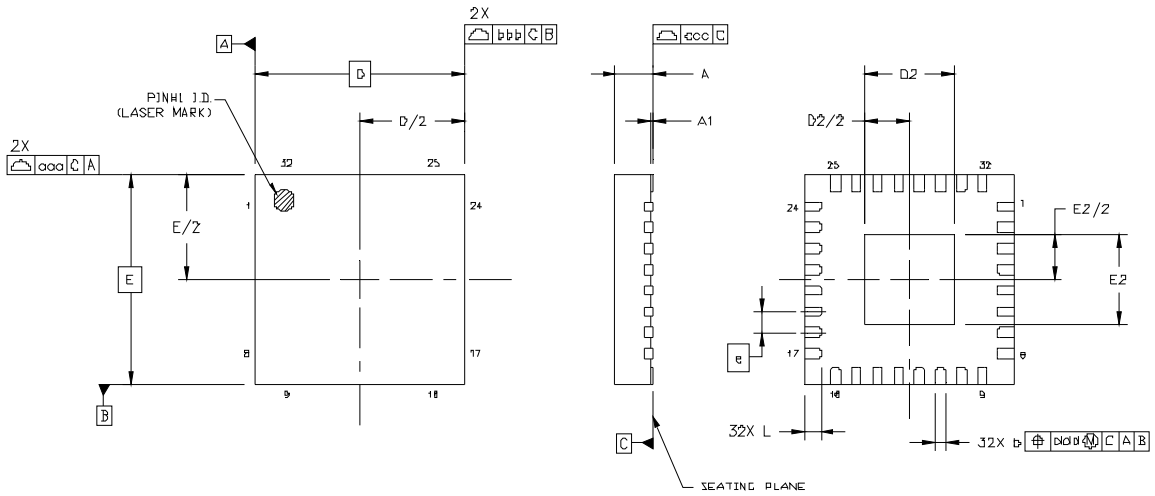


Figure 11. Si53325 32-QFN Package Diagram

Table 13. Package Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.20	0.25	0.30
D	5.00 BSC		
D2	2.00	2.15	2.30
e	0.50 BSC		
E	7.00 BSC		
E2	2.00	2.15	2.30
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC Solid State Outline MO-220.

6. PCB Land Pattern

6.1. 32-eLQFP Package Land Pattern

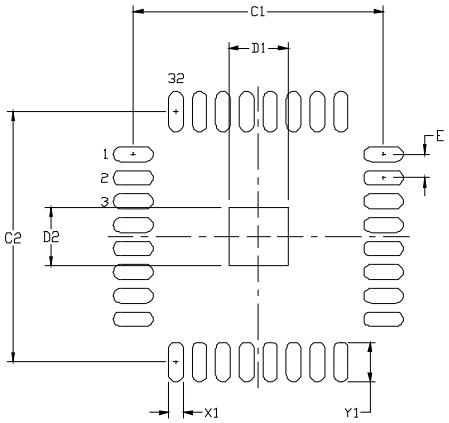


Figure 12. Si53325 32-eLQFP Package Land Pattern

Table 14. PCB Land Pattern

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
D1	1.84	2.00
D2	1.84	2.00
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A single 1.5 x 1.5 mm stencil aperture should be used for the center ground pad to achieve between 50-60% solder coverage.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2. 32-QFN Package Land Pattern

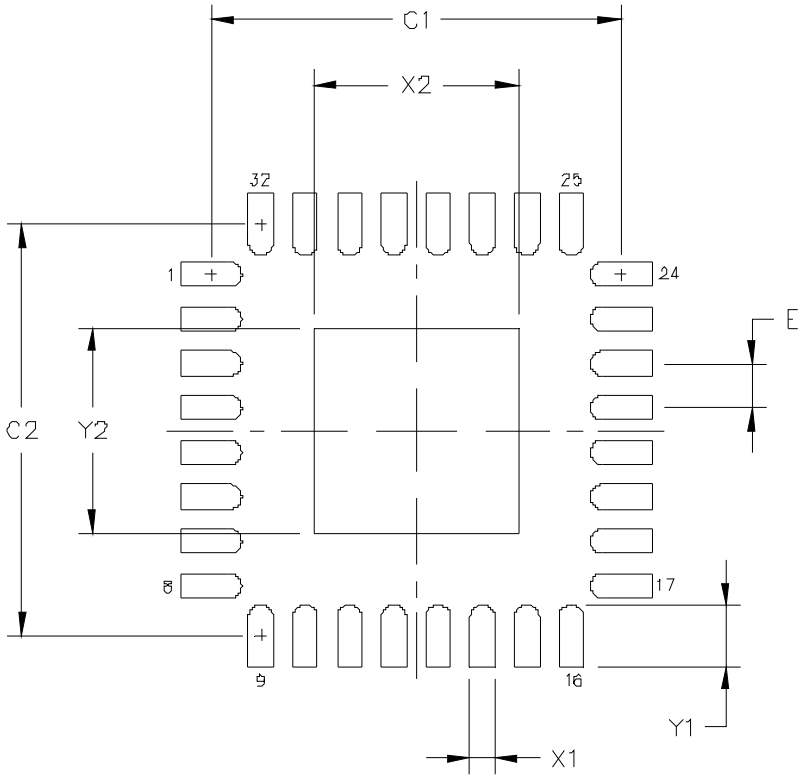


Figure 13. Si53325 32-QFN Package Land Pattern

Table 15. PCB Land Pattern

Dimension	Min	Max	Dimension	Min	Max
C1	4.52	4.62	X2	2.20	2.30
C2	4.52	4.62	Y1	0.59	0.69
E	0.50 BSC		Y2	2.20	2.30
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

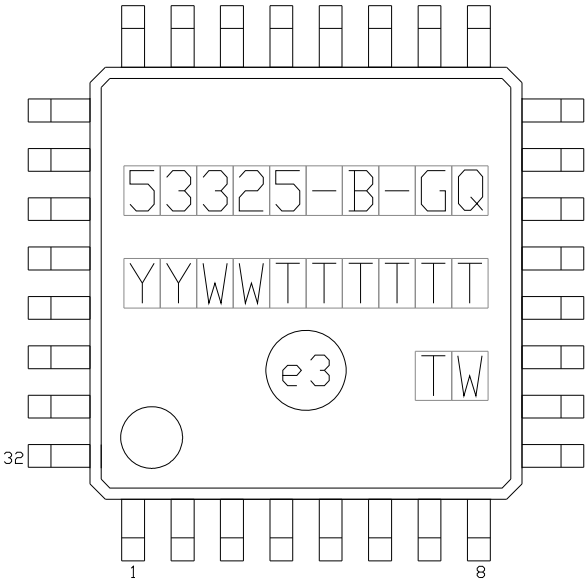
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.75 mm square openings on 1.15 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Markings

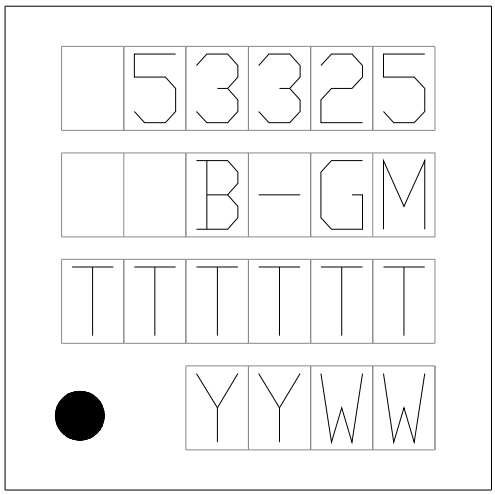
7.1. Si53325 32-eLQFP Top Marking



7.2. Top Marking Explanation (32-eLQFP)

Mark Method:	Laser	
Font Size:	1.9 Point (26 mils) Right-Justified	
Line 1 Marking:	Device Part Number	**53325-B-GQ**
Line 2 Marking:	YY = Year WW = Work Week	Assigned by Assembly Supplier. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.3 mm Diameter Center-Justified	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	**TW**

7.3. Si53325 32-QFN Top Marking



7.4. Top Marking Explanation (32-QFN)

Mark Method:	Laser	
Font Size:	2.0 Point (28 mils) Center-Justified	
Line 1 Marking:	Device Part Number	**53325**
Line 2 Marking:	Device Revision/Type	**B-GM**
Line 3 Marking:	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 4 Marking	Circle = 0.50 mm Diameter Lower-Left Justified	Pin 1 Identifier
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

CONTACT INFORMATION

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