TSW3082 and DAC5682z EVM

Contents

1 Demonstration Kit Configuration Options 2
1.1 DAC Component 2
1.2 Board Configuration 3
1.3 VCXO 4
1.4 LO Source 4
2 Block Diagrams 4
2.1 System Block Diagram 4
2.2 Demo Kit Block Diagram 5
3 Key Texas Instruments Components 6
3.1 CDCM7005 6
3.2 DAC5682 6
3.3 TRF3703 6
4 Software Installation 6
4.1 DAC5682 USB Control Software Installation 6
4.2 DAC5682 EVM Driver Installation 9
5 DAC5682 EVM Software 10
5.1 Software Functionality Overview 10
5.2 EVM Home Area 11
5.3 DAC5682z Register Configuration and Block Diagram 13
5.4 CDCM7005 Register Configuration 15
5.5 TSW3100 Configuration and Pattern Generation 17
5.6 Help 18
6 Introduction 18
6.1 Jumper Settings 18
6.2 Input/Output Connectors 18
6.3 USB Interface 19
6.4 Power Management 19
7 Demo Kit Test Configuration 20
7.1 Test Setup Block Diagram 20
7.2 Test Equipment 20
7.3 Calibration 20
7.4 Typical Performance Measurements 21
8 Initial Power Up and Test 22
8.1 Initial Inspection 22
8.2 Engage Power Supplies 22
8.3 Verify the Status of the Board 22
8.4 Program the CDCM7005 22
8.5 Program the DAC5682z 23
8.6 Carrier Suppression 23
9 Optional Configurations 23
9.1 External VCXO 23
9.2 RF or DAC Output 23
10 Baseband Filter 24
10.1 RF Output Matching Filter 24

11 Bill of Materials and Schematics 25
11.1 Bill of Materials 25
11.2 Schematics 27

List of Figures

1 DAC5682Z Resistor Jumper Configuration 3
2 TSW3082 Resistor Jumper Configuration 3
3 System Block Diagram 4
4 TSW3082 Block Diagram 5
5 DAC5682 USB Control Software Installation CD Contents 6
6 Destination Directory 7
7 License Agreement 7
8 Start Installation 8
9 Warning about Windows Logo Testing 8
10 Restart PC Necessary 8
11 Found New Hardware Wizard 9
12 How should the Wizard Install the DAC5682 Software 10
13 EVM Home Displaying EVM Status Settings 12
14 DAC5682Z Block Diagram and Register Configuration Settings 13
15 The CDCM7005 and DAC5682 Register Configuration Settings 15
16 TSW3100 Pattern Generator and DAC5682 Register Configuration Settings 17
17 TSW3082 EVM Driven by TSW3100 Pattern Generator 20
18 DAC5682 EVM Transformer Output With a Low IF at 30.72 MHz 21
19 TSW3082 EVM output at RF LO + low IF of 30.72M (6 dB lower than DAC output) 22
20 Response of Default Baseband Filter 24

List of Tables

1 Software Main Menu Selections 10
2 Software Area Descriptions 11
3 EVM Home Software Functionality 12
4 DAC8652Z Register Configuration Software Functionality 13
5 CDCM7005 Register Configuration Software Functionality 16
6 TSW3100 Configuration and Pattern Generation Functionality 17
7 Jumper Functions 18
8 Input and Output Connectors 18

1 Demonstration Kit Configuration Options

The TSW3082 and DAC5682z EVM Demonstration (Demo) Kit can be configured in different ways to evaluate different components in different frequency bands. This section outlines the component configurations. Based on the configuration, testing and board setup must be altered to accommodate the given components and features.

1.1 DAC Component

The TSW3082 and DAC5682z EVM are built for the DAC5682z.

1.2 Board Configuration

The analog quadrature modulator requires a common-mode DC voltage of approximately 3.3V. In order to use the dc-offset adjustment capabilities of the DAC5682 for carrier suppression, it is imperative to maintain a dc path from the DAC output to the modulator input. The common-mode voltage for the modulator is maintained with a passive resistor network that is designed to provide the proper operation point for the DAC5682 and the TRF3703 modulator. By design, in order to preserve the proper dc levels, the DAC coarse gain should be kept at the maximum (15), though deviation by a few steps is generally acceptable with no degradation in performance.

The resistor network can be configured such that the DAC output is routed to a transformer which defines the board as a DAC5682z EVM or routed to the TRF3703 which results in the TSW3082 EVM.

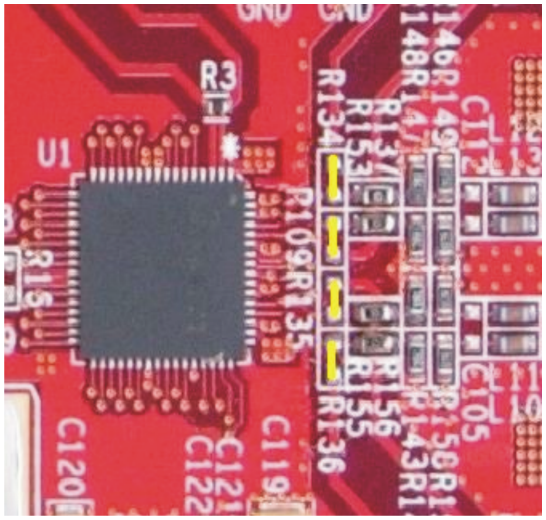

Figure 1. DAC5682Z Resistor Jumper Configuration

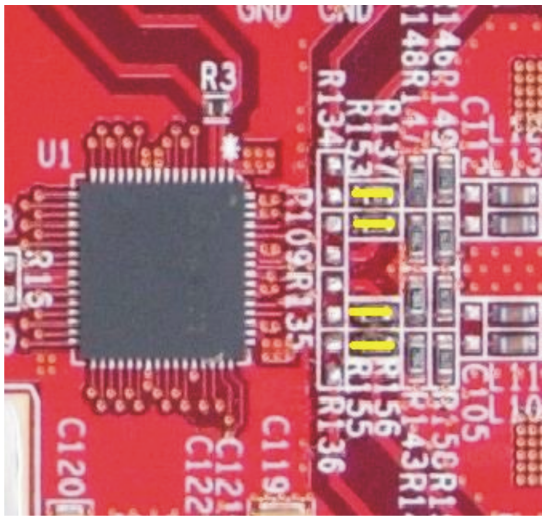

Figure 2. TSW3082 Resistor Jumper Configuration

1.3 VCXO

The CDCM7005 requires a VCXO or external clock source to derive its output clock signals. The VCXO is at reference designator U6. This TSW3082 and DAC5682z EVM release does not have a VCXO and requires an external clock source on SMA J6. The VCXO can be changed to operate the Demo Kit with different clocking schemes for different modulation standards or for specific customer requirements. Use the VCXO or external clock frequency to properly configure the CDCM7005 (see **Section 2** of Figure 15).

These conventions are typically used:

- WCDMA—derivatives of 61.44 MHz
- GSM—derivatives of 52 MHz
- CDMA2K—derivatives of 78.6432 MHz
- WiMAX—derivatives of 112 MHz

1.4 LO Source

The TSW3082 requires an external Local Oscillator (LO) source to drive the on board TRF3703-33 modulator. This external LO input can be connected at SMA connector J23. The signal level of the LO source should comply with the requirements in the TRF3703 data sheet (SLWS184), but typically an LO power around 0 to 3 dBm is adequate.

2 Block Diagrams

2.1 System Block Diagram

The basic radio system block diagram in Figure 3 demonstrates where the TSW3082 Demo Kit fits in the overall transceiver. The dash-line box illustrates the components found on the TSW3082 Demo Kit board.

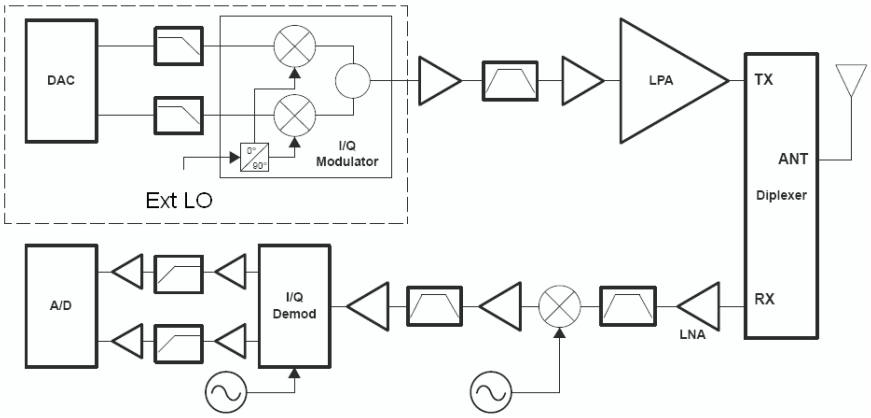

Figure 3. System Block Diagram

2.2 Demo Kit Block Diagram

The basic Demo Kit block diagram is shown in Figure 4. The shaded boxes illustrate the key Texas Instruments components found on the TSW3082 Demo Kit board.

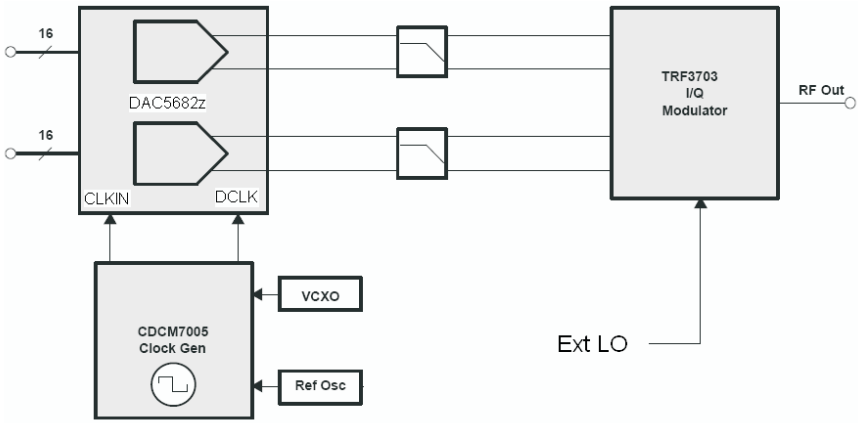

Figure 4. TSW3082 Block Diagram

3 Key Texas Instruments Components

3.1 CDCM7005

The CDCM7005 clock distribution chip is used to generate and synchronize the clock outputs to the system. The device has five outputs which can be either LVPECL or LVCMOS, and can be divided down by 1, 2, 3, 4, 6, 8, and 16. The divide by 16 can be replaced with a divide by 4 or 8 with a 90 degree phase shift. See the CDCM7005 data sheet (SCAS793) for more information.

3.2 DAC5682

The DAC5682 is a 16-bit interpolating dual digital-to-analog converter (DAC) with a high speed LVDS data interface. The device incorporates a digital complex coarse mixer, independent differential offset control, and I/Q amplitude control. The device can be used with excellent results in baseband mode, low IF mode, as well as in high IF mode with an analog quadrature modulator. See the DAC5682 data sheet (SLLS853) for more information.

3.3 TRF3703

The TRF3703 is a direct upconversion (DUC) IQ modulator. This device accepts a differential input voltage quadrature signal at baseband or low IF frequencies and outputs a modulated RF signal based on the LO drive frequency. See the TRF3703 data sheet (SLWS184) for more information.

4 Software Installation

The enclosed CD-ROM contains all of the necessary software needed for the host PC to control the DAC5682Zz and CDCM7005. The interface software is a Graphical User Interface (GUI) that can program all the registers in the CDCM7005 and the DAC5682z. Once the software is installed, the GUI is accessible from the **Start** → **All Programs** → **Texas Instruments DACs** → **DAC5682z EVM Control**.

4.1 DAC5682 USB Control Software Installation

The installation CD contains the files and folders shown in Figure 5.

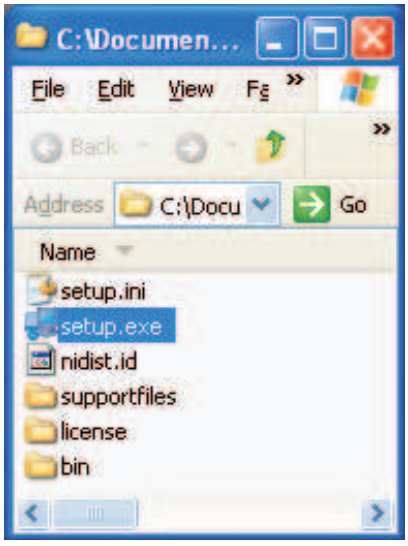

Figure 5. DAC5682 USB Control Software Installation CD Contents

1. Double-click the **setup.exe** file (Figure 5) to start the DAC5682z control software installation.
2. The destination folder for the installed software displays (Figure 6). TI recommends you accept the default folder location. Any necessary folders are created by the installation software, if they do not

exist. Click *Next*.

3. Select the *I accept the License Agreement(s)* option (Figure 7) and click *Next*.
4. Click *Next* (Figure 8) to start the installation.
5. Click *Continue Anyway* (Figure 9) to continue the installation.
6. Click *Restart* (Figure 10) to finish the installation.

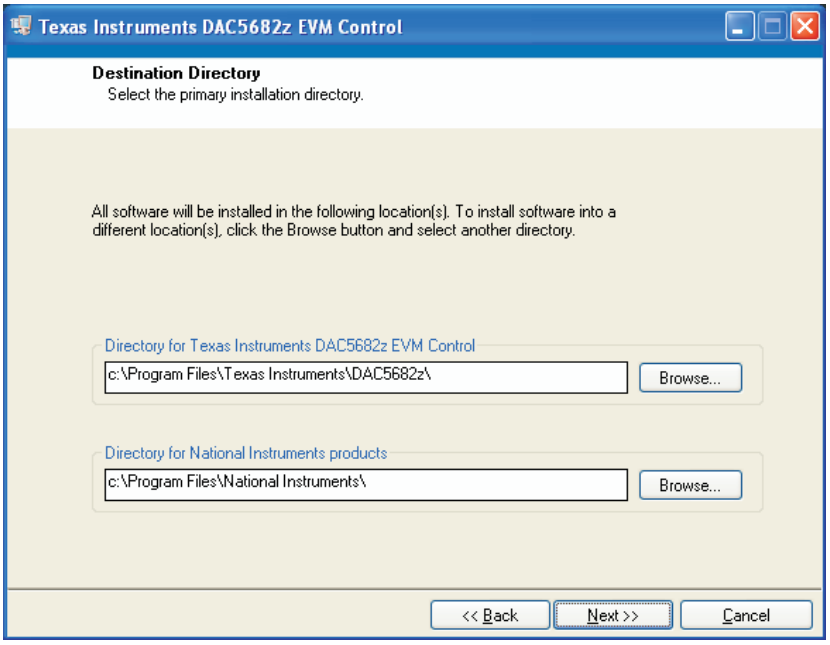

Figure 6. Destination Directory

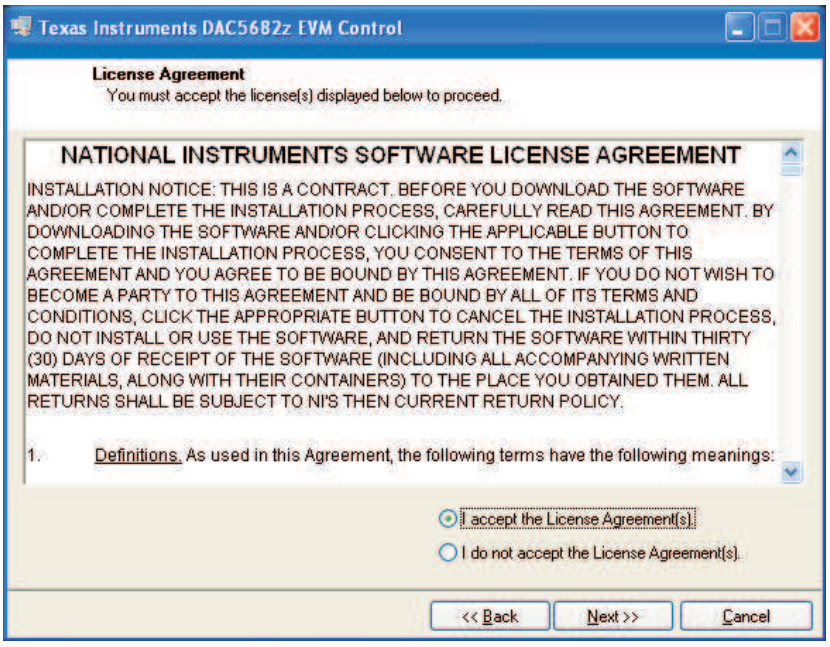

Figure 7. License Agreement

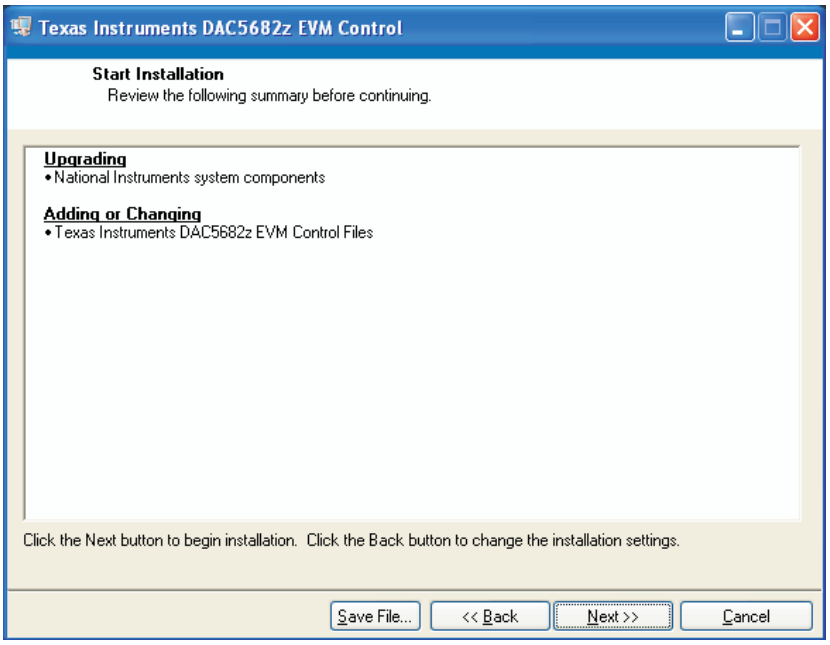

Figure 8. Start Installation

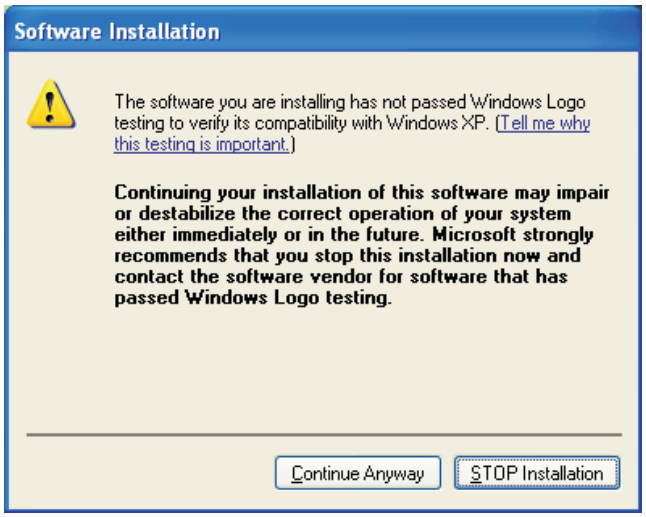

Figure 9. Warning about Windows Logo Testing

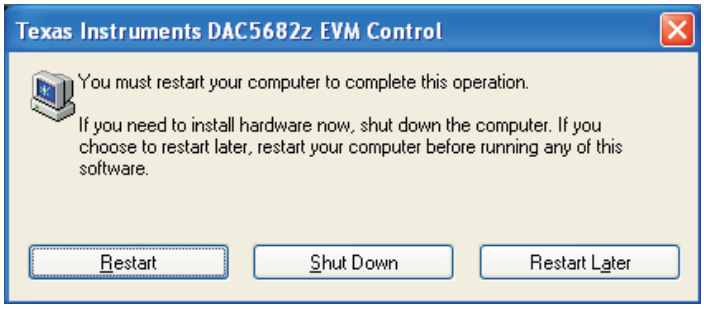

Figure 10. Restart PC Necessary

4.2 DAC5682 EVM Driver Installation

1. Once the PC has restarted, plug in the DAC5682z or TSW3082 EVM. This starts the driver installation process. The Found New Hardware Wizard (Figure 11) detects the DAC5682. When asked if Windows should connect to the Windows Update server to locate drivers, select the *No, not this time* option and click the *Next* button.
2. When asked how do you want the wizard to install the software (Figure 12), select the *Install the software automatically (Recommended}* option.. Click *Next*.
3. Click *Continue* for the digital signature.
4. The drivers were installed during the software installer and will be installed automatically. If asked to overwrite newer drivers, click *Yes*.
5. Click *Finish* to complete the driver installation.

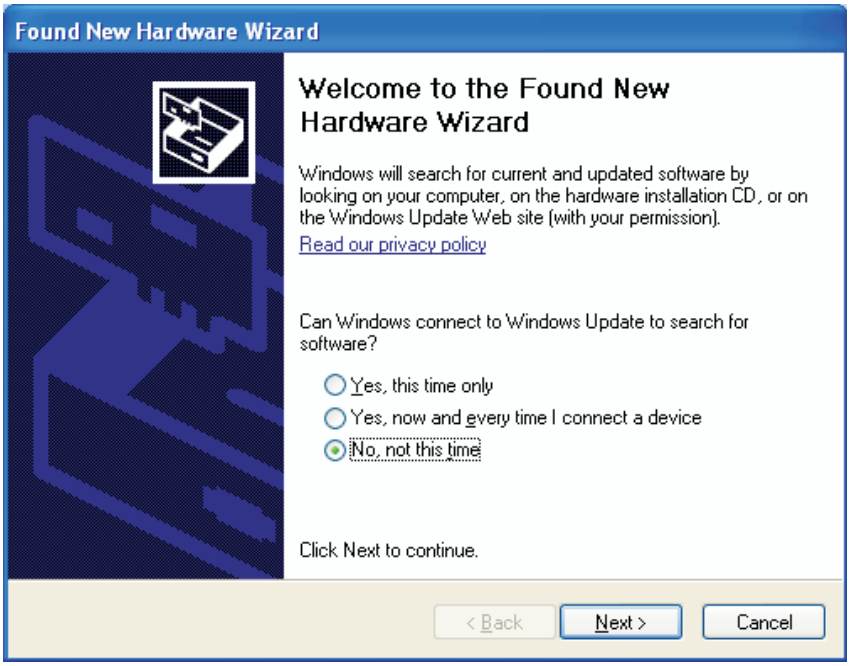

Figure 11. Found New Hardware Wizard

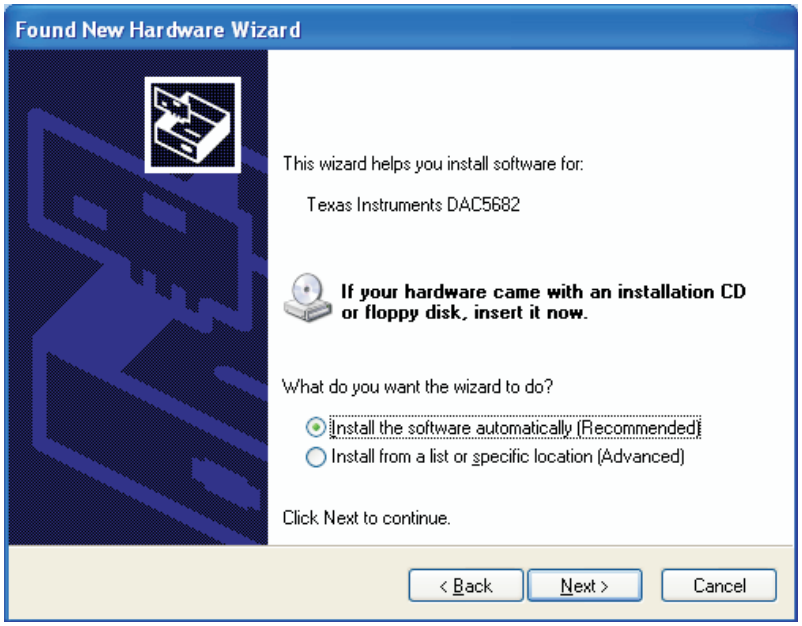

Figure 12. How should the Wizard Install the DAC5682 Software

5 DAC5682 EVM Software

The DAC5682z EVM Control Software is started by accessing the Windows **start** → **All Programs** → **Texas Instruments DACs** cascading menus.

The DAC5682z EVM application helps you to:

- Configure the DAC5682z and CDCM7005 registers.
- Save and load these register settings using text files.
- Visualize the data path through the DAC5682z
- Download a pattern to a TSW3100 Pattern Generator System (link to TSW3100 EVM folder).

5.1 Software Functionality Overview

This section provides you an overview of the software settings and functionality for the entire DAC5682 Graphical User Interface. The software has five groups of settings that help you modify the functionality of the active panels. You can switch between these settings by selecting one of the **Menu** items described in Table 1.

Table 1. Software Main Menu Selections

Menu Item	Top Panel	Bottom Panel	Section Example Screen Functionality Reference
EVM Home	EVM and DAC5682z serial information. EVM communication status	not applicable	Section 5.2 Figure 13 Table 3
DAC5682z Diagram	DAC5682z Register Configuration	DAC5682z data path under the current register settings	Section 5.3 Figure 14 Table 4
Register Config	DAC5682z Register Configuration	CDCM7005 Register Configuration	Section 5.4 Figure 15 Table 5

Table 1. Software Main Menu Selections (continued)

Menu Item	Top Panel	Bottom Panel	Section Example Screen Functionality Reference
TSW3100 Config	DAC5682z Register Configuration	TSW3100 Configuration Pattern Generator display	Section 5.5 Figure 16 Table 6
Help	DAC5682z Register Configuration	DAC5682z data path and help window	Section 5.6

The DAC5682z software interface controls are divided into areas. The functionality of these areas is described in Section 5.2 through Section 5.6.

Table 2. Software Area Descriptions

Area	Description
Menu	Switch between the main functionality settings described in Table 1.
DAC5682Z Home	Displays DAC5682Z part serial information and EVM status.
USB and Readback buttons	Reset the USB port to begin a new data session. Disable DAC5682z read capabilities (simulation mode).
DAC5682z Register Table	Displays DAC5682z register settings in binary and hexadecimal formats.
DAC5682z Register Configuration	Read/Write DAC5682z register configuration.
CDCM7005 Register Configuration	Write CDCM7005 register configuration (no read capability)
DAC5682z Diagram	Graphical representation of the DAC5682z data path under current register configuration.
TSW3100 Configuration	Controls TSW3100 pattern generation system (See TSW3100 User's Guide SLLU101 for more information)
Help	Information about specific DAC5682z register configuration GUI controls

Figure 13 through Figure 16 displays some of the Menu software areas.

5.2 EVM Home Area

The EVM Home Area includes these GUI controls:

- **Menu**—switches between the major functionality listed in Table 1 and displayed in Figure 13.
- **Home**—displays DAC5682Z part information and EVM status.
- **USB/Readback**—reset the USB port to begin a new data session. Disable DAC5682z read capabilities (simulation mode).
- **DAC5682z Register Table**—displays DAC5682Z register settings in binary and hexadecimal formats (Figure 14 - **Regs**).

Note: The numbers on Figure 13 through Figure 16 correspond to the numbered graphical user interface subareas **(X)**, described in each table for the DAC5682z EVM software functionality.

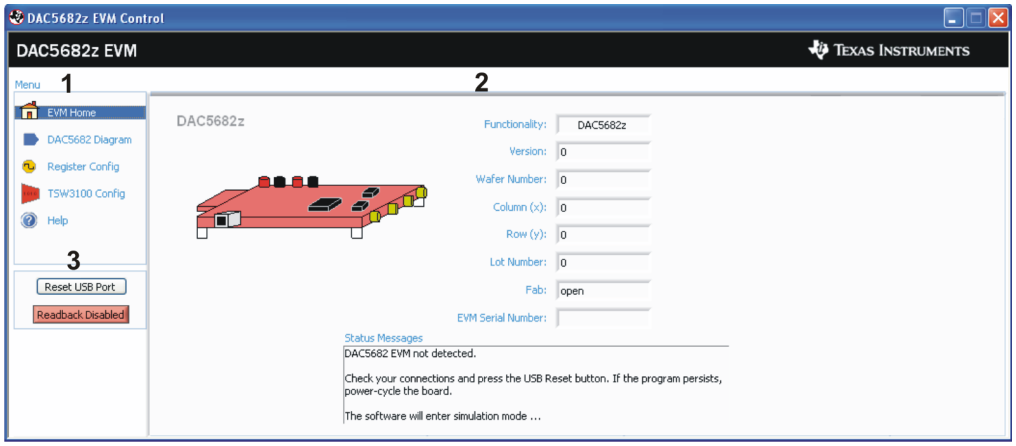

Figure 13. EVM Home Displaying EVM Status Settings

Table 3. EVM Home Software Functionality

Subarea Name	Input Output	Description
Menu Area (1)		
EVM Home	Input	DAC5682z EVM Home area - part number information and EVM status messages
DAC5682z Diagram	Input	DAC5682z Register Configuration and DAC5682z Diagram areas
Register Config	Input .	DAC5682z and CDCM7005 Register Configuration areas
TSW3100 Config	Input	DAC5682z Register Configuration and TSW3100 Configuration areas
Help	Input	Help area
DAC5682z EVM Home Area (2)		
Functionality	Output	DAC device
Version	Output	Chip version
Wafer number	Output	DAC5682z wafer number
Column (x)	Output	DAC5682z column position
Row (y)	Output	DAC5682z row position
Lot Number	Output	DAC5682z lot number
Fab	Output	Fabrication facility where the DAC5682z was manufactured
EVM Serial Number	Output	Serial number for this EVM
Status Messages	Output	Displays the status of the communication session.
USB / Readback Area (3)		
Reset USB Port	Input	Begins a new USB session. Click this button if you see a status error message.
Readback	Input/Output	Disables DAC5682z register reads (simulation mode)
DAC5682z Register Table Area (See Figure 14, Figure 15, and Figure 16)		
Register Table	Output	Displays the DAC5682z register configuration in binary and hexadecimal formats for all menu settings.

5.3 DAC5682z Register Configuration and Block Diagram

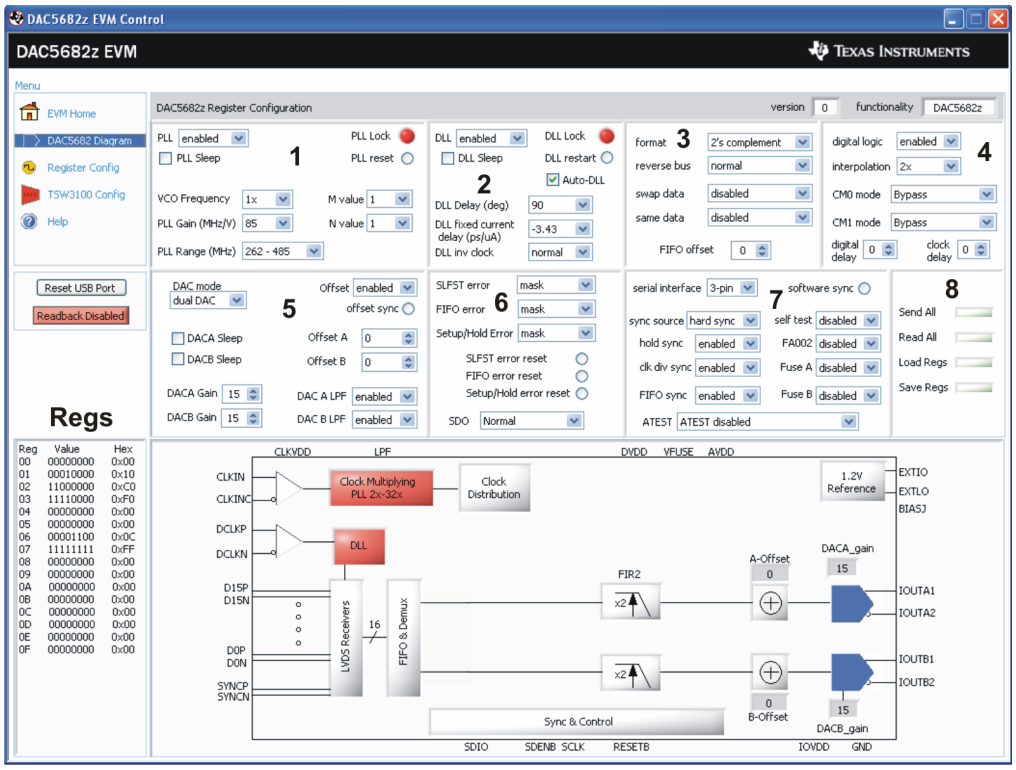

Figure 14. DAC5682Z Block Diagram and Register Configuration Settings

Table 4. DAC8652Z Register Configuration Software Functionality

Subarea Name	Input Output	Description of Functionality (GUI Setting)
PLL Settings (1)		
PLL	Input/Output	Phased-locked Loop (PLL) is bypassed (*disabled*)
PLL Sleep	Input/Output	PLL is put into sleep mode (*selected*)
PLL Lock	Output	Internal PLL is locked (*Green*)
PLL Reset	Input/Output	PLL loop filter is pulled down to 0V (*set*). Toggle to restart the PLL if an over-speed lock-up occurs.
VCO Frequency	Input/Output	PLL clock output is one-half the PLL VCO frequency (*2x*). Runs the VCO at twice the needed clock frequency to reduce phase noise for lower input clock rates.
PLL Gain (MHz/V)	Input/Output	Adjust the PLL Voltage Controlled Oscillator (VCO) gain.
PLL Range (MHz)	Input/Output	Sets the PLL VCO frequency range.
M value	Input/Output	M portion of the M/N divider of the PLL.
N value	Input/Output	N portion of the M/N divider of the PLL. This value should be chosen to divide down the input CLK_{IN} to maintain a maximum PFD of 160 MHz.
DLL Settings (2)		
DLL	Input/Output	Delay lock loop (DLL) is bypassed and LVDS data source provides correct setup and hold timing (*disabled*)
DLL Sleep	Input/Output	DLL is put into sleep mode (*selected*)
Auto-DLL	Input	DLL is restarted automatically when DLL settings change, so there is no need to press the DLL restart control (*selected*).
DLL Lock	Output	Internal DLL is locked (*Green*)
DLL restart	Input/Output	Restarts the DLL manually

Table 4. DAC8652Z Register Configuration Software Functionality (continued)

Subarea Name	Input Output	Description of Functionality (GUI Setting)
DLL Delay (deg.)	Input/Output	Manually adjust the DLL delay ± from the DLL fixed current delay.
DLL fixed current delay (ps/μA)	Input/Output	Adjusts the DLL delay line bias current. Used in conjunction with the DLL inv clock to select appropriate delay range for a given DCLK frequency
DLL inv clock	Input/Output	Inverts the internal DLL clock to force convergence to a different solution. Used when the DLL delay adjustment has exceeded the limits of its range.
Input Settings (3)		
format	Input/Output	Select *2's complement* or *offset binary* format.
reverse bus	Input/Output	Reverses the LVDS input data bus so that the MSB to LSB order is swapped (*enabled*)
swap data	Input/Output	A/B data paths are swapped prior to routing to the DACA and DACB outputs (*enabled*)
same data	Input/Output	Data routed to DACA is also routed to DACB (*enabled*)
FIFO offset	Input/Output	Sets the FIFO's output pointer location, allowing the input pointer to be shifted –4 to +3 positions upon SYNC. Default offset is *0* and is updated upon each sync event.
Digital Settings (4)		
digital logic	Input/Output	Uses the interpolation filters (*enabled*)
interpolation	Input/Output	Selects the interpolation rate.
CM0 mode	Input/Output	Determines the mode of FIR0 and CMIX0 blocks. Since CMIX0 is located between FIR0 and FIR1, its output is half-rate. Settings apply to both A and B channels.
CM1 mode	Input/Output	Determines the mode of FIR1 and final CMIX1 blocks. Settings apply to both A and B channels.
digital delay	Input/Output	DAC data delay adjustment (0–3 periods of the DAC clock). Used to adjust system level output timing. The same delay is applied to both DACA and DACB data paths.
clock delay	Input/Output	Changes the number of buffers that the input clock goes through. This allows some adjustment of the setup/hold of the handoff between the receivers and the digital section.
DAC Settings (5)		
DAC mode	Input/Output	Selects *dual DAC* mode or *single DAC* mode. Used to select input interleaved data (*dual DAC*).
DACA Sleep	Input/Output	DACA is put into sleep mode (*selected*)
DACB Sleep	Input/Output	DACB is put into sleep mode (*selected*). DACB is not automatically set into sleep mode when configured for single DAC mode. Use this control with *single DAC* mode to get the lowest power configuration for DACA output only.
DACA Gain	Input/Output	Scales the DACA output current in 16 equal steps.
DACB Gain	Input/Output	Scales the DACB output current in 16 equal steps.
Offset	Input/Output	Offset A and Offset B values are summed into the DACA and DACB data paths (*enabled*). Provides a system-level offset adjustment capability that is independent of the input data.
offset sync	Input/Output	Transfers the Offset A and Offset B values to the registers used in the DACA and DACB offset calculations. This control is enabled automatically for any change in the Offset A or Offset B values.
Offset A	Input/Output	Offset adjustment value for the A data path.
Offset B	Input/Output	Offset adjustment value for the B data path.
DAC A LPF	Input/Output	95 kHz low pass filter corner on the DACA current source bias (*enabled*). Uses a 472 Hz filter corner (*disabled*).
DAC B LPF	Input/Output	95 kHz low pass filter corner on the DACB current source bias (*enabled*). Uses a 472 Hz filter corner (*disabled*).
Error Settings (6)		
SLFST Error	Input/Output	Masks out SLFTST Errors.
FIFO Error	Input/Output	Masks out FIFO Errors.
Setup/Hold Error	Input/Output	Masks out Setup/Hold Errors.
SLFST error reset	Input/Output	Asserted when the Digital Self Test (SLFTST) fails. Clear to reset a SLFST error.
FIFO error reset	Input/Output	Asserted when the FIFO pointers overrun each other, causing a sample to be missed. Clear to reset a FIFO error.
Setup/Hold error reset	Input/Output	Any received data pattern other than 0xAAAA or 0x5555 causes this bit to be set. Clear to reset a Setup/Hold error.
SDO	Input/Output	Selects the signal polarity on the SDO pin (*normal* or *inverted*)

Table 4. DAC8652Z Register Configuration Software Functionality (continued)

Subarea Name	Input Output	Description of Functionality (GUI Setting)
SYNC Settings (7)		
serial interface	Input/Output	Selects *3-pin* or *4-pin* serial interface mode.
sync source	Input/Output	Selects the synchronization signal source. If *soft sync* is selected the software sync control is used as the only synchronization input and the LVDS external SYNC input pins (*hard sync*) are ignored.
software sync	Input/Output	Substitute for the LVDS external SYNC input pins for both synchronization and transmit enable control.
hold sync	Input/Output	Enables the sync to the FIFO output HOLD block.
clk div sync	Input/Output	Enables the clock divider sync.
FIFO sync	Input/Output	Enables the FIFO offset sync.
self test	Input/Output	Enables a Digital Self Test (SLFTST) of the core logic.
FA002	Input/Output	Keep *disabled*. Used only for factory test purposes.
Fuse A	Input/Output	Keep *disabled*. Used only for factory test purposes.
Fuse B	Input/Output	Keep *disabled*. Used only for factory test purposes.
ATEST	Input/Output	Keep *disabled*. Used only for factory test purposes.
SEND/SAVE Button Settings (8)		
Send All	Input	Writes all registers to the DAC5682z device.
Read All	Input	Reads all registers from the DAC5682z device. It is rarely necessary to use this as the registers are read every time a DAC5682z control changes.
Load Regs	Input	Loads a DAC5682z register configuration from a text file. Files need to consist of a single column with the register values in hexadecimal format.
Save Regs	Input	Saves a DAC5682z register configuration to a text file.

5.4 CDCM7005 Register Configuration

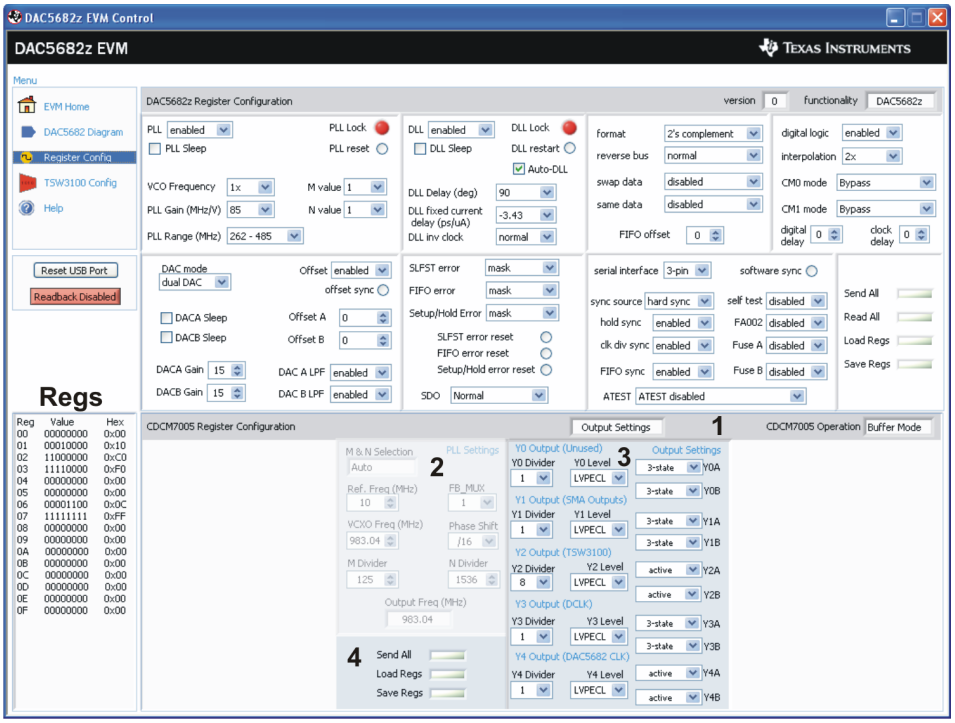

Figure 15. The CDCM7005 and DAC5682 Register Configuration Settings

Table 5. CDCM7005 Register Configuration Software Functionality

Subarea Name	Input Output	Description
General Settings (1)		
Output Settings	Input	Switches the display between the CDCM7005 *output settings* and advanced settings.
CDCM7005 Operation	Input	Select *Buffer Mode* when there is no VCXO installed or the VCXO is enabled. In this case the CDCM7005 operates as a buffer. Select *PLL Mode* when a VCXO is being used by the CDCM7005.
PLL Settings (2)		
M & N Selection	Input	(*Auto*) M and N divider values are calculated automatically based on Reference and VCXO frequencies.
Ref. Freq. (MHz)	Input	Frequency of the reference oscillator given to the CDCM7005.
VCXO Freq. (MHz)	Input	Frequency of the VCXO used.
M Divider	Input/Output	M divider value.
N Divider	Input/Output	N divider value.
FB_MUX	Input/Output	Feedback MUX select.
Phase Shift	Input	Phase shift select.
Output Freq (MHz)	Output	Output frequency of the CDCM7005 based on the Reference and VCXO frequencies, and M and N values. If Output Freq differs from VCXO Freq, Output Freq displays using a red text.
Output Settings (3)		
Y0-Y4 Dividers	Input	Selects the output dividers of the CDCM7005 outputs.
Y0-Y4 Levels	Input	Selects between CMOS or LVPECL levels of the CDCM7005 outputs.
Y0-Y4 States	Input	Selects the operating state of the CDCM7005 outputs.
SEND/SAVE Button Settings (4)		
Send All	Input	Writes all registers to the DCDM7005 device.
Load Regs	Input	Loads a DCDM7005 register configuration from a text file. Files need to consist of a single column with the register values in hexadecimal format.
Save Regs	Input	Saves a DCDM7005 register configuration to a text file.
Advanced Settings (not shown)		
Advanced Registers		Input CDCM7005 advanced registers. See the CDCM7005 data sheet (SCAS793) for more information about these registers.

5.5 TSW3100 Configuration and Pattern Generation

The TSW3100 can be loaded with a custom pattern file using the GUI options. For further details on the file format of the custom pattern, see the TSW3100 Users Guide (SLLU101).

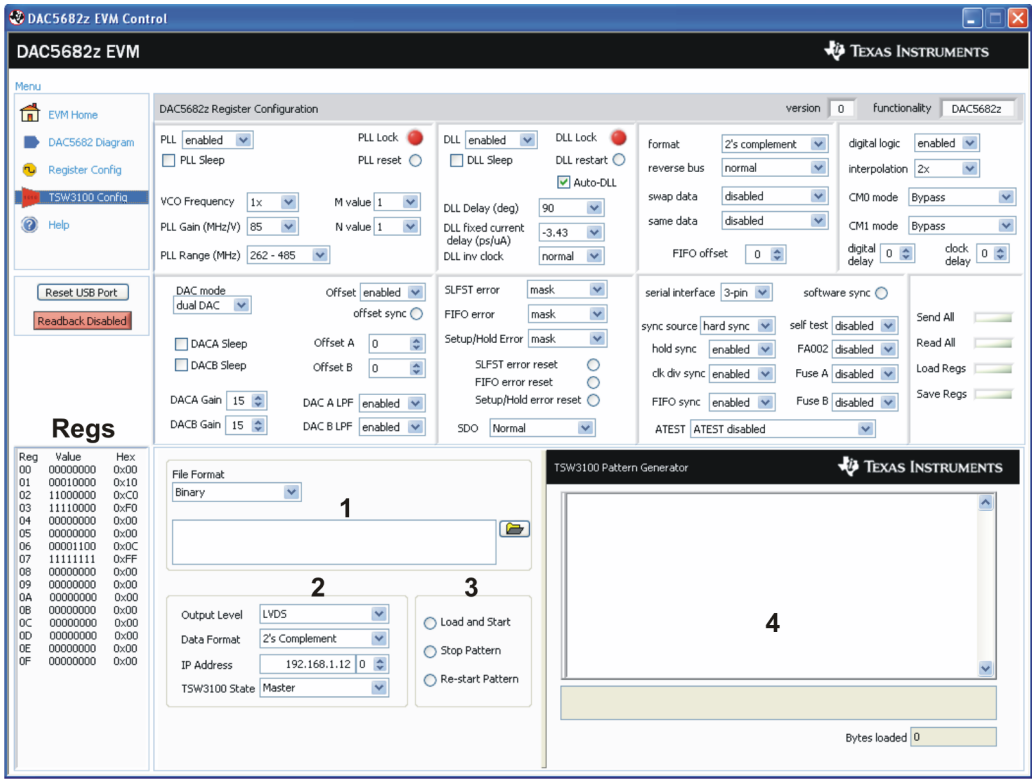

Figure 16. TSW3100 Pattern Generator and DAC5682 Register Configuration Settings

Table 6. TSW3100 Configuration and Pattern Generation Functionality

Subarea Name	Input Output	Description
Pattern Selection (1)		
File Format	Input	Selects *Binary* and 16-bit signed *Integer* format. If Binary is selected, the file must comply with the requirements described on the TSW3100 (SLLU101) documentation. If integer format is selected, the file must consist of a single column for a real signal or two columns for a two-channel or complex signal.
Browse Button	Input	Navigate to the folder containing the input pattern file name. Select the file to use.
Output Mode (2)		
Column Delimiter	Input	Column separator used in the two-channel or complex integer input file. (Not displayed)
Output Level	Input	*LVDS* or *CMOS* outputs. Only *LVDS* is available for the DAC5682z.
Data Format	Input	*2's complement* or *offset binary* format.
IP Address	Input	Specify final digit (1, 2, 3, or 4) of the IP address for the TSW3100 pattern generator.
TSW3100 State	Input	*Master* or *Slave* mode. The default state is *Master* mode. See TSW3100 (SLLU101) documentation for more information.
Command Buttons (3)		
Load and Start	Input	Load a pattern file and start the TSW3100.
Stop Pattern	Input	Stop the pattern transfer.
Re-start Pattern	Input	Re-start the pattern. A pattern must be loaded in memory for this command to work.
Pattern Generation Results (4)		
Command	Output	Shows sequence of commands sent to the TSW3100.

Table 6. TSW3100 Configuration and Pattern Generation Functionality (continued)

Subarea Name	Input Output	Description
Status	Output	Status of the TSW3100 transaction.
Bytes loaded	Output	Number of bytes loaded to the TSW3100.

5.6 Help

When you select the the **Help** menu item, the DAC5682 Diagram screen (Figure 14) and a detached, pop-up Help text window display. As you move the cursor over the DAC5682 Diagram GUI controls, the context-sensitive help text changes in the pop-up window.

6 Introduction

The DAC5682z EVM provides a robust and flexible evaluation system for the DAC5682z. The EVM includes (in addition to the DAC5682z) a CDCM7005 for clock distribution and an optional TRF3703 quadrature modulator path for RF measurements. For a complete hardware description, please consult the schematics and layout sections at the end of this guide. See the DAC5682 (SLLS853), CDCM7005 (SCAS793), and TRF3703 (SLWS184) data sheets for more information.

6.1 Jumper Settings

The DAC5682z uses onboard jumpers to help you modify the DAC5682z board configuration. Table 7 explains the functionality of these jumpers.

Table 7. Jumper Functions

Jumper	Label	Function	Condition	Default
JP8	EXTLO	Internal (GND) or external (3.3V) voltage reference	GND	Pin 2-3
JP10	VFUSE	Factory use only. Connect to 1.8VDD for normal operation.	1.8 VDD	Pin 1-2
JP12	CDC_PD	Low active power down of CDCM7005	3.3 VCLK	Pin 1-2
JP13	VCXOB	Choose internal VCXO or external VCXO INB	External VCXO	Pin 2-3
JP14	VCXO_P	Choose internal VCXO or external VCXO positive input	External VCXO	Pin 2-3
JP15	VCXO_N	Choose CDCM7005 or external VBB	CDCM7005	Pin 1-2
JP16	REF_CLK	Choose internal 10-MHz ref or external ref	Internal Ref	Pin 2-3
JP17	+3.3V_IN	Main or TP3 3.3 voltage source for CDCM7005 and USB	Main	Pin 1-2
JP19	+3.3VCLK	VCXO power down	3.3 VCLK	Pin 1-2

6.2 Input/Output Connectors

Table 8 lists the input and output connectors.

Table 8. Input and Output Connectors

Reference Designator	Label	Connector Type	Description
J1	IOUTB2	SMA	DACB transformer output. Optional IOUTB2 output.
J2	IOUTB1	SMA	Optional IOUTB1 output.
J3	IOUTA2	SMA	DACA transformer output. Optional IOUTA2 output.
J4	IOUTA1	SMA	Optional IOUTA1 output.
J5		SEMTEK	Input LVDS data to DAC682z. Output clock to data source.
J6	EXT_VCXO_P	SMA	External main clock input.
J7	EXT_VCXO_N	SMA	External VCXO negative connection. Not required.

Table 8. Input and Output Connectors (continued)

Reference Designator	Label	Connector Type	Description
J8	Y2A_CLK	SMA	Optional CDCM7005 clock output.
J9	EXT_REF_CLK	SMA	External reference clock input.
J10	Y2B_CLK	SMA	Optional CDCM7005 clock output.
J13	USB_CONN	USB	USB connector for software communication.
J14/J15	+1.8V_IN	Banana Plug	+1.8V connection pair.
J16	RFOUT	SMA	RF output from TRF3703.
J17/J18	+3.3V_IN	Banana Plug	+3.3V connection pair.
J19/J20	+5VA_IN	Banana Plug	+5V connection pair. Required only for RF measurements.
J23	RF_LO_IN	SMA	TRF3703 LO source input.

6.3 USB Interface

The DAC5682z EVM has a 4-pin USB port connector that interfaces to a USB 1.1 (or later) compliant USB port. You can program the CDCM7005 and DAC5682z using this USB port.

6.4 Power Management

The DAC5682z EVM requires 1.8 V and 3.3 V supplies for normal operation. An additional 5 V supply is required supply power to the TRF3073 for RF measurements.

7 Demo Kit Test Configuration

7.1 Test Setup Block Diagram

The test setup for the TSW3082 and DAC5682z EVM is shown in Figure 17. This setup shows the TSW3100 pattern generator supplying an LVDS signal to the TSW3082/DAC5682 EVM.

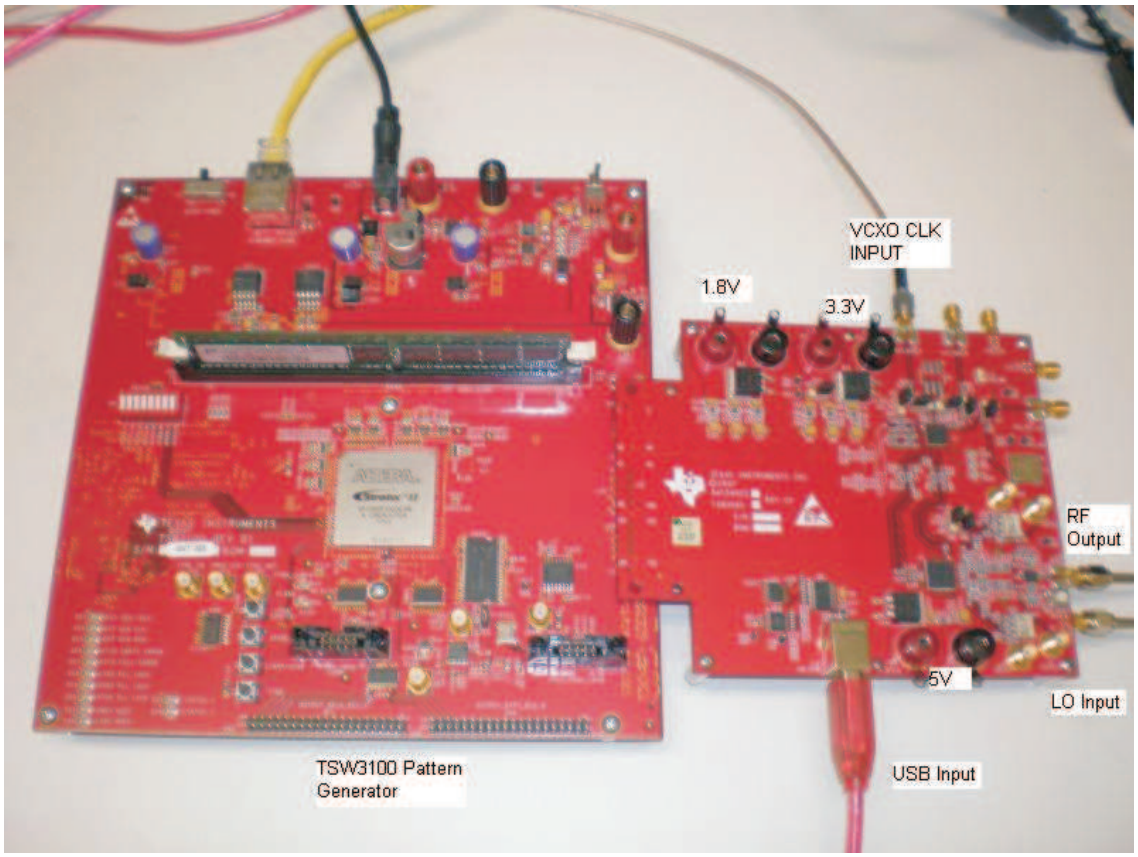

Figure 17. TSW3082 EVM Driven by TSW3100 Pattern Generator

7.2 Test Equipment

This test equipment is required for testing the TSW3082 and DAC5682 EVM. Other equipment may be substituted, however results may vary due to instrument limitations.

- Power supplies—1.8 V (DAC digital), 3.3 V (DAC analog), and 5 V (RF modulator)
- Spectrum Analyzer—Rhode & Schwarz FSU, FSQ, or equivalent. This is necessary to measure the noise floor ACPR greater than 70 dBm with the noise correction option.
- Pattern generator—TSW3100 using LVDS mode, or some other LVDS capable generator.
- Oscilloscope—probe clock and data lines for troubleshooting.
- Digital volt meter—verify signal levels.

7.3 Calibration

To measure the proper output power, the insertion loss of the analyzer cable must be calibrated. Measure a calibrated 0 dBm source to see how much loss is in the cable at the frequency of interest.

7.4 Typical Performance Measurements

The DAC5682 EVM measurements at the transformer outputs J1 and J3 (modulator is not used) will have better performance than the RF output. The RF output is typically limited by the performance of the RF parts. In this case the DAC output at 0 IF or low IF is several dB better than the noise floor of the modulator output at J16.

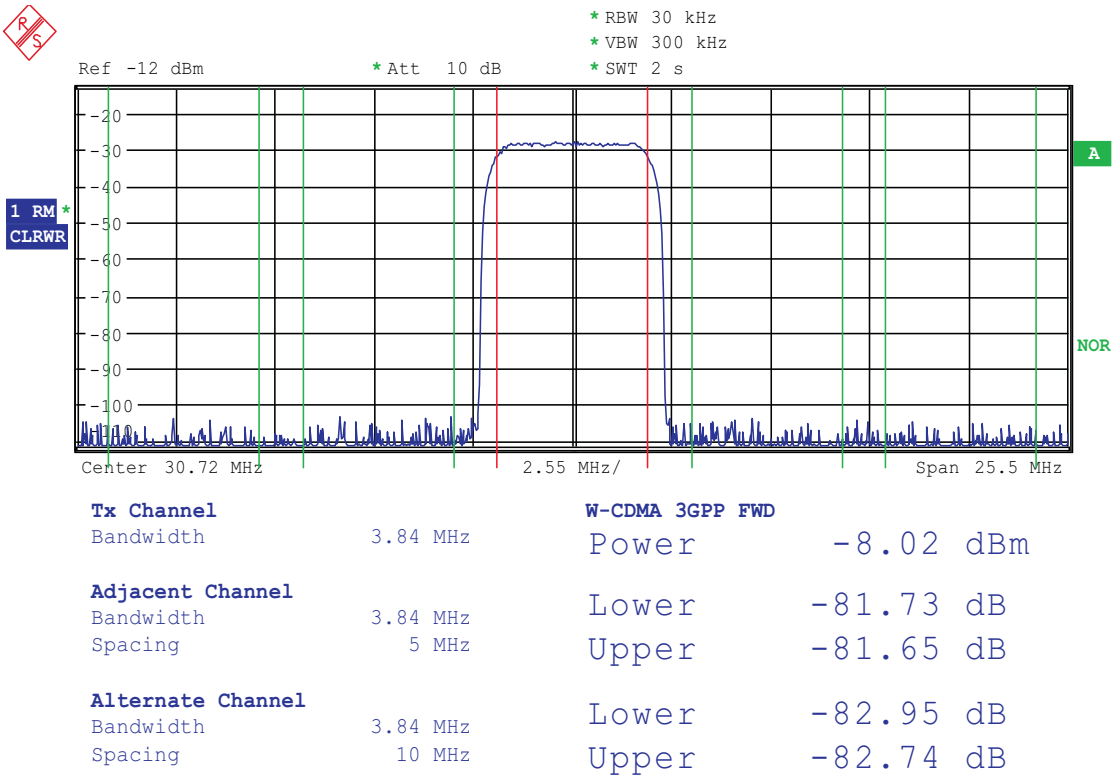

Figure 18. DAC5682 EVM Transformer Output With a Low IF at 30.72 MHz

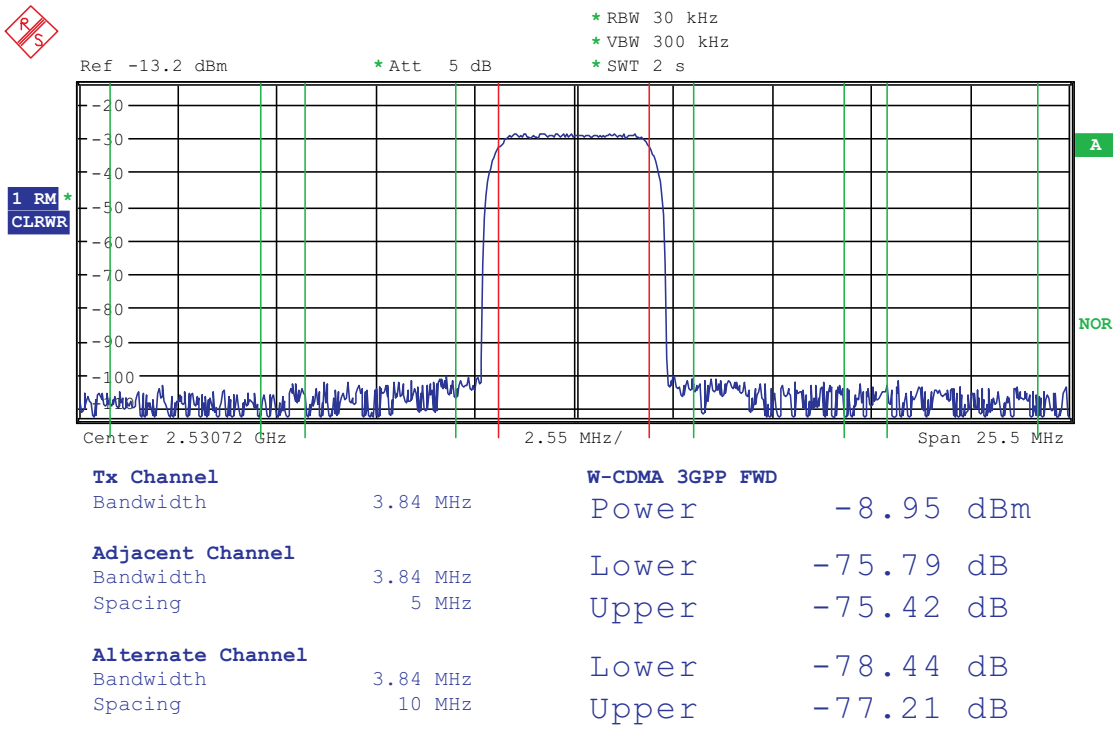

Figure 19. TSW3082 EVM output at RF LO + low IF of 30.72M (6 dB lower than DAC output)

8 Initial Power Up and Test

This section outlines the basic power application and test procedure to ensure the EVM is in an operational state.

8.1 Initial Inspection

Inspect the board to determine which VCXO resides on the board. This is useful when programming the CDCM7005 to lock the DAC clock to the reference.

8.2 Engage Power Supplies

Engage the power supplies for 1.8 V, 3.3 V, and 5 V. Ensure that each supply is not drawing more than 1 A of current. Typically the 1.8 V will be less than 1 A, 3.3 V less than 200 mA, and 5 V less than 0.5 A.

8.3 Verify the Status of the Board

The DAC software detects if the USB port is active and if it is capable of reading the serial number from the EVM. This determines if the communication between the board and PC is correct. The **EVM Home** menu (Figure 13 and Table 3) of the DAC8652z GUI software provides this status information.

8.4 Program the CDCM7005

Navigate to the **Register Config** menu (Figure 15 and Table 5). Program the CDCM7005 registers as necessary. Typically a *reg.cdcm7005* register file is provided to initialize the default settings. Load this register file using the section 4 (**SEND/SAVE Button Settings**) controls described in Table 5 .

8.5 Program the DAC5682z

Navigate to the **DAC5682 Diagram** menu (Figure 14 and Table 4). Adjust the register settings as desired. Typically a *reg.dac5682* register file provides a set of test register values. Load this register file using the section 8 (**SEND/SAVE Button Settings**) controls described in Table 4 .

8.6 Carrier Suppression

Carrier feed through is dependent on the DC offset between I and Q paths. There are registers in the DAC that provided some digital DC correction. A feedback path is necessary to perform this correction. Contact the TI factory applications team for more details.

9 Optional Configurations

9.1 External VCXO

It is possible to configure the TSW3082 and DAC5682 EVM to use an external VCXO for application flexibility. J13 and J14 may be used in position 2-3 to select an external VCXO or clock signal.

9.2 RF or DAC Output

The board is populated with the TRF3703 modulator. If the board is configured for DAC output, the modulator is not used and 5 V power is unnecessary. The DAC outputs in this setup are J1 and J3.

If the board is configured for RF output, the 5 V must be used to power the modulator. The resistor path at the output of the DAC must be changed to pass the signal to the modulator instead of to the transformers. In this case an external LO must be provided on J23 and the RF output is present at J16.

10 Baseband Filter

The TSW3082 EVM is configured with enough pads to provide a customer a specific 5th-order differential passive LC filter. By default, it is only populated with a simple LC low pass filter to attenuate the higher clock harmonics. The 3 dB corner of this filter is approximately 300 MHz.

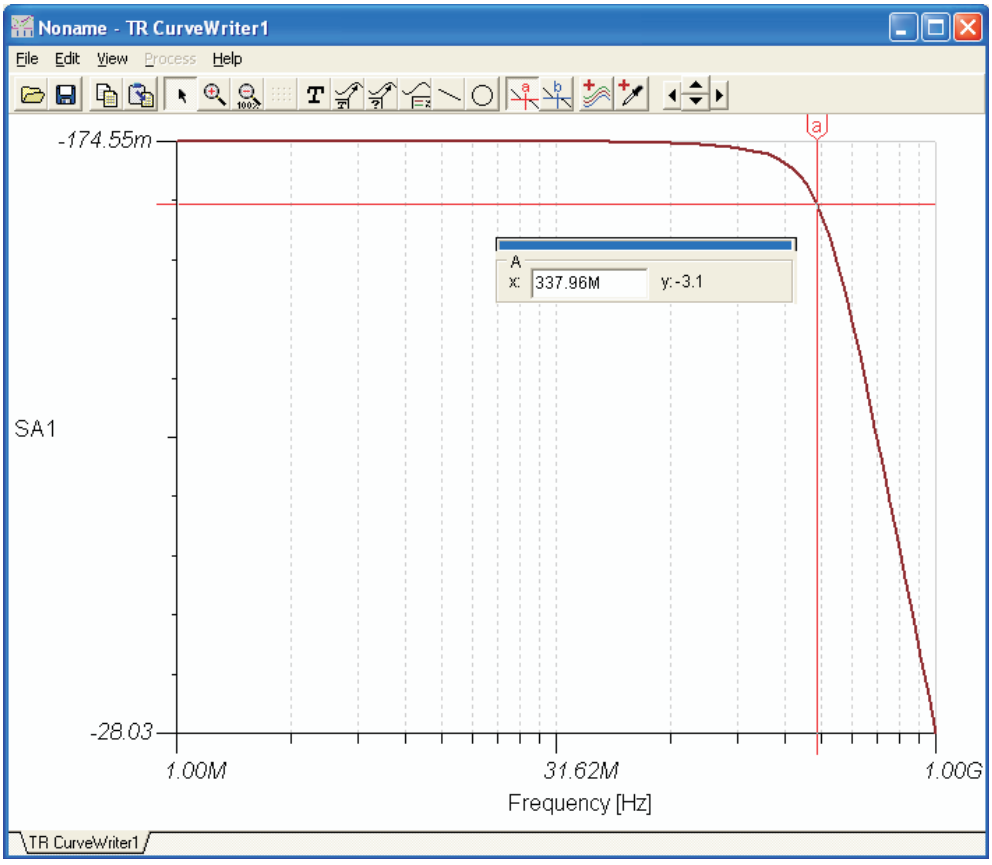

Figure 20. Response of Default Baseband Filter

10.1 RF Output Matching Filter

The TSW3082 RF output provides a pi pad network on the modulator output to provide some matching or filtering if desired. In its default state the pad is not used and a series cap is used on the RF output.

11 Bill of Materials and Schematics

This section contains the bill of materials and schematics for the DAC5682 and TSW3083 EVM.

11.1 Bill of Materials

Qty	Part Reference	Value	PCB Footprint	Mfr_Name	Mfr_Part_Number	Note
12	C1 C2 C5 C8 C56 C70 C76 C79 C84 C87 C121 C124	0.01 µF	0603	Panasonic	ECJ-1VB1C103K	
1	C3	0.15 µF	0402	Murata	GRM36X5R154K10H520	
6	C4 C29 C48 C104 C106 C127	1000 pF	0402	Panasonic	ECJ-0EB1E102K	
38	C6 C7 C9–C15 C17 C18 C20 C23–C25 C27 C33 C38–C47 C50–C52 C57 C61 C94 C95 C107 C114 C130 C131	0.1 µF	0402	Panasonic	ECJ-0EB1C104K	
16	C16 C21 C32 C36 C53 C54 C71 C74 C80 C82 C88 C93 C97 C98 C120 C126	10 µF	tant_a	Kermet	T494A106M016AS	
1	C22	560 pF	0402	Panasonic	ECJ-0EB1H561K	
2	C31 C113	100 pF	0402	Panasonic	ECJ-0EB1E101K	
8	C34 C69 C75 C78 C83 C86 C122 C125	1 µF	0603	Panasonic	ECJ-1V41E105M	
1	C35	0.47 µF	0603	Murata	GRM188R71C474KA88D	
3	C49 C128 C129	0.01 µF	0402	Panasonic	ECJ-0EB1E103K	
3	C58 C108 C115	4.7 µF	tant_a	AVX	TAJA475K020R	
2	C59 C60	47 pF	0603	Panasonic	ECJ-1VC1H470J	
7	C72 C77 C81 C85 C89 C119 C123	47 µF	tant_b	Kemet	T494B476M010AS	
0	C73 C100 C101 C116	4.7 pF	0603	Panasonic	ECJ-1VC1H047C_DNI	DNI
2	C99 C109	3.3 pF	0402	Murata	GRM1555C1H3R3CZ01D	
2	C102 C103	22 pF	0402	Panasonic	ECJ-0EC1H220J	
0	C105 C112	2.2 pF	0603	AVX	06035A2R2CAT2A_DNI	DNI
2	C110 C111	2.7 pF	0603	AVX	06035A2R7CAT2A	
0	C117 C118	0.01 uF	0402	Panasonic	ECJ-0EB1E103K_DNI	DNI
3	D1-D3	LED green	LED_0805	Panasonic	LNJ306G5UUX	
3	D12–D14	MBRB2515L	DIODE_MBRB2515L	ON Semiconductor	MBRB2515LT4G	
13	FB1–FB13	68 Ω at 100 MHz	1206	Panasonic	EXC-ML32A680U	
4	J1–J4	SMA_PCB_THVT	SMA_THVT_312x312	Johnson Components	142-0701-201	
7	J6–J10 J16 J23	SMA_END_JACK_RND	SMA_SMEL_218x247_096	Johnson Components	142-0761-801	
1	J13	USB_B_S_F_B_TH	CON_THRT_USB_B_F	SAMTEC	USB-B-S-F-B-TH	
3	J14 J17 J20	BANANA_JACK_RED	CON_THVT_BANANA_JACK_250 DIA	SPC Technology	845-R	
3	J15 J18 J19	BANANA_JACK_BLK	CON_THVT_BANANA_JACK_250 DIA	SPC Technology	845-B	
1	J5	ASP-122952-01	CON_SMVT_160POS_ASP_122952	SAMTEC	ASP-122952-01	
4	JP8 JP13 JP14 JP16	Jumper_1x3_100_430L	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-.230	(SHUNT 2-3)
4	JP10 JP12 JP15 JP17	Jumper_1x3_100_430L	HDR_THVT_1x3_100_M	SAMTEC	HMTSW-103-07-G-S-.230	(SHUNT 1-2)
1	JP19	Jumper_1x2_100_430L	HDR_THVT_1x2_100_M	SAMTEC	HMTSW-102-07-G-S-.230	
0	L6 L7	56 nH	IND_0603	Panasonic	ELJ-RE56NJF3_DNI	DNI
4	L8 L9 L14 L15	10 nH	IND_0603	Coilcraft	0603CS-10NXLU	
4	L10–L13	68 nH	0603	Coilcraft	0603CS-68NXJL	
0	R1 R2 R4 R5 R12 R14 R17 R19	1 KΩ	0402	Panasonic	ERJ-2RKF1001X_DNI	DNI

Qty	Part Reference	Value	PCB Footprint	Mfr_Name	Mfr_Part_Number	Note
10	R3 R7 R13 R21 R26 R80 R82 R90 R93 R96	100 Ω	0402	Panasonic	ERJ-2RKF1000X	
0	R6 R9 R15 R20 R23 R27 R109 R134–R136	0	0603	Panasonic	ERJ-3GEY0R00V_DNI	DNI
5	R8 R22 R44 R49 R62	0	0402	Panasonic	ERJ-2GE0R00X	
1	R10	93.1 Ω	0402	Panasonic	ERJ-2RKF93R1X	
0	R11 R24 R132 R133	60.4 Ω	0603	Yageo	RC0603FR-0760R4L_DNI	DNI
0	R16	100 Ω	0603	Panasonic	ERJ-3EKF1000V_DNI	DNI
1	R18	953 Ω	0402	Panasonic	ERJ-2RKF9530X	
1	R25	1 KΩ	0402	Panasonic	ERJ-2RKF1001X	
3	R28–R30	750 Ω	0402	Panasonic	ERJ-2RKF7500X	
8	R31–R34 R42 R43 R66 R67	130 Ω	0402	Panasonic	ERJ-2RKF1300X	
8	R36–R39 R46 R47 R69 R70	82.5 Ω	0402	Panasonic	ERJ-2RKF82R5X	
2	R40 R116	150 Ω	0402	Panasonic	ERJ-2RKF1500X	
2	R41 R150	90.9 Ω	0603	Panasonic	ERJ-3EKF90R9V	
0	R45 R51 R122 R123	0	0402	Panasonic	ERJ-2GE0R00X_DNI	DNI
0	R48 R54	130 Ω	0402	Panasonic	ERJ-2RKF1300X_DNI	DNI
9	R50 R56 R78 R79 R81 R84 R89 R95 R97	22.1 Ω	0402	Panasonic	ERJ-2RKF22R1X	
0	R52 R57 R110 R111	150 Ω	0402	Panasonic	ERJ-2RKF1500X_DNI	DNI
0	R53 R58	82.5 Ω	0402	Panasonic	ERJ-2RKF82R5X_DNI	DNI
0	R55	49.9 Ω	0402	Panasonic	ERJ-2RKF49R9X_DNI	DNI
7	R59–R61 R64 R108 R113 R114	10 KΩ	0402	Panasonic	ERJ-2RKF1002X	
1	R63	162 Ω	0402	Panasonic	ERJ-2RKF1620X	
1	R65	4.75 KΩ	0402	Panasonic	ERJ-2RKF4751X	
1	R92	100 Ω	0603	Panasonic	ERJ-3EKF1000V	
14	R137 R140–R142 R145 R153 R155 R156 R159–R164	0	0603	Panasonic	ERJ-3GEY0R00V	
4	R138 R151 R152 R154	60.4 Ω	0603	Yageo	RC0603FR-0760R4L	
1	R139	49.9 Ω	0402	Panasonic	ERJ-2RKF49R9X	
4	R143 R144 R147 R148	634 Ω	0603	Yageo	RC0603FR-07634RL	
4	R146 R149 R157 R158	115 Ω	0603	Yageo	RC0603FR-07115RL	
1	SW1	SW RESET	SW_SMVT_RESET	C&K	KT11P3JM	
2	T1 T2	ADT4-1T	TFMR_6_250x340_100	Mini-Circuits	ADT4-1T	
8	TP1-TP8	Testloop_Black	TP_THVT_060_RND	Components Corporation	TP-105-01-00	
1	U1	DAC5682Z	QFN_64_360x360_0p50mm_pwrpad	Texas Instruments	DAC5682Z	
1	U2	CDCM7005	QFN_48_281x281_0p50mm_pwrpad	Texas Instruments	CDCM7005RGZT	
1	U3	OSC-VECTRON	OSC_4_SM_460x386	Vectron	VTD3-J0BC-10M000	
1	U5	FT245RL	SSOP_28_413x220_26	FTDI Chip	FT245RL	
0	U6	2115–491.52 MHZ	VCXO_6	Toyocom	TCO-2111-491.52_DNI	DNI
1	U8	TRF3703-33	QFN_24_163x163_0p50mm_pwrpad	Texas Instruments	TRF3703-33IRGET	
1	U10	SN74AHC541PW	TSSOP_20_260x177_26	Texas Instruments	SN74AHC541PW	
1	U11	SN74HC241PW	TSSOP_20_260x177_26	Texas Instruments	SN74HC241PW	
4	Z_SCREW1–Z_SCREW4	SCREW PANHEAD 4-40 x 3/8		Building Fasteners	PMS 440 0038 PH	SCREW FOR STANDOFF
8	Z_SH-H1–Z_SH-H6 Z_SH-H9–Z_SH-H10	SHUNT-HEADER		Keltron	MJ-5.97-G	SHUNT FOR HEADER
4	Z_STANDOFF1–Z_STANDOFF4	STANDOFF ALUM HEX 4-40 x .500		Keystone	2203	STANDOFF

11.2 Schematics

The TSW3082 and DAC5682 schematics are attached. These two EVMs share the same schematic with a different bill of materials.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.8 V to 5.0 V and the output voltage range of 0.0 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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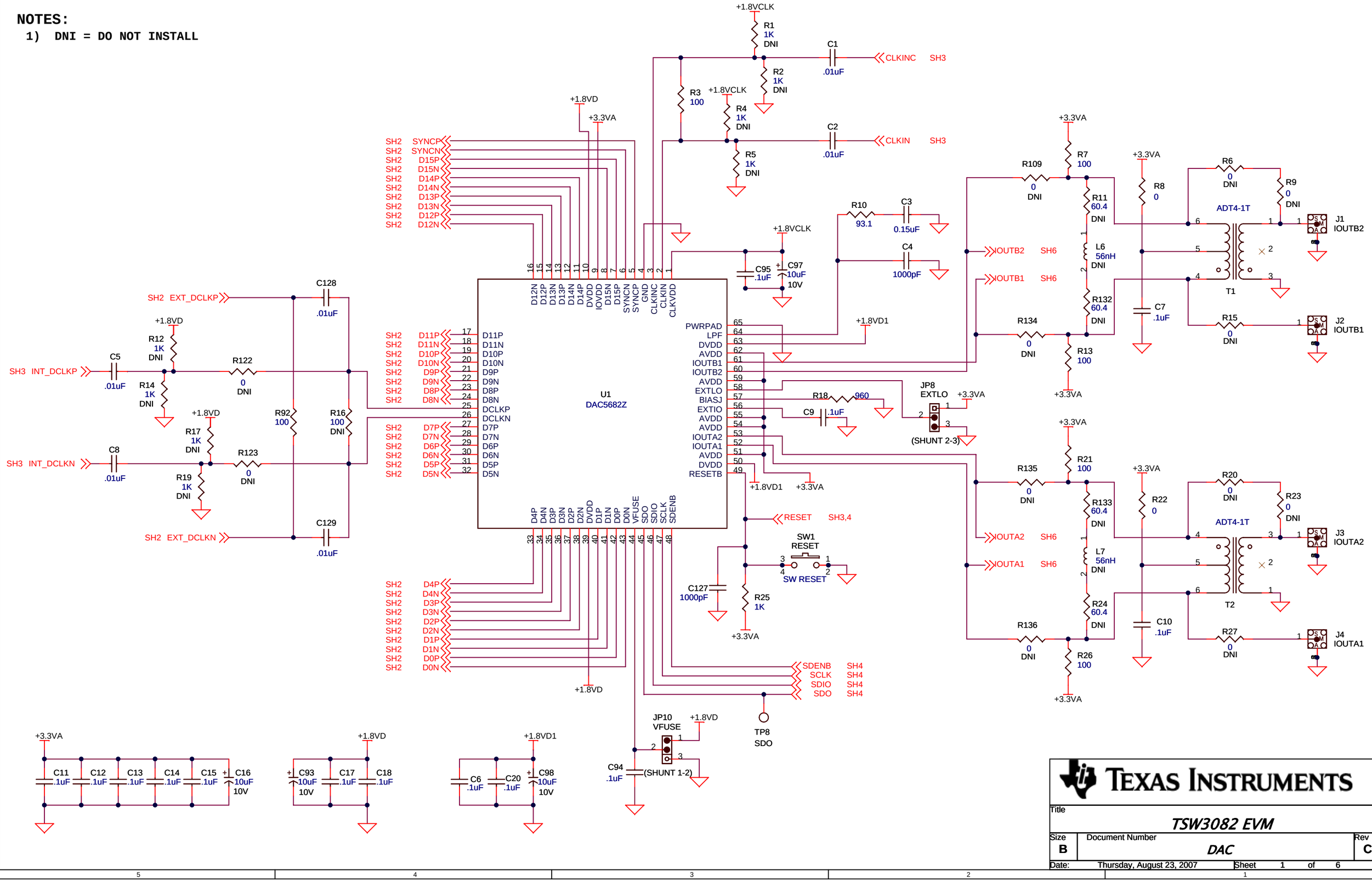
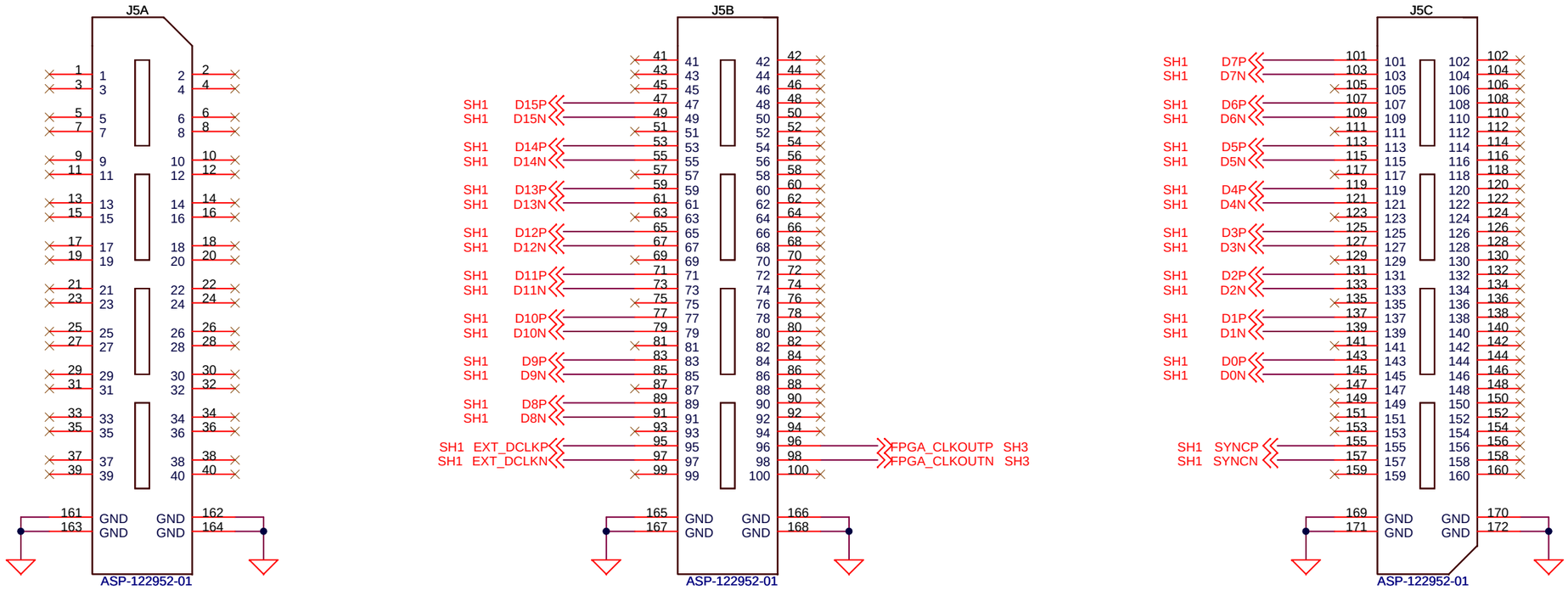
NOTES:

1) DNI = DO NOT INSTALL

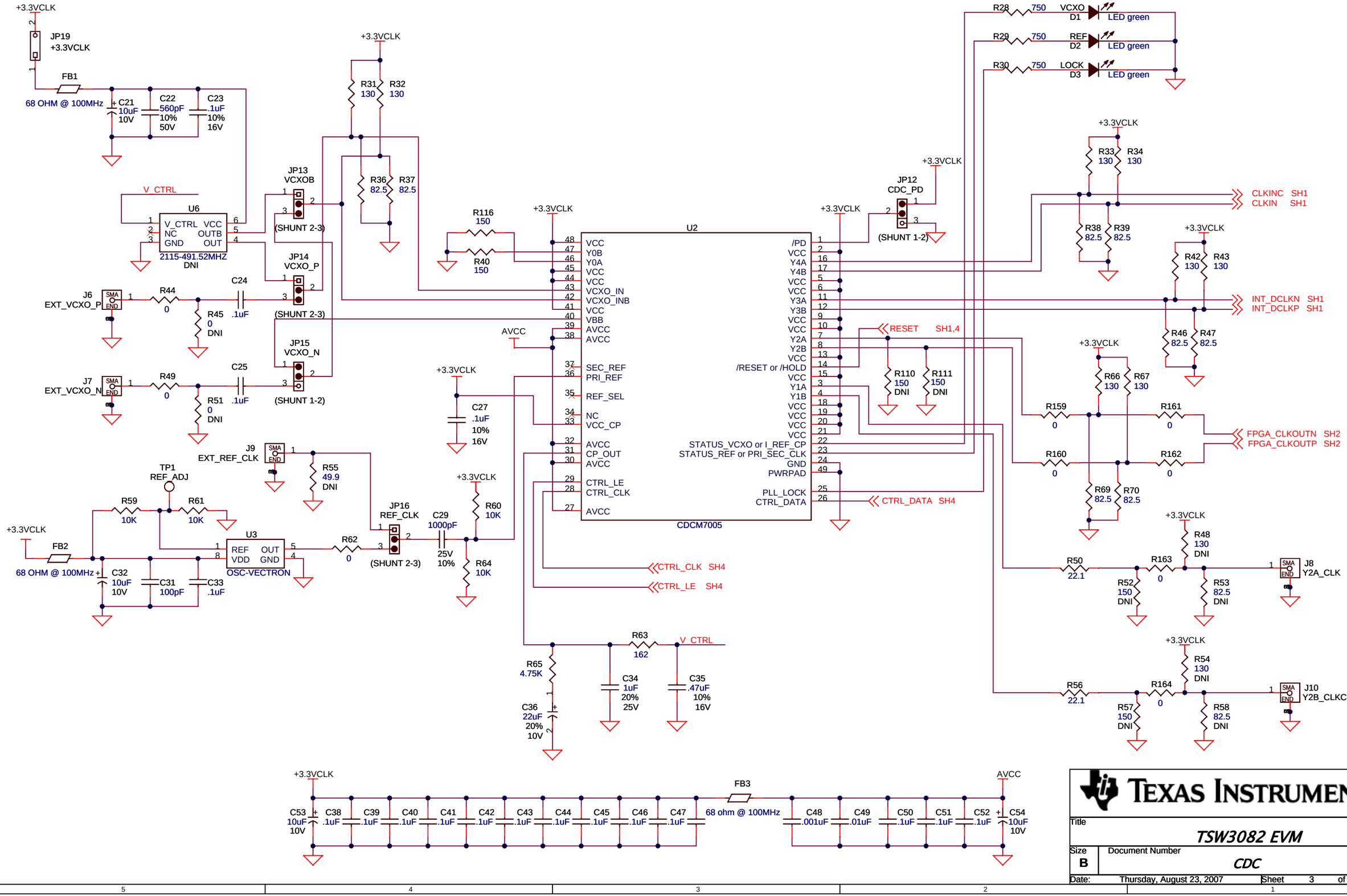


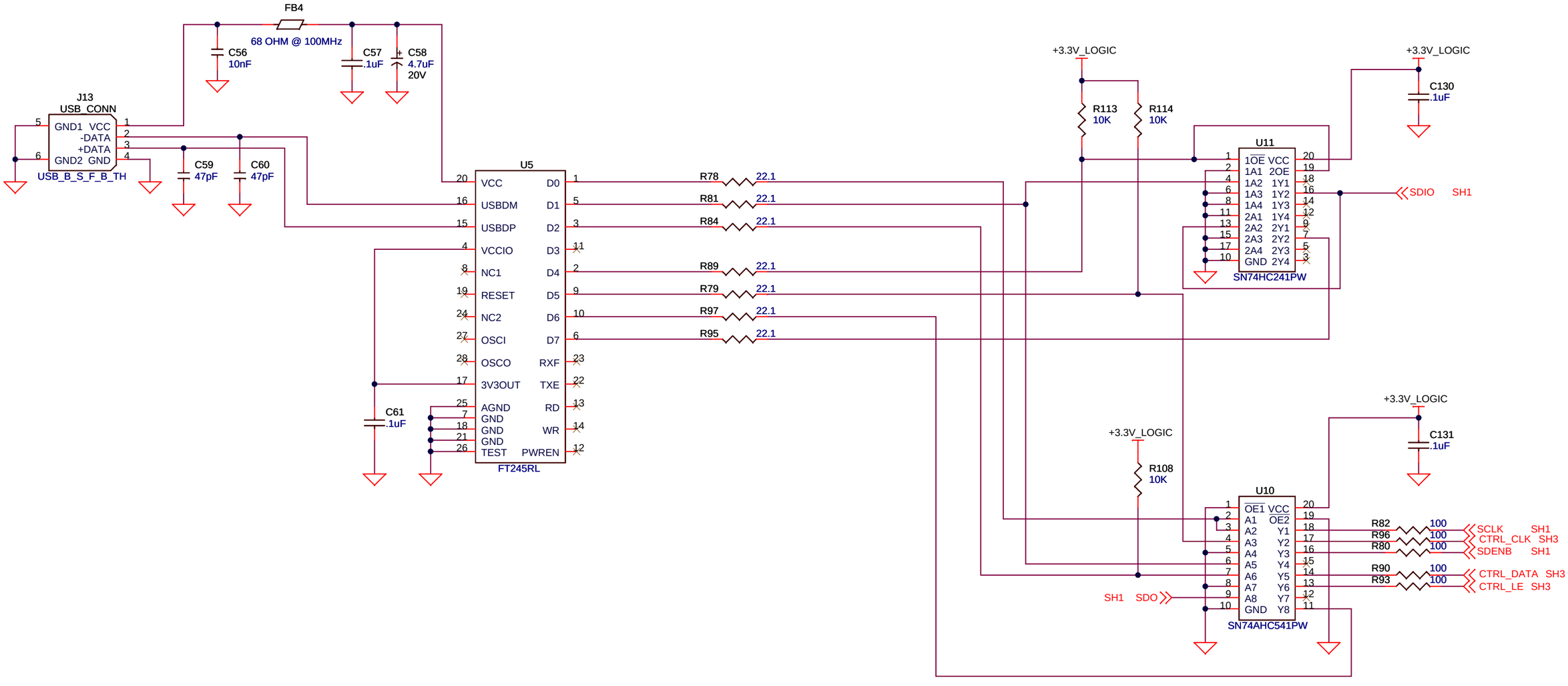
TEXAS INSTRUMENTS

Title	TSW3082 EVM	
Size: B	Document Number: DAC	Rev: C2
Date: Thursday, August 23, 2007	Sheet 1 of 6	



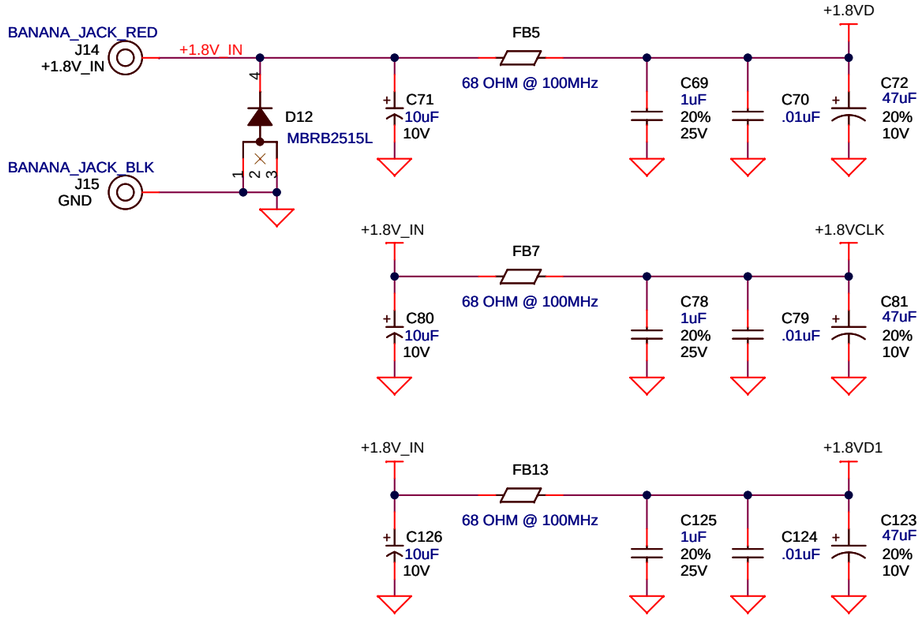
Title	TSW3082 EVM	
Size: B	Document Number: INTERFACE CONTROL	Rev: C2
Date: Thursday, August 23, 2007	Sheet 2 of 6	

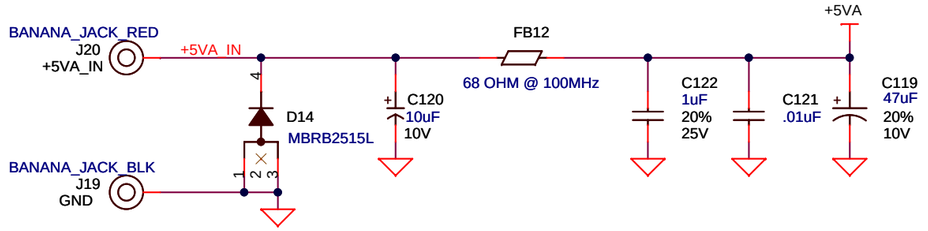

+3.3VCLK
JP19
+3.3VCLK
FB1
68 OHM @ 100MHz
C21
10uF
10V
C22
560pF
10%
50V
C23
.1uF
10%
16V
R31
130
R32
130
JP13
VCXOB
(SHUNT 2-3)
R36
82.5
R37
82.5
V_CTRL
U6
V_CTRL VCC
NC OUTB
GND OUT
2115-491.52MHZ
DNI
R116
150
R40
150
U2
J6
EXT_VCXO_P
SMA
END
R44
0
R45
0
DNI
C24
.1uF
JP14
VCXO_P
(SHUNT 2-3)
J7
EXT_VCXO_N
R49
0
R51
0
DNI
C25
.1uF
JP15
VCXO_N
(SHUNT 1-2)
AVCC
C27
.1uF
10%
16V
J9
EXT_REF_CLK
R55
49.9
DNI
TP1
REF_ADJ
R59
10K
R61
10K
JP16
REF_CLK
C29
1000pF
25V
10%
R60
10K
R64
10K
FB2
68 OHM @ 100MHz
C32
10uF
10V
C31
100pF
C33
.1uF
U3
REF OUT
VDD GND
OSC-VECTRON
R62
0
(SHUNT 2-3)
VCC
Y0B
Y0A
VCC
VCC
VCXO_IN
VCXO_INB
VCC
VBB
AVCC
AVCC
SEC_REF
PRI_REF
REF_SEL
NC
VCC_CP
AVCC
CP_OUT
AVCC
CTRL_LE
CTRL_CLK
AVCC
CDCM7005
/PD
VCC
Y4A
Y4B
VCC
VCC
Y3A
Y3B
VCC
VCC
Y2A
Y2B
VCC
/RESET or /HOLD
VCC
Y1A
Y1B
VCC
VCC
VCC
VCC
STATUS_VCXO or I_REF_CP
STATUS_REF or PRI_SEC_CLK
GND
PWRPAD
PLL_LOCK
CTRL_DATA
JP12
CDC_PD
(SHUNT 1-2)
RESET SH1,4
R110
150
DNI
R111
150
DNI
CTRL_DATA SH4
CTRL_CLK SH4
CTRL_LE SH4
R63
162
V_CTRL
R65
4.75K
C34
1uF
20%
25V
C35
.47uF
10%
16V
C36
22uF
20%
10V
R28
750
VCXO
D1
LED green
R29
750
REF
D2
LED green
R30
750
LOCK
D3
LED green
R33
130
R34
130
CLKINC SH1
CLKIN SH1
R38
82.5
R39
82.5
R42
130
R43
130
INT_DCLKN SH1
INT_DCLKP SH1
R46
82.5
R47
82.5
R66
130
R67
130
R159
0
R161
0
FPGA_CLKOUTN SH2
FPGA_CLKOUTP SH2
R160
0
R162
0
R69
82.5
R70
82.5
R48
130
DNI
R50
22.1
R163
0
J8
Y2A_CLK
R52
150
DNI
R53
82.5
DNI
R54
130
DNI
R56
22.1
R164
0
J10
Y2B_CLKC
R57
150
DNI
R58
82.5
DNI
FB3
68 ohm @ 100MHz
C53
10uF
10V
C38
.1uF
C39
.1uF
C40
.1uF
C41
.1uF
C42
.1uF
C43
.1uF
C44
.1uF
C45
.1uF
C46
.1uF
C47
.1uF
C48
.001uF
C49
.01uF
C50
.1uF
C51
.1uF
C52
.1uF
C54
10uF
10V
AVCC
TEXAS INSTRUMENTS
Title
TSW3082 EVM
Size
B
Document Number
CDC
Rev
C2
Date:
Thursday, August 23, 2007
Sheet
3
of
6

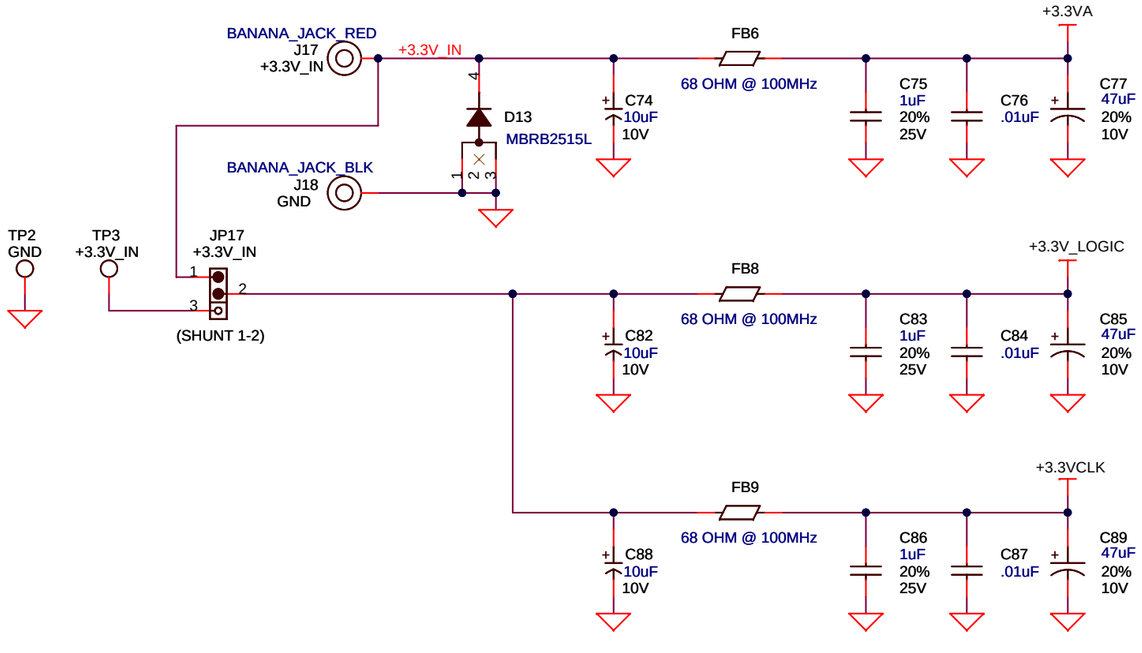


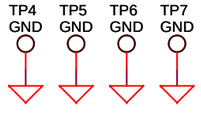
TEXAS INSTRUMENTS

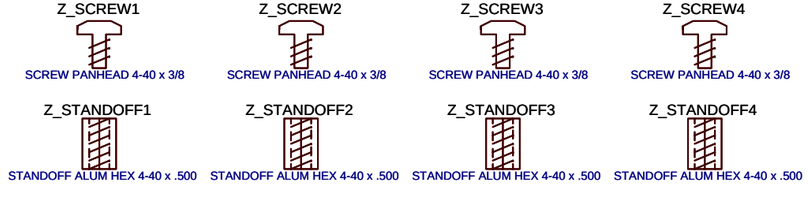
Title	TSW3082 EVM	
Size: B	Document Number: USB INTERFACE	Rev: C2
Date: Thursday, August 23, 2007	Sheet 4 of 6	











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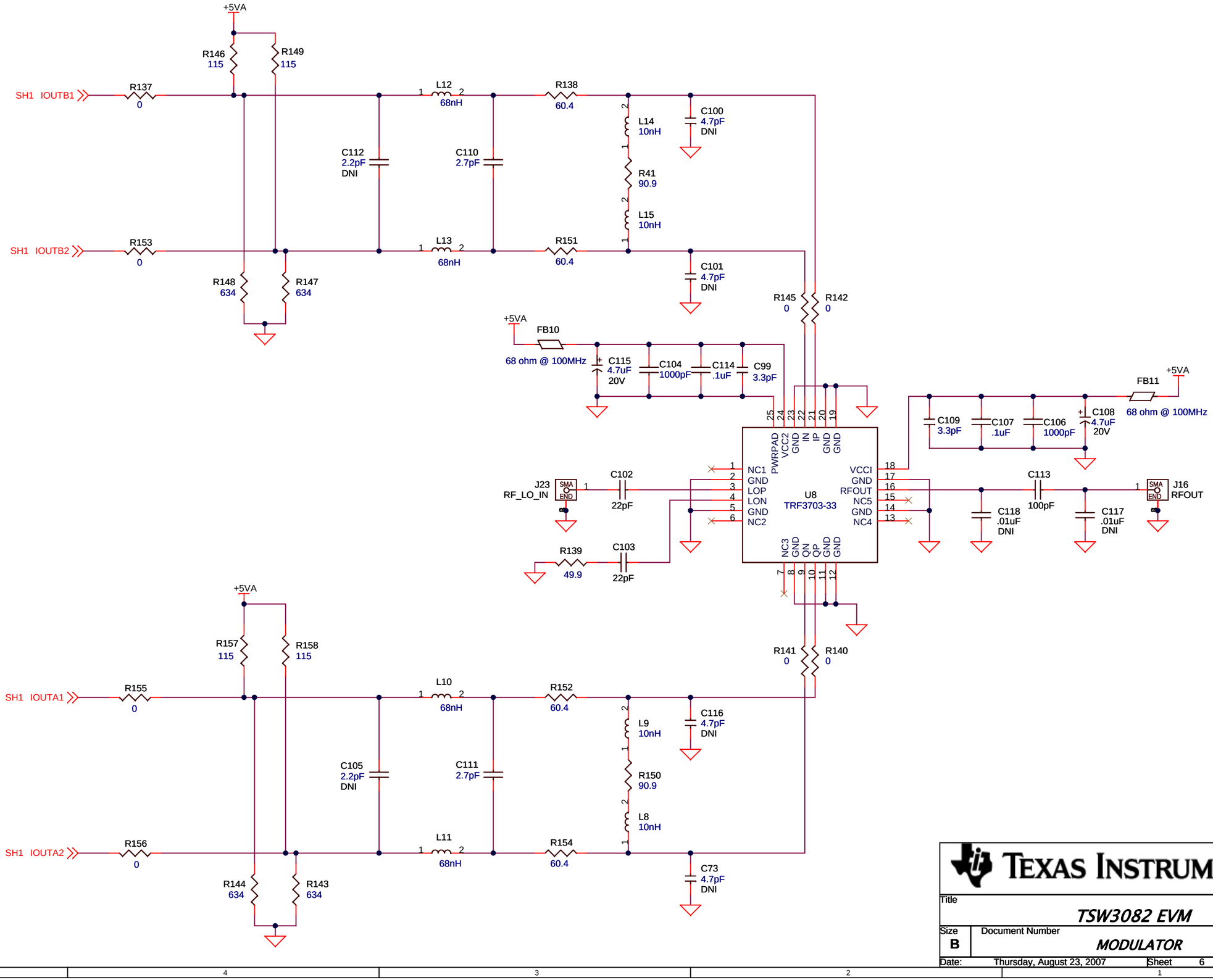
Title	*TSW3082 EVM*	
Size: B	Document Number: *POWER DISTRIBUTION*	Rev: C2
Date: Thursday, August 23, 2007	Sheet 5 of 6	



Title	TSW3082 EVM	
Size: B	Document Number: MODULATOR	Rev: C2
Date: Thursday, August 23, 2007	Sheet 6 of 6	

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