

Isolated, Full-Duplex, 20-Mbps, 3.3-V to 5-V RS-485 Interface

1 Circuit Function and Benefits

This circuit provides an isolated, 20-Mbps, 3.3-V to 5-V RS-485 interface using the ISO3086T isolated RS-485 transceiver and the TPS76350 high-accuracy linear regulator. This circuit achieves signal and power isolation and at the same time decreases board space and power consumption.

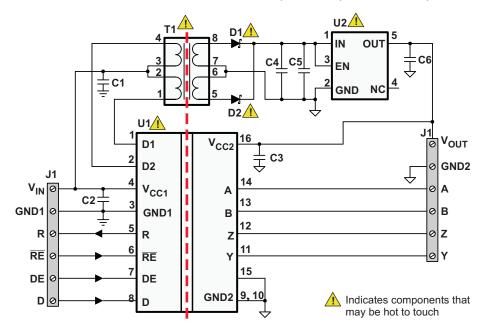


Figure 1. Isolated, Full-Duplex, 20-Mbps, 3.3-V to 5-V RS-485 Interface

2 Circuit Description

The ISO3086T is an isolated differential line transceiver with integrated transformer driver that provides the primary voltage for an isolation transformer. The device is ideal for long transmission lines because the ground loop is broken to allow the device to operate with a much larger common-mode voltage range. The symmetrical isolation barrier of each device is tested to provide 2500 Vrms of isolation between the line transceiver and the logic-level interface.

The galvanically isolated differential bus transceiver is designed for full-duplex data communication on multipoint bus-transmission lines. The transceiver combines a galvanically isolated differential line driver and differential-input line receiver.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or nearby sensitive circuitry if they are of sufficient magnitude and duration. The ISO3086T can significantly reduce the risk of data corruption and damage to expensive control circuits.



Common Variations www.ti.com

The integrated transformer driver consists of an oscillator followed by a flip-flop stage generating two complementary 50% duty-cycle square waves. These two signals drive the ground-referenced N-channel power switches. Internal circuitry ensures break-before-make action between the two switches.

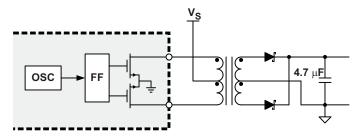


Figure 2. Simplified Transformer Driver

A pair of Schottky diodes and a bulk capacitor build a full-wave rectifier, providing the input voltage for the TPS76350 linear voltage regulator.

This low-dropout (LDO) voltage regulator offers the benefits of low dropout voltage, low-power operation, and miniaturized packaging. The regulator features low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in a 5-terminal, small-outline, integrated-circuit SOT-23 package, the TPS76350 is ideal for cost-sensitive designs and for applications where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low (typically 300 mV at 150 mA of load current) and is directly proportional to the load current. Because the PMOS pass element is a voltage-driven device, the quiescent current is very low (140 µA maximum) and is stable over the entire range of output load current (0 mA to 150 mA).

The TPS76350 also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μ A maximum at $T_J = 25$ °C. The TPS76350 output provides a regulated 5-V power supply to the ISO3086T bus-side circuitry (V_{CC2}) as shown in Figure 1.

Although not required, a 0.047 μ F or larger ceramic bypass input capacitor, connected between IN and GND and located close to the TPS763xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low-dropout regulators, the TPS76350 requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7 μ F and the equivalent series resistance (ESR) must be between 0.3 Ω and 10 Ω . Capacitor values of 4.7 μ F or larger are acceptable, provided the ESR is less than 10 Ω . Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously. Most of the commercially available 4.7- μ F surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated previously.

3 Common Variations

When the ISO3086T is powered by 3.3 V on the logic side, a 1CT : 2.2CT transformer (T1) is required to step up the 3.3-V input supply (V_s) to 6 V at the transformer secondary, thereby ensuring enough headroom for the TPS76350 LDO to provide a regulated 5-V output. If the ISO3086T is powered by 5 V on the logic side, a 1CT : 1.5CT transformer is needed.

The external transformer used with the ISO3086T must have a center-tapped primary winding. The turns ratio of the transformer must provide the minimum required output voltage at the maximum anticipated load current with the minimum input voltage. Table 1 lists suitable transformers for the circuit in Figure 1.



www.ti.com Circuit Performance

Table 1	Recommended	Isolation	Transformers

Manufacturer	Primary Voltage (3.3 V)	Primary Voltage (5 V)
Coilcraft	DA2304-AL	DA2303-AL
Murata	782482/35C	782485/55C

4 Circuit Performance

Figure 3 shows a low-frequency sweep for measuring the radiated emissions to demonstrate compliance with the EN55022 standard, which specifies the limits and methods of measurement of radio disturbance characteristics of information technology equipment.

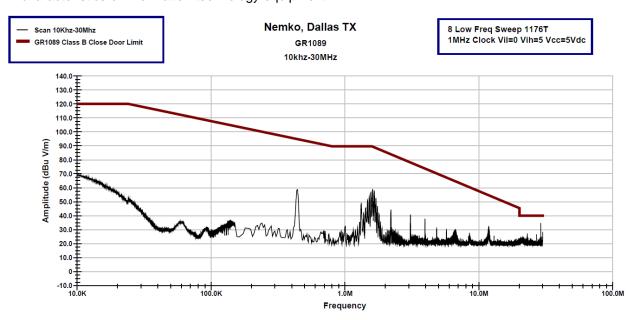


Figure 3. Radiated Emissions (dBµV/m) from 10 kHz to 30 MHz

Figure 4 shows the circuit efficiency over the load current. While load currents in the lower 20 mA can be expected for low data rates and no common-mode voltage, higher load currents around 100 mA are required for high data rates and high common-mode voltages.

Circuit Layout and BOM www.ti.com

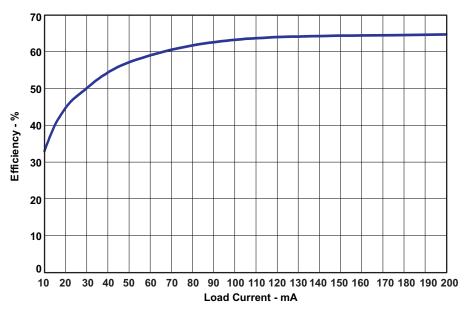


Figure 4. Efficiency Over Load Current

5 Circuit Layout and BOM

Figure 5 shows the silk screen as well as the top and bottom layers of the two-layer board, with the actual dc-dc converter capturing an area of 20 mm \times 14 mm only.

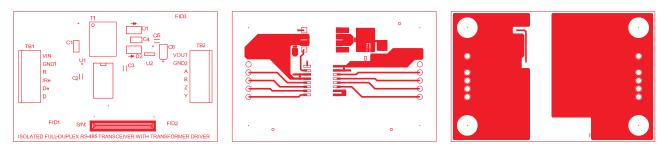


Figure 5. Board Layout: Silk Screen (Left), Top Layer (Middle), Bottom Layer (Right)

Figure 6 shows a picture of the actual board.

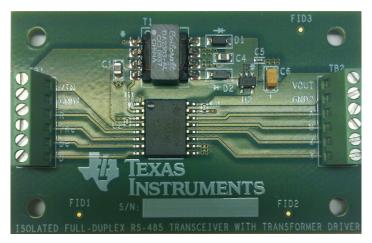


Figure 6. Reference Design Board: Top View



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Table 2 shows the final bill of materials.

Table 2. Bill of Materials

Designator	Part No.	MFR	Value	Package/Size
C1, C4	GRM21BR61C106KE15L	Murata	10-μF/16-V/X5R (ceramic)	0805 (2 × 1,25 mm ²)
C2, C3, C5	C0402C104K4RACTU	KEMET	0.1-µF/16-V/X7R (ceramic)	$0402 (1 \times 0.5 \text{ mm}^2)$
C6	T491A475K016AT	KEMET	4.7-µF/16-V (tantalum)	3,2 × 1,6 mm ²
D1, D2	MBR0520L	Fairchild	0.4-W Schottky diode	SOD123
J1, J2	MPT 0,5 / 6-2,54	Phoenix-Contact	6-position terminal block	6,2 × 15, mm ²
T1	DA2304-AL	Coilcraft	1:2.2	10 x 12 mm ²
U1	ISO3086T	TI	Half-duplex XCVR	DW-16
U2	TPS76350	TI	5-V LDO	DBV-5

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