AN-2105 LM3243 DSBGA Evaluation Board

1 Introduction

The Texas Instruments LM3243 evaluation board is a working demonstration of a step-down DC-DC converter optimized for powering multi-mode 2G/3G/4G RF power amplifiers (PAs) from a single Lithium-Ion cell. Output voltage is set using a VCON analog input for controlling power levels and efficiency of the RF PA.

This user's guide contains information about the evaluation board. For more details and electrical characteristics, please refer to *LM3243 High-Current Step-Down Converter for 2G/3G/4G RF Power Amplifiers* (SNVS782). If you are considering using the LM3243 in a system design, please review the "PCB Layout Considerations" section of the data sheet.

2 Operating Conditions

The device will operate under the following conditions:

- VIN range: 2.7V to 5.5V
- VOUT Range: 0.4V to 3.6V
- VCON range: 0.16V to 1.44V
- VOUT = 2.5 × VCON
- IOUT range: 0mA to 2.5A

3 Package

The LM3243 is available in a 16-bump (0.4 mm pitch) lead-free DSBGA package.

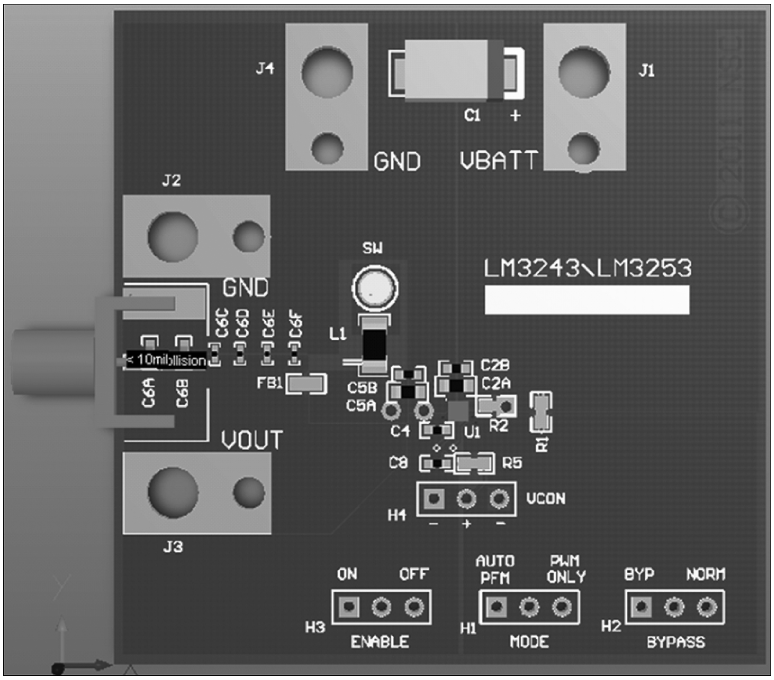


Figure 1. LM3243 Evaluation Board

4 Connection Diagram

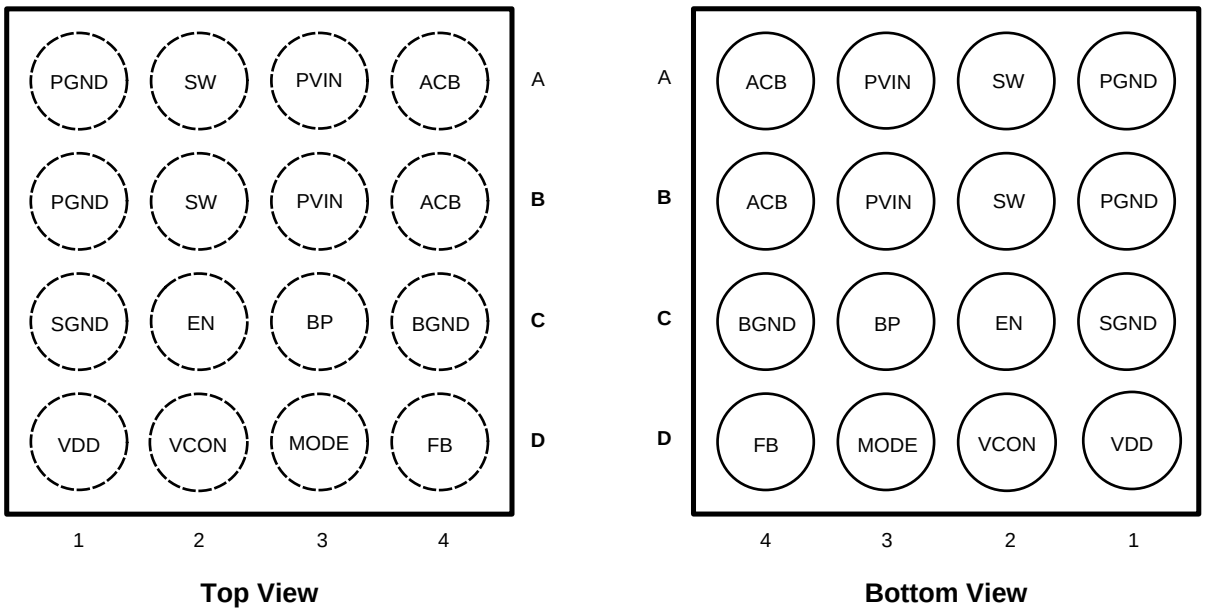


Figure 2. Connection Diagram

5 Pin Descriptions

Pin #	Name	Description
A1	PGND	Power Ground for Buck Regulator.
B1		
C1	SGND	Signal Analog and Control Ground (Low Current).
D1	VDD	Analog Supply Input.
A2	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the $I_{LIM,PFET,Steady\ State}$ Current Limit specification of the LM3243.
B2		
C2	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low. Pin has an 800 kΩ internal pull down resistor.
D2	VCON	Voltage Control Analog input. V_{OUT} = 2.5 * VCON
A3	PVIN	Power Supply Voltage Input to the internal PFET switch.
B3		
C3	BP	Bypass mode Input. Set the pin high for forced bypass mode operation. Set the pin low for automatic Analog Current Bypass mode (recommended).
D3	MODE	PWM/PFM Mode Selection Input. Setting the pin high allows for PFM or PWM depending on the output current and output voltage (2.7 MHz PWM switching). Setting the pin low forces the part to be in PWM only (2.7 MHz Switching).
A4	ACB	Analog Current Bypass. Connect to the output at the output filter capacitor.
B4		
C4	BGND	Analog Current Bypass Ground (High Current).
D4	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.

6 Connections

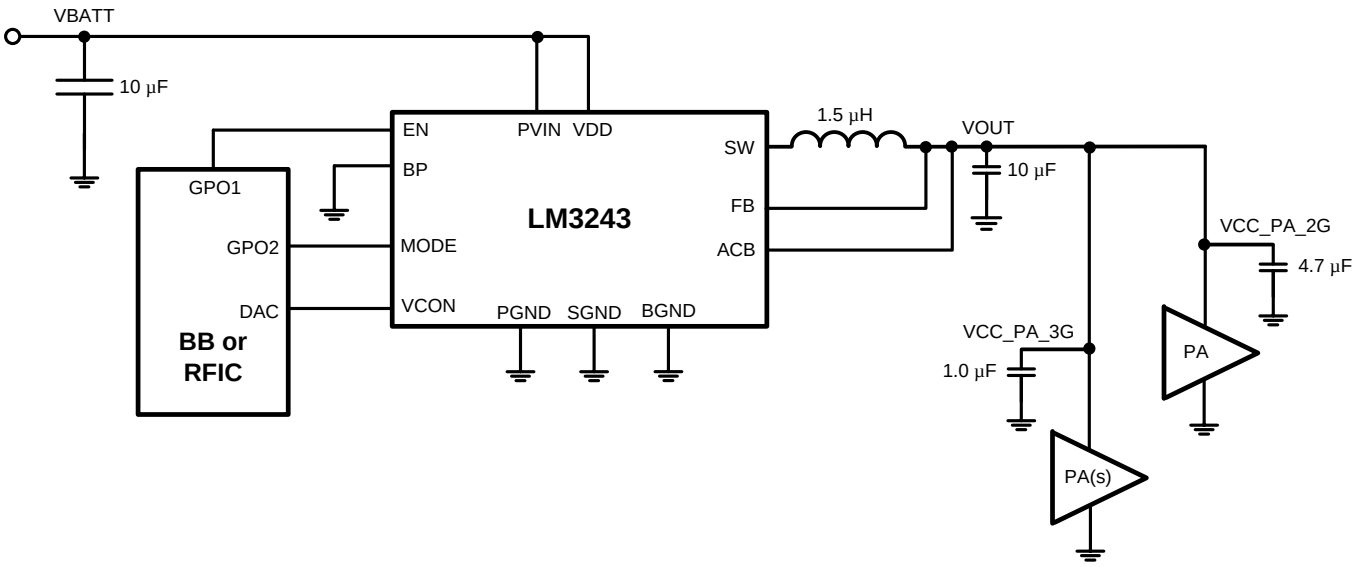
Note that Headers H1 to H4 are 3-pin Header Connectors, with the center pin (Pin 2) connected to the corresponding signal directly to the IC.

1. VBATT is connected to the red (+) and black (gnd) banana connector pins.
2. The load (resistor or PA) is connected to the yellow (+) and black (gnd) banana connector pins.
3. Header H1 - 2G/3G mode:
   - For 2G - the jumper is between center and right pins (PWM only).
   - For 3G - the jumper is between center and left pins (AUTO PFM/PWM).
4. Header H2- Switcher/Forced Bypass mode:
   - Jumper is always between center and right pin (normal switcher mode) for DC/DC switcher operation.
5. Header H3 - Enable of the IC:
   - Disable - Jumper between center and right pin (OFF).
   - Enable - Jumper between center and left pin (ON).
6. Header H4 – VCON:
   - The VCON signal is connected to H4. The center pin is VCON and the pins on either side are GND.

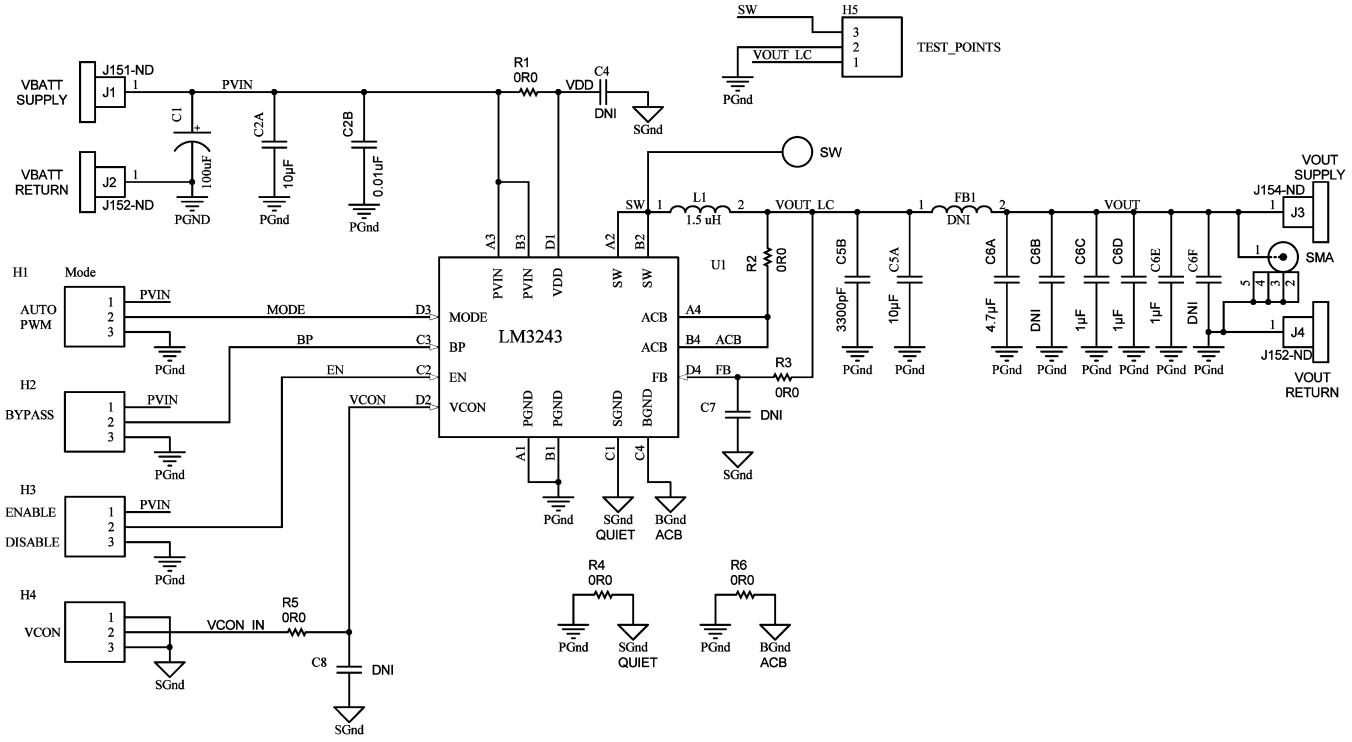
7 Turn-on Sequencing

1. VBATT is turned ON with VCON = LOW (< 0.5V) and EN = LOW (< 0.5V).
2. EN is set to HIGH (> 1.2V).
3. VCON is set to desired voltage level.

8 Typical Application Circuit



9 Evaluation Board Schematic



10 Bill of Materials For Typical Configurations

Designator	Model	Description	Manufacturer
C1	POSCAP or equivalent	100 µF	Sanyo
C2A	GRM185R60J106M	10 µF, 6.3V, 0402	Murata
C2B	GRM022R60J102KE19	10nF, 6.3V, 01005	
L1	DFE201610C-1R5M	1.5 µH, 2.0 mm x 1.6 mm x 1.0 mm	TOKO
C5A	CL05A106MQ5NUN	10 µF, 6.3V, 0402	Samsung
C6A	CL05A475MQ5NRN	4.7 µF, 6.3V, 0402	
C6C, C6D, C6E	CL03A105MQ3S5N	1.0 µF, 6.3V, 0201	
C5B	GRM022R60J332K	3300 pF, 6.3V, X5R, 01005	Murata
U1	LM3243TME	Buck DC/DC Converter	Texas Instruments

11 Evaluation Board Layout

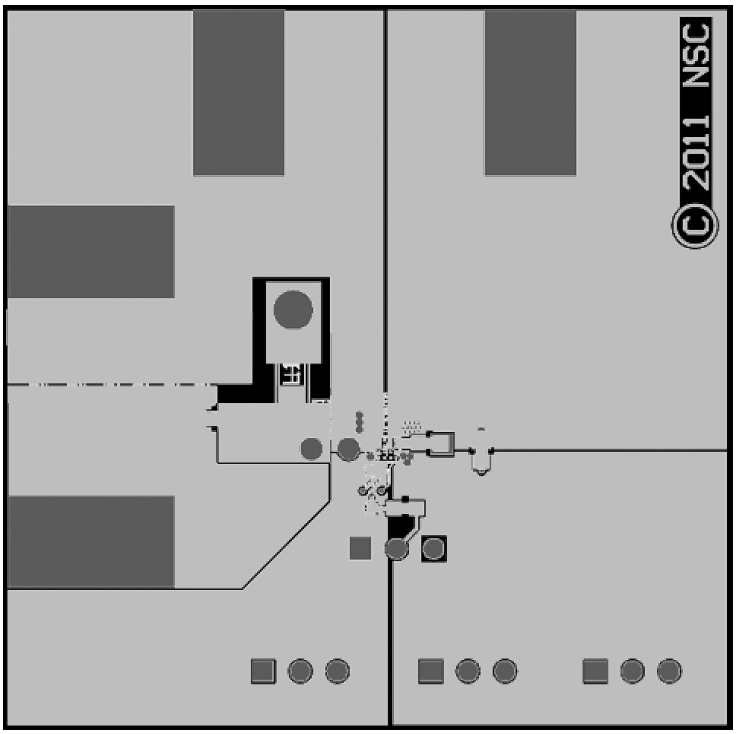


Figure 3. Top Layer:
All Components on Top Layer

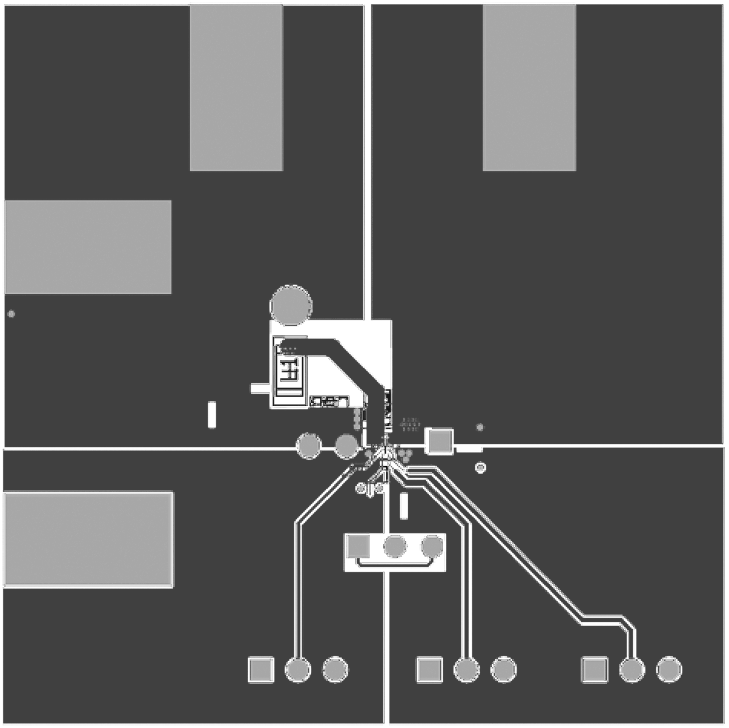


Figure 4. Mid Layer 1:
Switching Path and Power Ground Plane

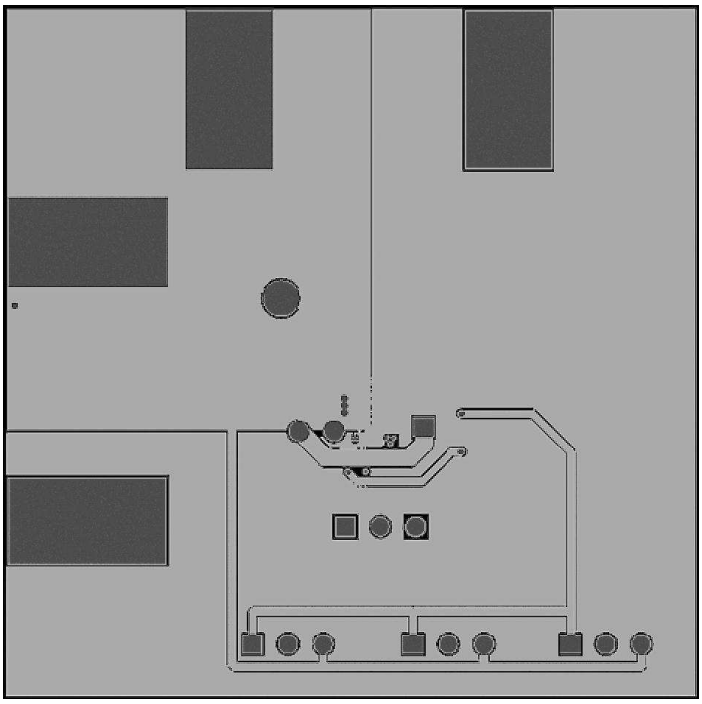


Figure 5. Mid Layer 2:
Digital Signals and ACB

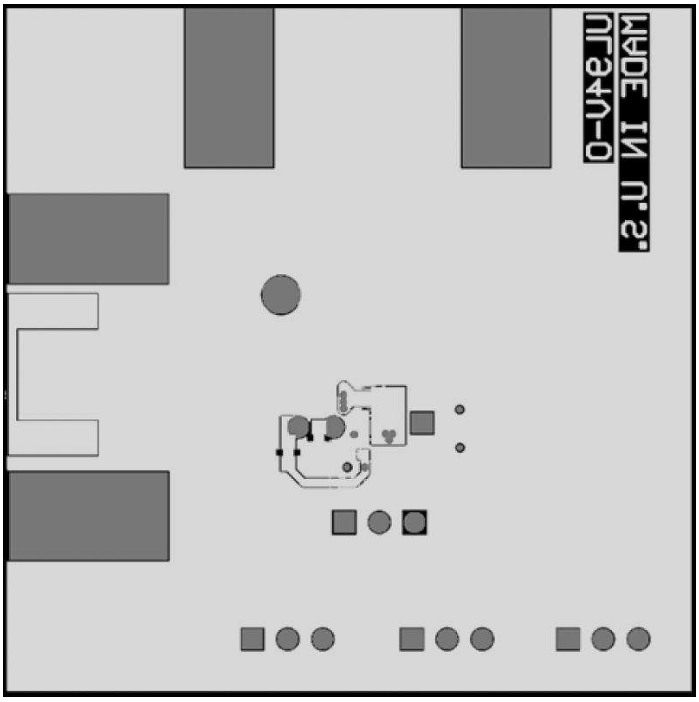


Figure 6. Bottom Layer:
Feedback Path and Power Ground Plane

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