AN-2149 LM5113 Evaluation Board

1 Introduction

The LM5113 evaluation board is designed to provide the design engineers with a synchronous buck converter to evaluate the LM5113, a 100V half-bridge enhancement mode Gallium Nitride (GaN) FET driver. The active clamping voltage mode controller LM5025 is used to generate the PWM signals of the buck switch and the synchronous switch. The specifications of the evaluation board are as follows:

- Input Operating Voltage: 15V to 60V
- Output Voltage: 10V
- Output Current: 10A @ 48V, 7A @ 60V
- Measured Efficiency at 48V: 93.9% @ 10A
- Frequency of Operation: 800kHz
- Line UVLO: 13.8V (Rising) /10.8V (Falling)
- Board size: 3.00 x 2.83 inches

The printed circuit board (PCB) consists of 2 layers of 2 ounce copper on FR4 material, with a thickness of 0.050 inches.

This document contains the schematic of the evaluation board, Bill of Materials (BOM) and a quick setup procedure. The evaluation board can be reconfigured for different switching frequency, dead time, and the output voltage from the specifications above. An example of 48V to 3.3V conversion is given in Appendix A. For more complete information, see the *LM5113 5A, 100V Half-Bridge Gate Driver for Enhancement Mode GaN FETs Data Sheet* (SNVS725)

2 IC Features

- Independent high-side and low-side TTL logic inputs
- 1.2A/5A peak source/sink current
- High-side floating bias voltage rail operates up to 100VDC
- Internal bootstrap supply voltage clamping
- Split outputs for adjustable turn-on/turn-off strength
- 0.6Ω/2.1Ω pull-down/pull-up resistance
- Fast propagation times (28 ns typical)
- Excellent propagation delay matching (1.5 ns typical)
- Supply rail under-voltage lockout
- Low power consumption

3 Powering and Loading Considerations

Certain precautions need to be followed when applying power to the LM5113 evaluation board. A misconnection can damage the assembly.

3.1 Proper Board Connection

Figure 2 depicts the typical evaluation setup. The source power is connected to the J1 (VIN) and the J3 (GND). The load is connected to the J2 (VOUT) and the J4 (GND). Be sure to choose the correct connector and wire size. The input and output voltage must be monitored directly at the terminals of the board. The voltage drop across the connection wires will cause inaccurate measurements.

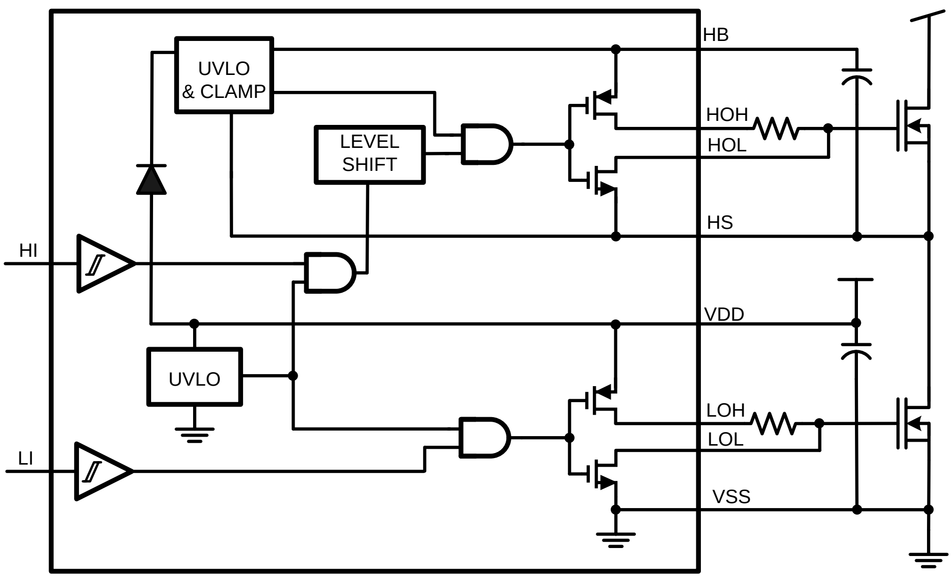


Figure 1. Simplified Block Diagram of LM5113

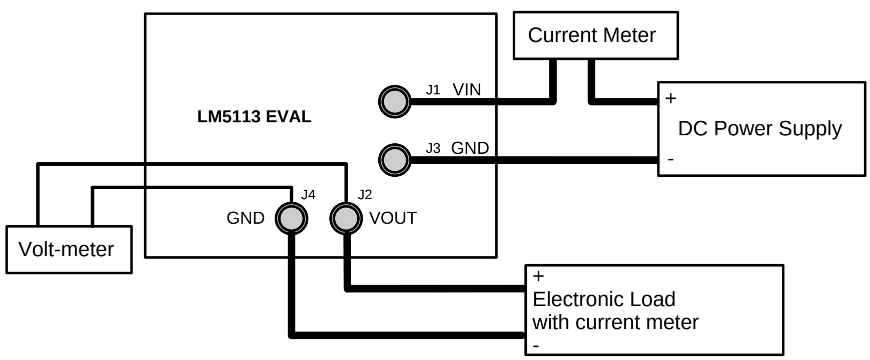


Figure 2. Typical Evaluation Setup

3.2 Source Power

To fully test the LM5113 evaluation board, a DC power supply capable of 60V and 8A is required. The power supply and cabling must present low impedance to the evaluation board. Insufficient cabling or a high impedance power supply will droop during power supply application with the evaluation board inrush current. If large enough, this droop will cause a chattering condition upon power up. This chattering condition is an interaction with the evaluation board under voltage lockout, the cabling impedance and the inrush current.

3.3 Output Current Derating

The LM5113 evaluation board is designed to operate with a maximum load current of 10A for input voltages ranging from 15V to 48V. With further increases of the input voltage, the maximum allowable load current gradually decreases to 7A, to ensure reliable prolonged operation. Figure 3 illustrates the derating curve of the output current at room temperature with airflow of 200CFM. It may be necessary to further reduce the maximum load current at higher ambient temperature.

Note that the LM5113 evaluation board does not have over current protection. Certain precautions should be taken to prevent the load current from exceeding the derating curve shown in Figure 3, otherwise a catastrophic failure may result.

3.4 Air Flow

Sufficient cooling is required to ensure a proper and reliable operation. Especially at high line input and full load, most of the power losses are dissipated in the buck switch. Insufficient airflow can cause overheating of the GaN FETs. A minimum airflow of 200CFM should always be provided.

3.5 Quick Start-Up Procedure

1. Set the current limit of the source supply to provide about 1.5 times the anticipated output power. Connect the source supply to J1 and J3.
2. Connect the load cable between J2 and J4. Disable the load.
3. Set the input voltage and turn on the power supply without load current. Check that the output voltage is 10V.
4. Slowly increase the load current while monitoring the output voltage.

When the evaluation board is powered off, wait for 30 seconds before powering on the evaluation board again to allow the full discharge of the soft start capacitor.

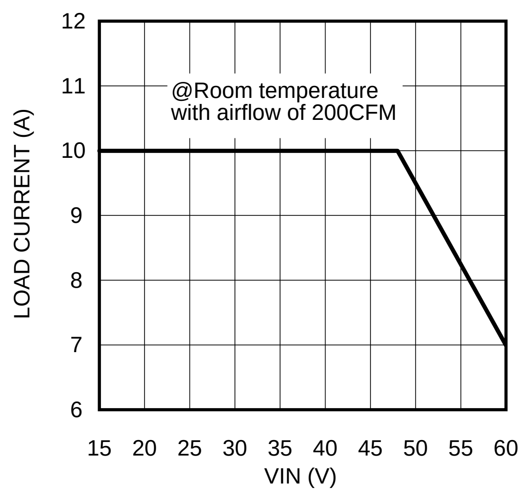


Figure 3. Load Current Derating Curve

4 Performance Characteristics

Figure 4 shows the efficiency of the LM5113 evaluation board at different input voltage and the load current. 30ns dead time between HI and LI input of the LM5113 is selected to eliminate the shoot through while achieving high efficiency.

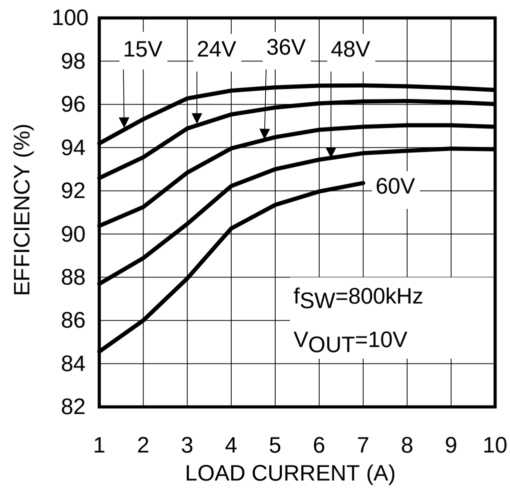


Figure 4. Evaluation Board Efficiency vs. Load Current

During the dead time, the HS pin voltage can be pulled down below -0.7V and results in an excessive bootstrap voltage. The LM5113 has an internal clamping circuitry that prevents the bootstrap voltage from exceeding 5.25V typically. Figure 5 shows the average of the bootstrap voltage with the different load current. As can be seen, the bootstrap voltage is well regulated.

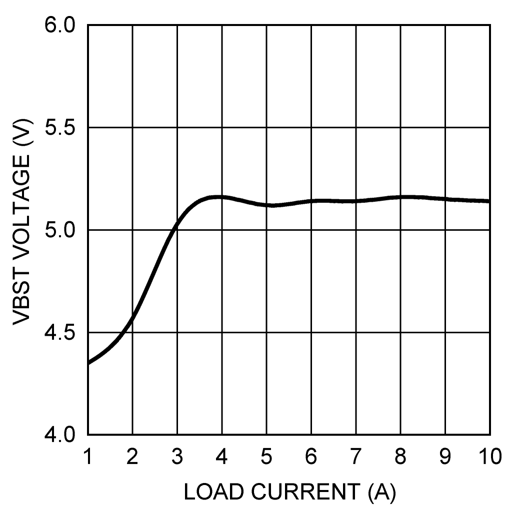
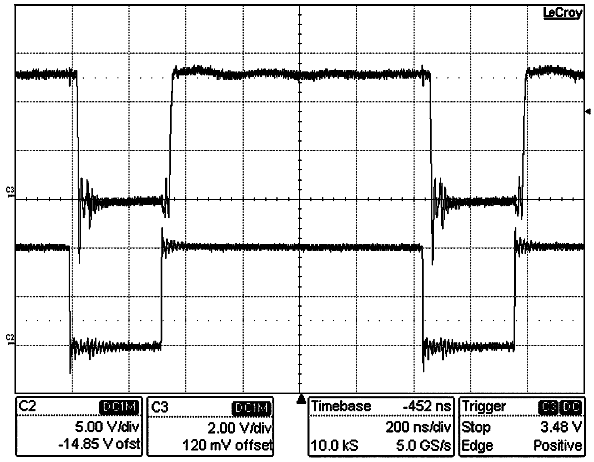


Figure 5. Bootstrap Voltage Regulation vs. Load Current

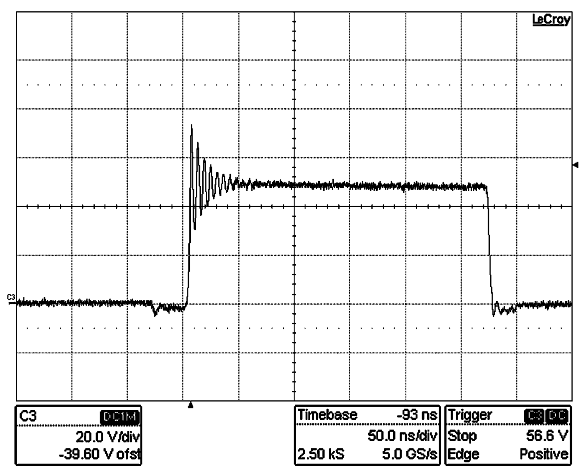
Figure 6 compares the input and the output of the low-side driver.



Conditions:
Input Voltage = 48V DC, Load Current = 5A
Traces:
Top Trace: Gate of Low-Side eGaN FET, Volt/div = 2V
Bottom Trace: LI of LM5113, Volt/div = 5V
Bandwidth Limit = 600MHz
Horizontal Resolution = 0.2 µs/div

Figure 6. Low-Side Driver Input and Output

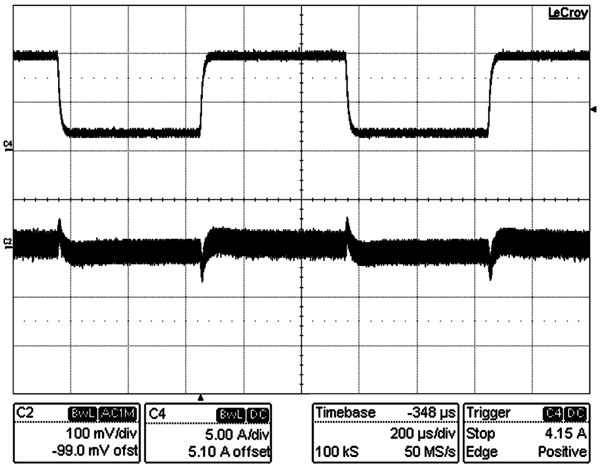
Figure 7 shows the switch node voltage that is also the drain voltage of the low-side FET. The ringing on the switch node voltage can be reduced by the HOH gate resistor. 2Ω HOH gate resistance is selected to achieve a drain-source voltage margin of 12V for a 60V input.



Conditions:
Input Voltage = 48V DC
Load Current = 10A
Traces:
Trace: Switch–Node Voltage, Volts/div = 20V
Bandwidth Limit = 600 MHz
Horizontal Resolution = 50 ns/div

Figure 7. Switch-Node Voltage

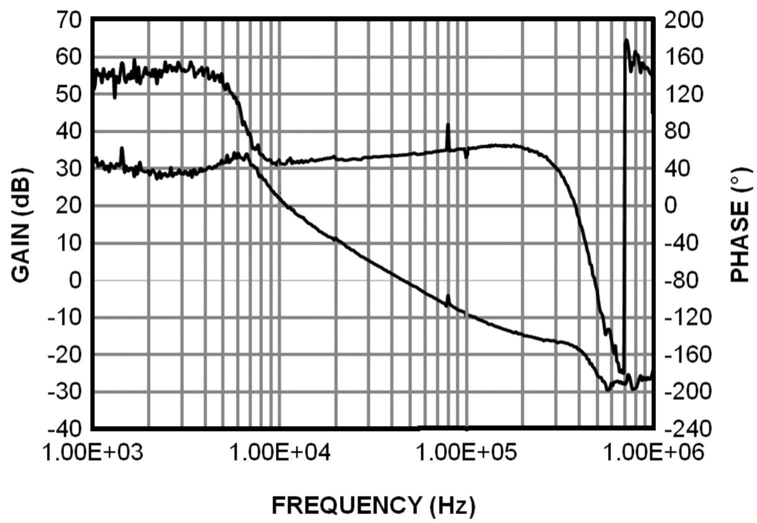
Figure 8 shows the load transient response. The load changes between 2A and 10A. 800 kHz switching frequency allows the use of a small inductor of 2.7uH, which helps improve the large signal transient response.



Conditions:
Input Voltage = 48V DC
Output Current = 2A to 10A
Traces:
Top Trace: Load Current, Amp/div = 5A
Bottom Trace: Output Voltage
Volt/div = 100mV, AC coupled
Bandwidth Limit = 20 MHz
Horizontal Resolution = 0.2 ms/div

Figure 8. Load Transient Response

Figure 9 shows the measured overall loop response. The crossover frequency is 46 kHz and the phase margin is around 55°.



Conditions:
Input Voltage = 48V DC
Output Current = 10A

Figure 9. Loop Gain and Phase

5 Evaluation Board Schematic

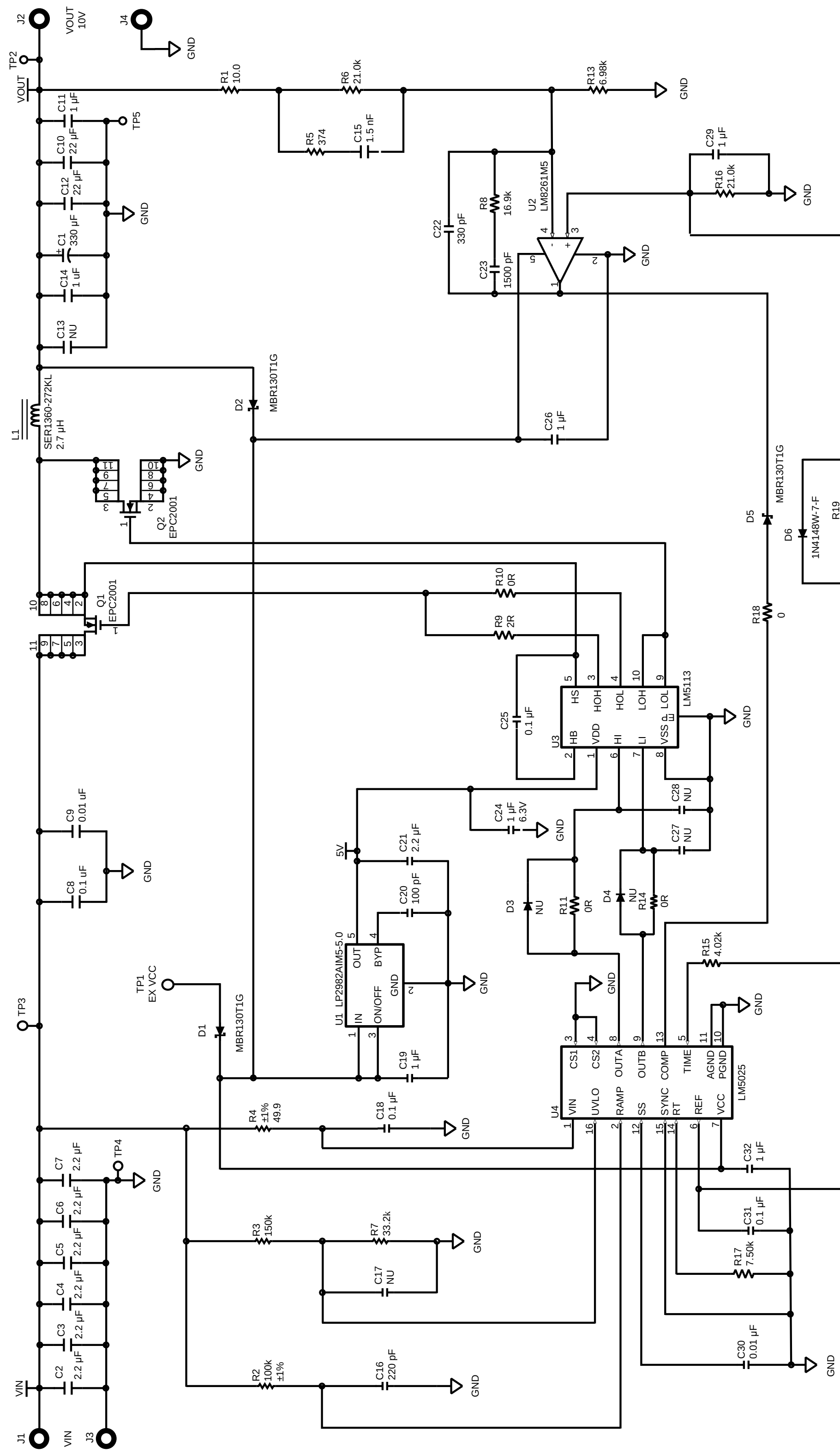


Figure 10. Application Circuit: Input 15V to 60V, Output 10V, 800 kHz

6 Bill of Materials (BOM)

Table 1. Bill of Materials (BOM)

Item	Part	Value	Package	Part Number	Manufacturer
1	C1	CAP, 330uF, 16V, 16mΩ	10mm x 10mm	PCJ1C331MCL1GS	Nippon Chemi-Con
2	C2, C3, C4	CAP, CERM, 2.2uF, 100V, X7R,	1812	C4532X7R2A225M	TDK
3	C5, C6, C7	CAP, CERM, 2.2uF, 100V, X7R	1210	HMK325B7225KN-T	Taiyo Yuden
4	C8	CAP CER .1UF 100V X7R 0603	0603	GRM188R72A104KA35D	Murata
5	C9	CAP CER 10000PF 100V X7R	0603	C1608X7R2A103K	TDK
6	C13	NU			
7	C18, C31	CAP, CERM, 0.1uF, 16V, X7R	0603	C1608X7R1C104K	TDK
8	C10, C12	CAP CER 22UF 16V X7R	1210	C3225X7R1C226K	TDK
9	C14, C11, C19, C26, C29, C32	CAP, CERM, 1uF, 16V, X7R	0603	C1608X7R1C105K	TDK
10	C15, C23	CAP, CERM, 1500pF, 25V, +/-5%, C0G/NP0	0603	GRM1885C1E152JA01D	MuRata
11	C16	CAP, CERM, 220pF, 100V, X7R	0603	06031C221KAT2A	AVX
12	C17	NU			
13	C20	CAP, CERM, 100pF, 25V, X7R	0603	06033C101KAT2A	AVX
14	C21	CAP, CERM, 2.2uF, 10V, X7R	0603	GRM188R71A225KE15D	Murata
15	C22	CAP, CERM, 330pF, 50V, +/-5%, C0G/NP0	0603	GRM1885C1H331JA01D	Murata
16	C24	CAP, CERM, 1uF, 6.3V, X5R	0402	C1005X5R0J105M	TDK
17	C25	CAP CER .1UF 16V X7R	0402	GRM155R71C104KA88D	TDK
18	C27, C28	NU			
19	C30	CAP, CERM, 0.01uF, 50V, X7R	0603	GRM188R71H103KA01D	Murata
20	D1, D2, D5	Diode, Schottky, 30V, 1A	SOD-123	MBR130T1G	ON Semiconductor
21	D3, D4	NU	SOD-323		
22	D6	Diode, Ultrafast, 100V, 0.15A	SOD-123	1N4148W-7-F	Diodes Inc
23	L1	Inductor, Shielded E Core, Ferrite, 2.7uH, 12A	SMD 12.6mmX12.7mm	SER1360-272KLB	Coilcraft
24	Q1, Q2	eGaN FET, 100V, 25A, 7mΩ	4105um X 1632 um	EPC2001	EPC
25	R1	RES, 10.0 ohm, 1%, 0.1W	0603	RC0603FR-0710RL	Yageo America
26	R2	RES, 100k ohm, 1%, 0.125W	0805	CRCW0805100KFKEA	Vishay-Dale
27	R3	RES, 150k ohm, 1%, 0.125W	0805	CRCW0805150KFKEA	Vishay-Dale
28	R4	RES 49.9 OHM 1/8W 1%	0805	CRCW080549R9FKEA	Vishay-Dale
29	R5	RES, 374 ohm, 1%, 0.1W	0603	CRCW0603374RFKEA	Vishay-Dale
30	R6, R16, R19	RES, 21.0k ohm, 1%, 0.1W	0603	RC0603FR-0721KL	Yageo America

Table 1. Bill of Materials (BOM) (continued)

Item	Part	Value	Package	Part Number	Manufacturer
31	R7	RES, 33.2k ohm, 1%, 0.1W	0603	RC0603FR-0733K2L	Yageo America
32	R8	RES, 16.9k ohm, 1%, 0.1W	0603	RC0603FR-0716K9L	Yageo America
33	R9	RES, 2.00 ohm, 1%, 0.063W	0402	CRCW04022R00FKED	Vishay-Dale
34	R10	RES, 0.0 Ohm, 1/10W	0402	ERJ-2GE0R00X	Panasonic
35	R11, R14, R18	RES, 0 ohm, 5%, 0.1W	0603	ERJ-3GEY0R00V	Panasonic
36	R13	RES, 6.98k ohm, 1%, 0.1W	0603	RC0603FR-076K98L	Yageo America
37	R15	RES, 4.02k ohm, 1%, 0.1W	0603	RC0603FR-074K02L	Yageo America
38	R17	RES, 7.50k ohm, 1%, 0.1W	0603	CRCW06037K50FKEA	Vishay-Dale
39	U1	5.0V, 50 mA LDO	SOT-23	LP2982	Texas Instruments
40	U2	Op Amp	SOT-23	LM8261	Texas Instruments
41	U3	5A, 100V, GaN FET Driver	DSBGA-10	LM5113	Texas Instruments
42	U4	Active clamp voltage mode PWM Controller	16–pin TSSOP	LM5025	Texas Instruments

7 PCB Layouts

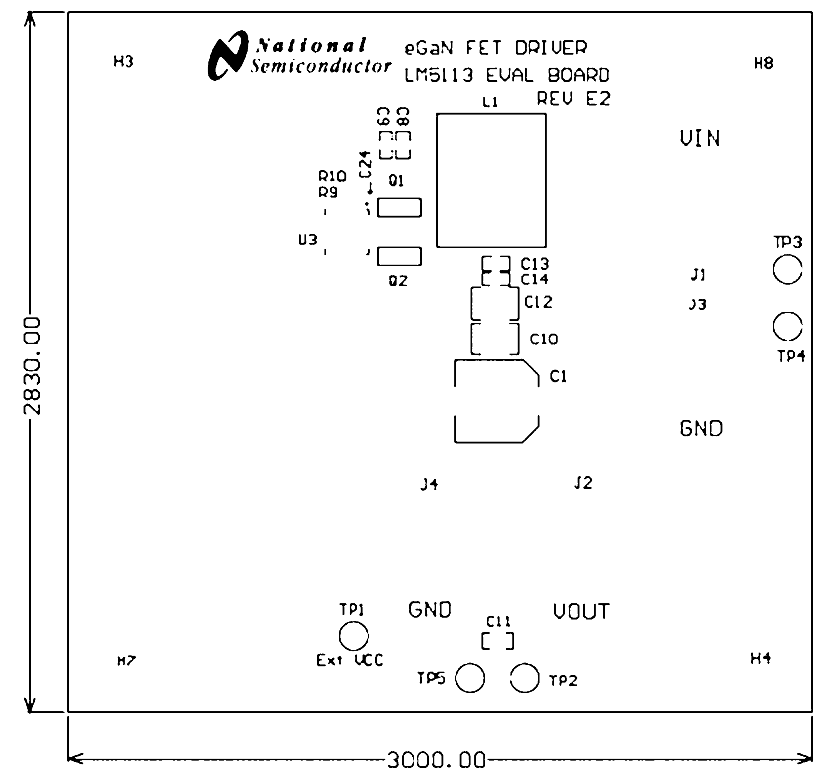


Figure 11. Top Side Silk Screen

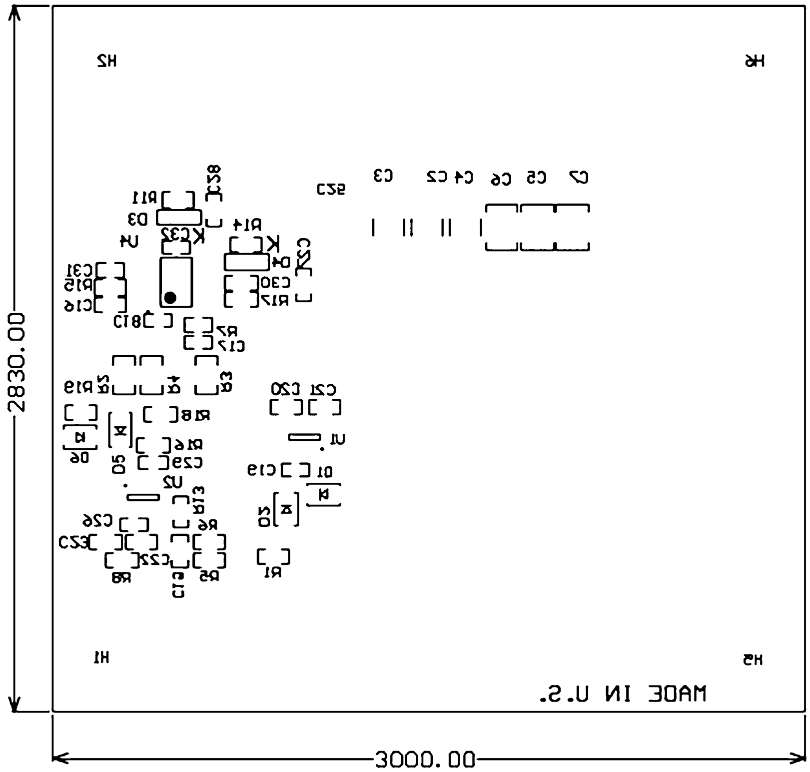


Figure 12. Bottom Side Silk Screen

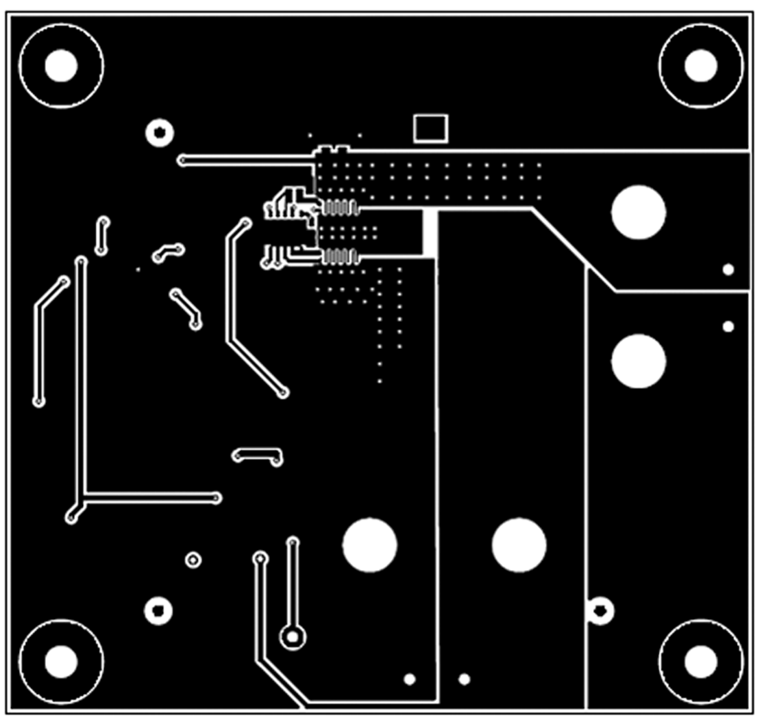


Figure 13. Top Layer

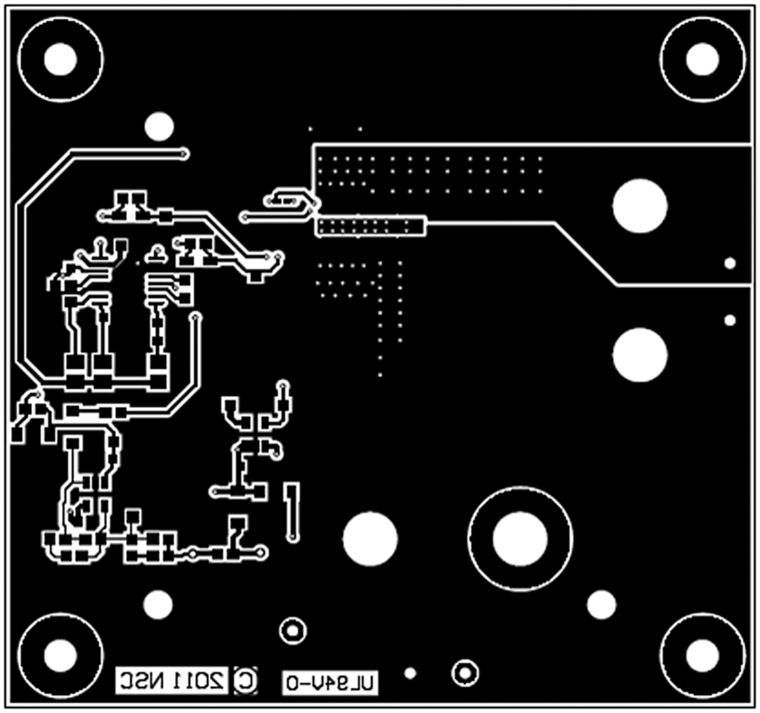


Figure 14. Bottom Layer

Appendix A 48V to 3.3V Conversion

The LM5113 evaluation board can also be reconfigured for different switching frequency, dead time and output voltage. By adjusting the resistor R17, the PWM controller LM5025 can operate up to 1MHz. The dead time can be adjusted with the resistor R15, and/or with RCD circuitry at the inputs of the LM5113. The output voltage can be adjusted with R16 as follows:

$$R16 = \frac{21 \times V_0}{20 - V_0} \, k\Omega \tag{1}$$

It should be noted that the maximum output power may be derated to ensure the safe operation of the GaN FETs when the evaluation board is configured for the switching frequency beyond the preceding specifications.

Figure 15 shows the design for a 48V to 3.3V conversion. The switching frequency is set at 500 kHz. It should be noted that the bias supply for the control circuitry is generated from the internal LDO of the LM5025. To aid thermal dissipation, sufficient cooling should be provided for the LM5025. Alternatively, an external 10V supply can be connected to the terminal TP1 EXT VCC to provide the bias voltage for the control circuitry.

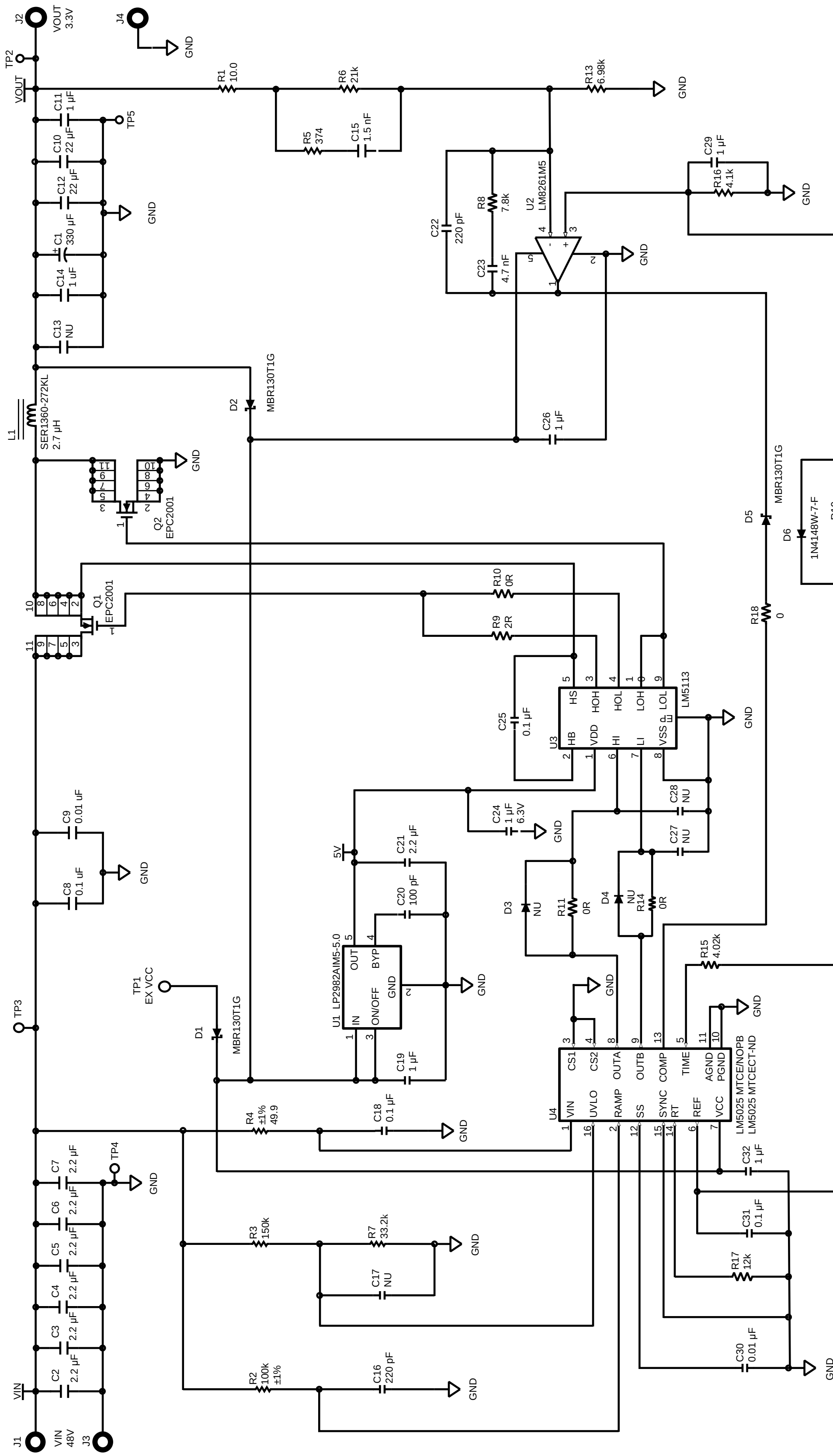


Figure 15. Application Circuit: Input 48V, Output 3.3V, 10A, 500 kHz

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