

Full Bridge Power Amplifier

FEATURES

- Dual Power Operational Amplifiers
- $\pm 2A$ Output Current Guaranteed
- Precision Current Sense Amplifier
- Two Supply Monitoring Inputs
- Parking Function and Under-Voltage Lockout
- Safe Operating Area Protection
- 3V to 35V Operation

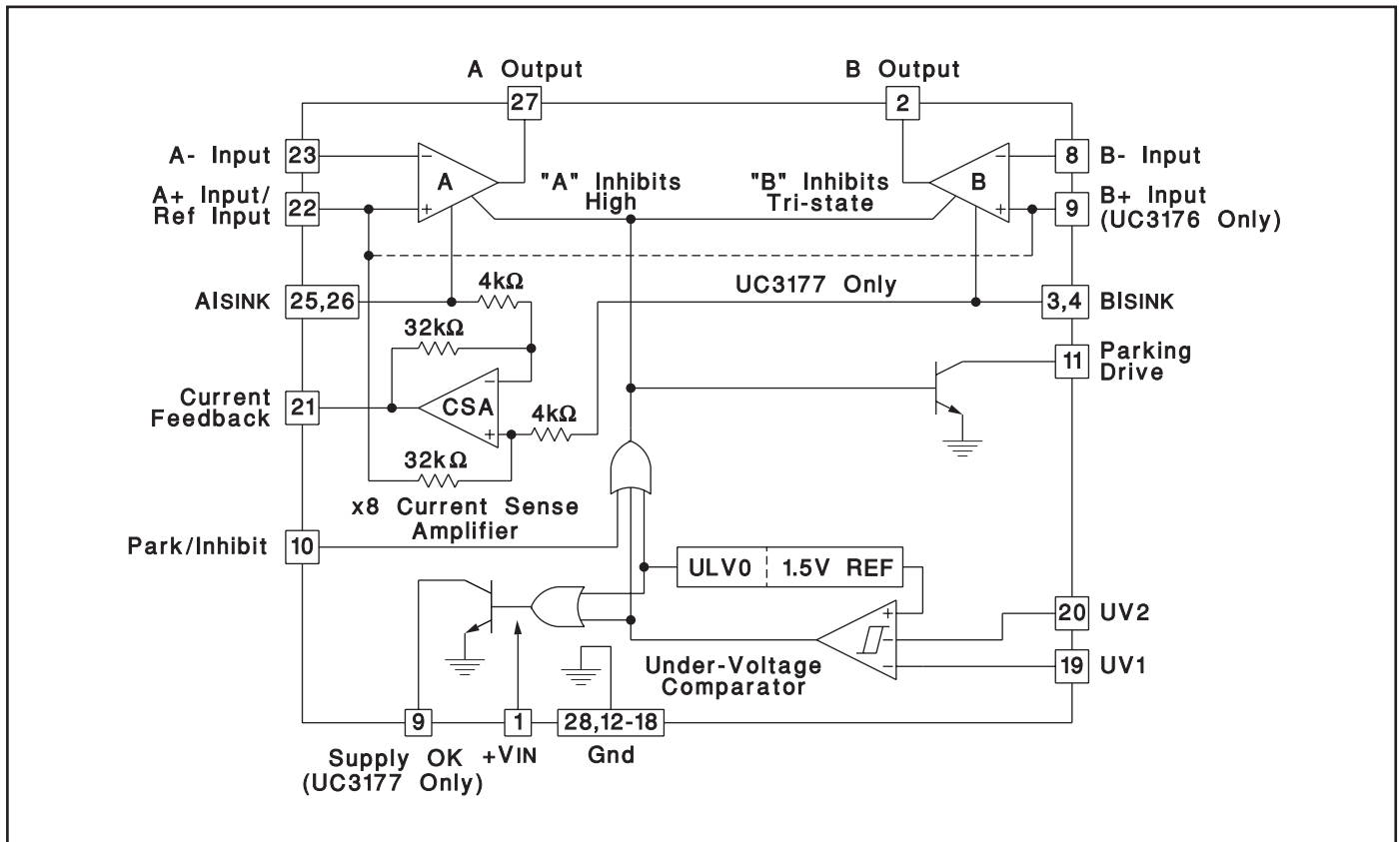
DESCRIPTION

The UC3176/7 family of full bridge power amplifiers is rated for a continuous output current of 2A. Intended for use in demanding servo applications such as disk head positioning, the onboard current sense amplifier can be used to obtain precision control of load current, or where voltage mode drive is required, a standard voltage feedback scheme can be used. Output stage protection includes foldback current limiting and thermal shutdown, resulting in a very rugged device.

Auxiliary functions on this device include a dual input under-voltage comparator that can be programmed to respond to low voltage conditions on two independent supplies. In response to an under-voltage condition the power Op-Amps are inhibited and a high current, 100mA, open collector drive output is activated. A separate Park/Inhibit command input.

The devices are operational over a 3V to 35V supply range. Internal under-voltage lockout provides predictable power-up and power-down characteristics.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

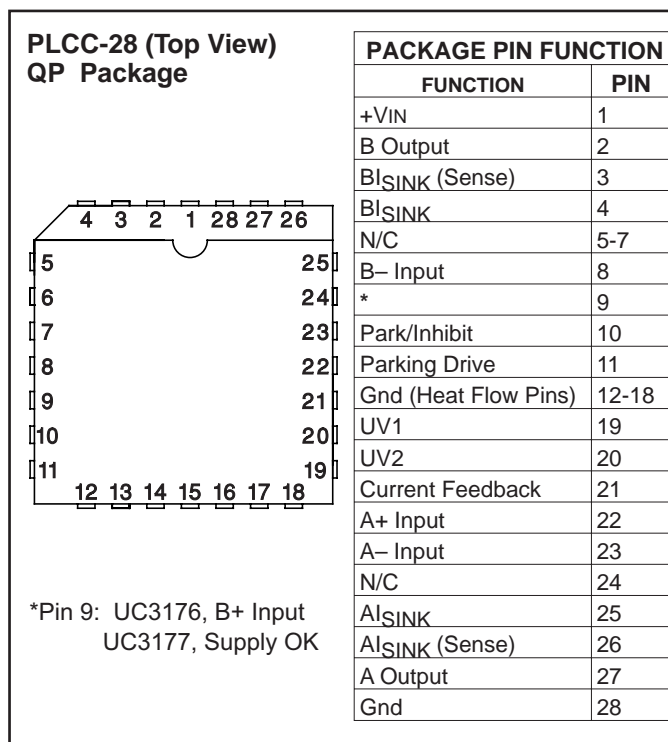
Input Supply voltage, (+V _{IN})	40V
Park/Inhibit, UV1 and UV2 inputs (zener clamped)	
Maximum forced voltage	-0.3V to 10V
Maximum forced current	±10mA
Other Input Voltages	-0.3V to +V _{IN}
A _{SINK} and B _{SINK} Voltages	-0.3V to 6V
Open Collector Output Voltages	40V
A and B Output Currents (Continuous)	
Source	Internally Limited
Sink	2.5A
Total Supply Current (Continuous)	4A
Parking Drive Output Current (Continuous)	200mA
Supply OK Output Current, UC3177 (Continuous)	30mA
Operating Junction Temperature	-55°C to +150°C
Power Dissipation at TC = +75°C	
QP package	4W
Storage Temperature	-65°C to +150°C

THERMAL DATA

QP package:

Thermal Resistance Junction to Leads, θ_{JL}	15°C/W
Thermal Resistance Junction to Ambient, θ_{JA}	50°C/W
Thermal Resistance Junction to C _{OSC} , θ_{JC}	30°C/W

CONNECTION DIAGRAM

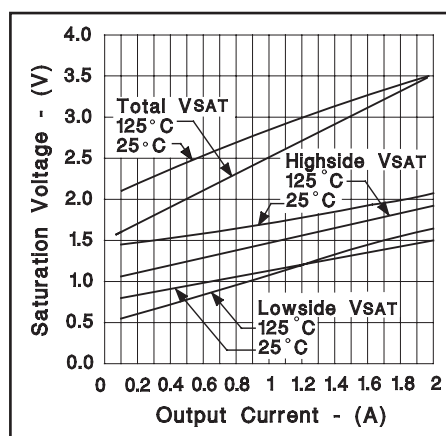


ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0 to 70°C, +V_{IN} = 12V, T_A = T_J.

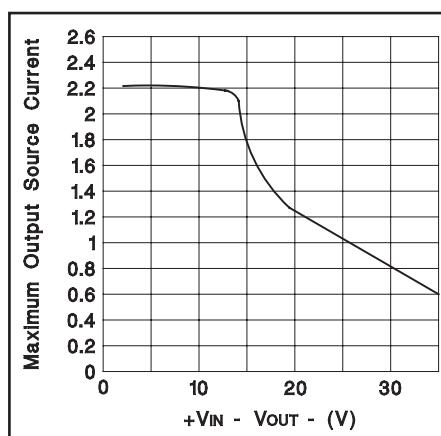
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	+V _{IN} = 12V		18	25	mA
	+V _{IN} = 35V		21	30	mA
UVOL Threshold	+V _{IN} low to high		2.8	3.0	V
	Threshold Hysteresis		220	300	mV
Power, Amplifier, A and B					
Input Offset Voltage	V _{CM} = 6V, V _{OUT} = 6V			8	mV
Input Bias Current	V _{CM} = 6V, Except A+ Input	-500	-100		nA
Input Bias Current at A+/Reference Input	(A+/REF - B _{SINK}) / 36kΩ; T _J = 25°C	23	28	35	μA/V
Input Offset Current B Amp (UC3176 Only)	V _{CM} = 6V			200	nA
CMRR	V _{CM} = 1 to 33V, +V _{IN} = 35V, V _{OUT} = 6V	70	100		dB
PSRR	+V _{IN} = 5 to 35V, V _{CM} = 2.5V	70	100		dB
Large Signal Voltage Gain	V _{OUT} = 3V, w/I _{OUT} = 1A to V _{OUT} = 9V, w/I _{OUT} = -1A	1.5	4		V/mV
Thermal Feedback	+V _{IN} = 20V, Pd = 20W at opposite output		25	200	μV/W
Saturation Voltage	I _{OUT} = -2A, High Side, T _J = 25°		1.9		V
	C _I _{OUT} = 2A, Low Side, T _J = 25°C		1.6		V
	Total V _{SAT} at 2A, T _J = 25°C		3.5	3.7	V
Unity Gain Bandwidth			1		MHz
Slew Rate			1		V/μs
Differential I _{OUT} Sense Error Current in Bridge Configuration	I _{OUT} (A) = -I _{OUT} (B), /I _{OUT} / - /A _{SINK} - B _{SINK} /				
	I _{OUT} ≤ 200mA		3.0	6.0	mA
	I _{OUT} ≤ 2A		5.0	10	mA
High Side Current Limiting	=V _{IN} - V _{OUT} < 12V		-2.7	-2.0	A

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for $T_A = 0$ to 70°C , $+V_{IN} = 12\text{V}$, $T_A = T_J$.

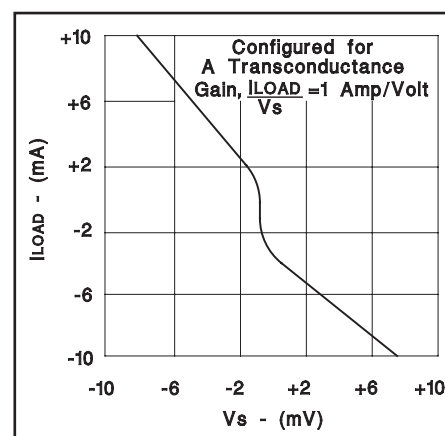
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Current Sense Amplifier					
Input Offset Voltage	$V_{CM} = 0\text{V}$, A+ / REF at 6V			3	mV
	REF = 2V to 20V, $+V_{IN} = 35$, change with REF Input voltage			600	$\mu\text{V/V}$
Thermal Gradient Sensitivity	$+V_{IN} = 20\text{V}$, REF = 10V Pd = 20W @ A or B Output		5.0	75.0	$\mu\text{V/W}$
PSRR	REF = 2.5V, $+V_{IN} = 5$ to 35V	70	100		dB
Gain	$ A_{SINK-B SINK} \leq 0.5\text{V}$	7.8	8.0	8.1	V/V
Slew Rate			2		V/ μS
3dB Bandwidth			1		MHz
MAX Output Current	$I_{SOURCE} = +V_{IN} - V_{OUT} = 0.5\text{V}$	2.5	3.5		mA
Output Saturation Voltage	$I_{SOURCE} = 1.5\text{mA}$, High Side		0.15	0.30	V
	$I_{SINK} = 5\text{mA}$, Low Side		1.4	1.85	V
Under-Voltage Comparator					
Threshold Voltage	Low to High, other input at 5V	1.44	1.50	1.56	V
	Threshold Hysteresis	50	70	80	mV
Input Current	Input = 2V, other input at 5V	-2.00	-0.05		μA
Supply OK V_{SAT} (UC3177 Only)	$I_{OUT} = 5\text{mA}$			0.45	V
Supply OK Leakage (UC3177 Only)	$V_{OUT} = 35\text{V}$			5	μA
Park/Inhibit					
Park/Inhibit Th'l'd		1.1	1.3	1.7	V
Park/Inhibit Input Current	At threshold		60	100	μA
Parking Drive Saturation Voltage	$I_{OUT} = 100\text{mA}$		0.3	0.7	V
Parking Drive Leakage	$V_{OUT} = 35\text{V}$			15	μA
Thermal Shutdown					
Shutdown Temperature			165		$^\circ\text{C}$



Output saturation voltage vs. current.

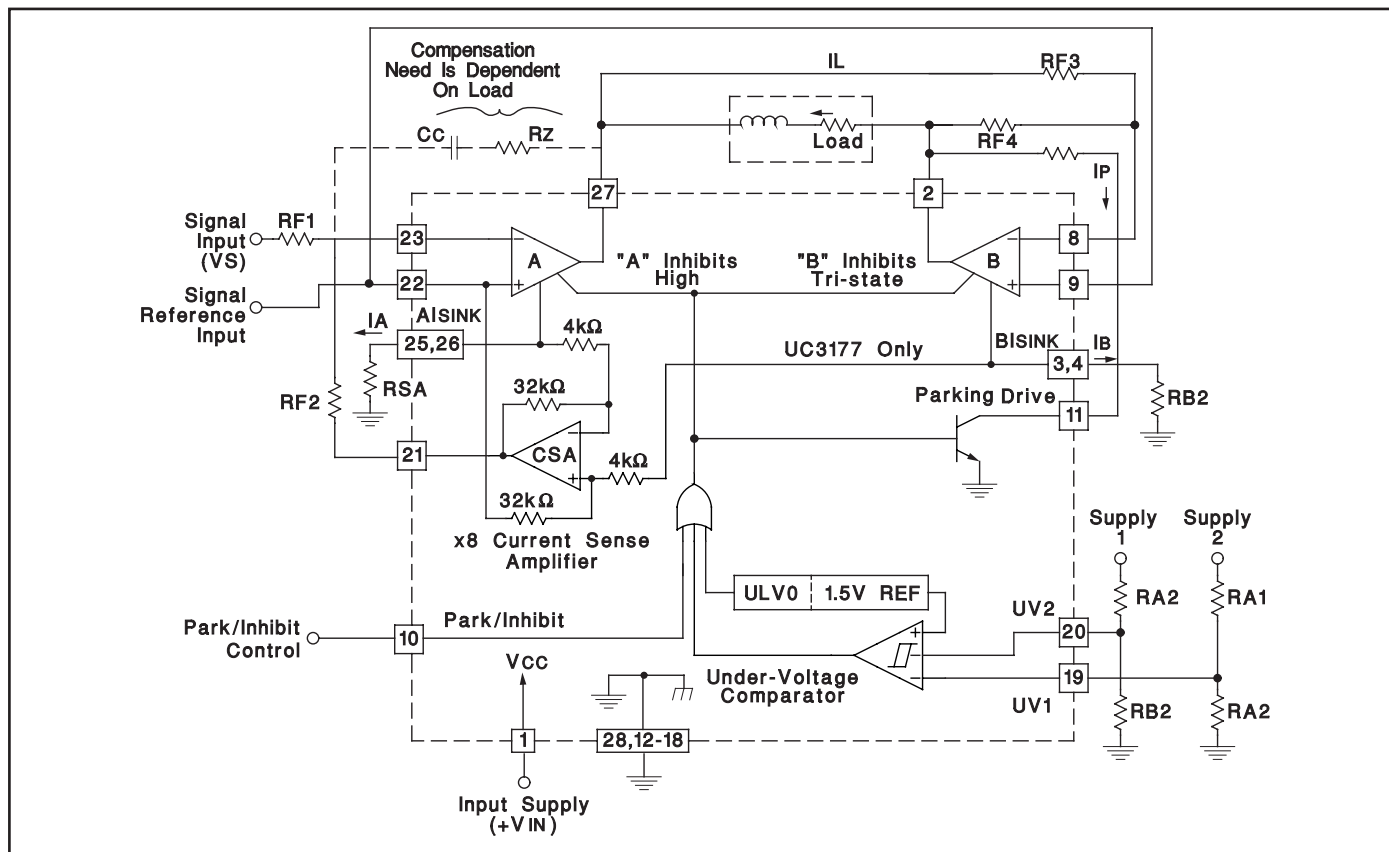


Maximum source current vs. $+V_{IN} - V_{OUT}$.

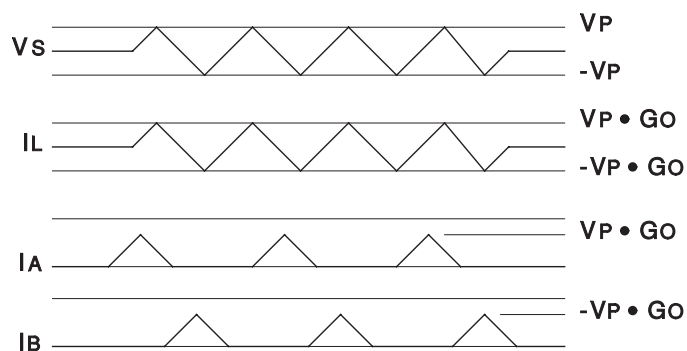


Crossover current error characteristic.

APPLICATION AND OPERATION INFORMATION



WAVEFORMS FOR ABOVE APPLICATION



DESIGN EQUATIONS

$$\text{Transconductance } (G_O) = \frac{I_L}{V_S} = \frac{R_{F2}}{R_{F1}} \times \left(\frac{1}{8R_S} \right)$$

with: $R_{SA} = R_{SB}$ and $R_{F3} = R_{F4}$

$$\text{Parking Current } (I_P) = \frac{V_{IN} - 1.5}{R_P + R_L}$$

where: R_L = load resistance

Under-Voltage Thresholds, at Supplies
 High to Low Threshold, $(V_{LH}) = 1.425 (R_A + R_B) / R_B$
 Low to High Threshold, $(V_{HL}) = 1.5 (R_A + R_B) / R_B$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UC3176QP	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	UC3176QP	Samples
UC3176QPTR	ACTIVE	PLCC	FN	28	750	TBD	Call TI	Call TI	0 to 70	UC3176QP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

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