ACML-7400, ACML-7410 and ACML-7420

3.3 V/5 V 100 MBd High Speed CMOS Digital Isolator

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

ACML-7400, ACML-7410 and ACML-7420 are multi-channel high speed CMOS digital isolators. Using magnetic coupling through a thick insulation barrier, the isolators enable high speed transmissions without compromise in isolation performance. These isolators consume low power even at high data rates, yet provide excellent transient immunity performance in compact surface mount packages. The devices are qualified to a maximum propagation delay of 36 ns and a maximum pulse width distortion of 3 ns. They are capable of running at a 100 MBaud data rate

ACML-7400, ACML-7410 and ACML-7420 are available in 16-pin SOIC wide-body packages. They operate at dual 3.3 V/5 V supply voltages. The DC and timing specifications are specified over the temperature range of -40° C to +105° C. ACML-7400, ACML-7410 and ACML-7420 are built using CMOS input buffers and CMOS output drivers to eliminate the need for both input limiters and output pull-up resistors. Refresh circuitry is built in to ensure DC-correctness.

Applications

- Isolated data interfaces
- Data acquisition
- Digital oscilloscopes
- Power meters
- High speed video transmission

Features

- Dual supply voltage compatible – 3.3 V & 5 V
- Wide operating temperature range (-40° C to +105° C)
- Support high speed data rate of at least 100 MBd
- Lower power consumption – 15 mA per channel typical
- Low propagation delay: 36 ns max
- Low propagation delay skew
  - Channel-to-channel: 4 ns max
  - Part-to-part: 8 ns max
- Low pulse width distortion: 3 ns max
- Safety and Regulatory Approvals

  UL Recognised
  - 5600 V_{RMS} for 1 min. per UL1577
  - CSA Component Acceptance Notice #5

  IEC 60950-1
  - Basic Insulation, 800 V_{RMS} max. working voltage
  - Reinforced Insulation, 400 V_{RMS} max. working voltage

  IEC 61010-1
  - Basic Insulation, 800 V_{RMS} max. working voltage
  - Reinforced Insulation, 400 V_{RMS} max. working voltage

  IEC 60601-1
  - 2 Means of Patient Protection, 250 V_{RMS} max. working voltage
  - 2 Means of Operator Protectioin, 400 V_{RMS} max. working voltage
- High Common Mode Transient Immunity – 25 kV/μs min
- CMOS buffer input and output
- DC correctness
- Lead-free

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Device Selection Guide

Device Number	Channel Configuration	Package
ACML-7400	Quad, All-in-One	16-pin Small Outline, Wide Body
ACML-7410	Quad, Bi-directional, 3/1	16-pin Small Outline, Wide Body
ACML-7420	Quad, Bi-directional, 2/2	16-pin Small Outline, Wide Body

Ordering Information

ACML-7400, ACML-7410 and ACML-7420 are UL Recognized with 5600 V_{RMS} for 1 minute per UL1577.

Part number	Option	Package	Surface Mount	Tape & Reel	UL 5600 V_{RMS} / 1 Minute rating	Quantity
	RoHS Compliant					
ACML-7400	-000E	Wide Body SO-16	X		X	45 per tube
ACML-7410 ACML-7420	-500E		X	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

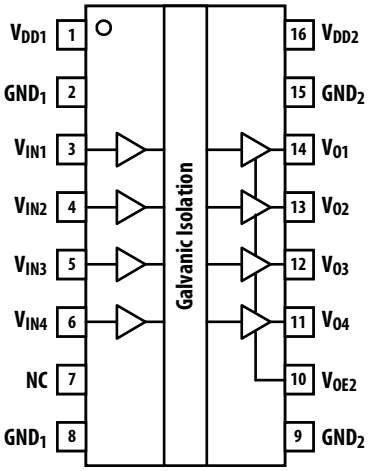
ACML-7420-500E to order product of Wide Body SO-16 package in Tape and Reel in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

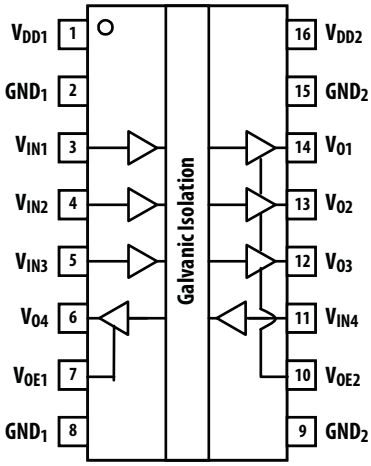
Functional Diagram

Quad Channel

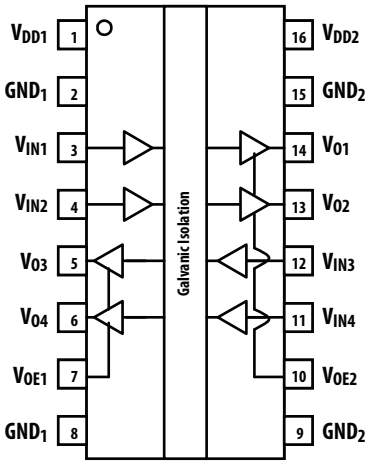
ACML-7400



ACML-7410



ACML-7420



Pin Description

Pin	Description
V_{DD1}, V_{DD2}	Power supply at primary and secondary side
GND_1, GND_2	Ground at primary and secondary side
V_{IN1}, V_{IN2}, V_{IN3}, V_{IN4}	Input for channel 1, 2, 3 and 4
V_{O1}, V_{O2}, V_{O3}, V_{O4}	Output for channel 1, 2, 3 and 4
V_{OE1}, V_{OE2}	Output enable at V_{DD1} and V_{DD2} side, these pins should be connected to the respective V_{DD} when not in use.
NC	No connectivity

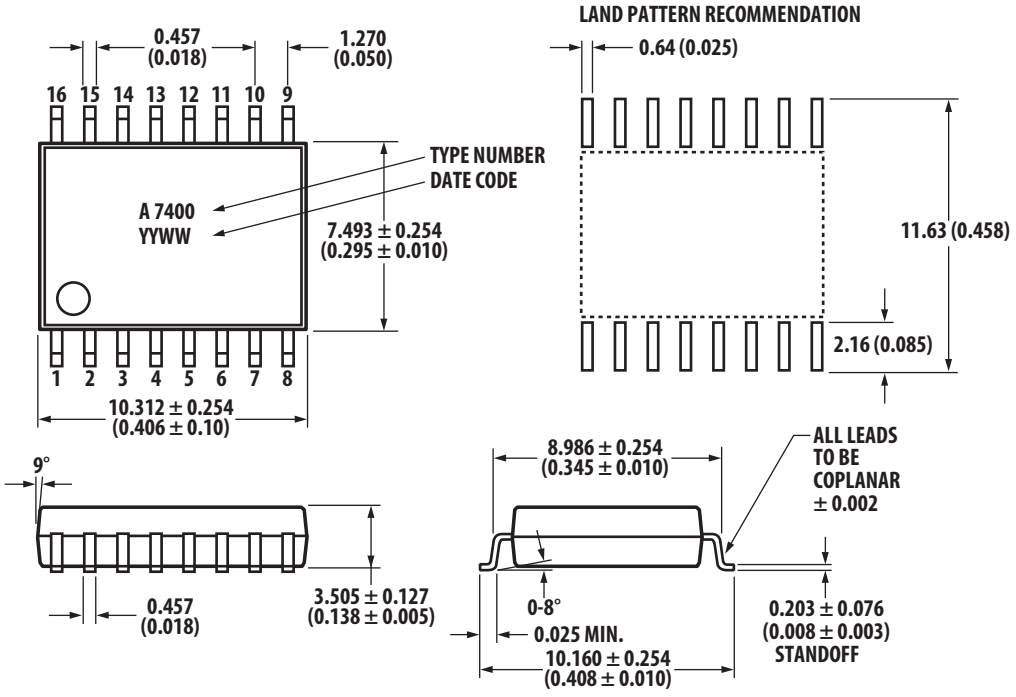
Truth Table (ACML-7410)

V_{DD1}	$V_{IN1,IN2,IN3}$	V_{OE1}	V_{O4}	V_{DD2}	V_{IN4}	V_{OE2}	$V_{O1, O2, O3}$	Remark
H	H	X	X	H	X	H or NC	H	Input ($V_{IN1, IN2, IN3}$) logic High during normal operation. The default state for V_{OE2} is High state.
H	L	X	X	H	X	H or NC	L	Input ($V_{IN1, IN2, IN3}$) logic Low during normal operation. The default state for V_{OE2} is High state.
H	X	X	X	H	X	L	Z	Output ($V_{O1, O2, O3}$) is disabled to high impedance state when V_{OE2} is set to Low.
L	X	X	X	H	X	H	H	When V_{DD1} is not powered, the output ($V_{O1, O2, O3}$) default state is High. Output ($V_{O1, O2, O3}$) typically restored 100 µs after V_{DD1} is restored.
H	X	H or NC	H	H	H	X	X	Input (V_{IN4}) logic High during normal operation. The default state for V_{OE1} is High state.
H	X	H or NC	L	H	L	X	X	Input (V_{IN4}) logic Low during normal operation. The default state for V_{OE1} is High state.
H	X	L	Z	H	X	X	X	Output (V_{O4}) is disabled to high impedance state when V_{OE1} is set to Low.
H	X	H	H	L	X	X	X	When V_{DD2} is not powered, the output (V_{O4}) default state is High. Output (V_{O4}) typically restored 100 µs after V_{DD2} is restored.

X means don't care
NC means not connection.

Package Outline Drawings

ACML-7400, ACML-7410 and ACML-7420 16-Lead Surface Mount (SOIC-16) Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACML-7400, ACML-7410 and ACML-7420 are approved by the following organizations:

UL

UL1577, component recognition program.
CSA Component Acceptance Service Notice #5A.

TUV Rheinland

	IEC 60950-1		IEC 61010-1		IEC 60601-1	
Insulation Category	**Reinforced**	**Basic**	**Reinforced**	**Basic**	**2 Means of Patient Protection**	**2 Means of Operator Protection**
Working Voltage	400 V_{RMS} (567 V_{PEAK})	800 V_{RMS} (1132 V_{PEAK})	400 V_{RMS} (567 V_{PEAK})	800 V_{RMS} (1132 V_{PEAK})	250 V_{RMS} (354 V_{PEAK})	400 V_{RMS} (567 V_{PEAK})

Insulation and Safety Related Specifications

Parameter	Symbol	ACML-7400 ACML-7410 ACML-7420	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.1	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.05	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All creepage and clearance pertain to the isolation component itself. These dimensions are needed as a starting point for the designer when determining the circuit insulation requirements, and not reflective of the equipment standard requirements.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units
Storage Temperature		T_S	-55	+125	°C
Ambient Operating Temperature		T_A	-40	+125	°C
Supply Voltages		V_{DD1}, V_{DD2}	0	6.5	Volts
Input Voltage		V_I	-0.5	V_{DD} +0.5	Volts
Output Voltage		V_O	-0.5	V_{DD} +0.5	Volts
Average Output Current		I_O		±15	mA
Electrostatic Discharge	Human Body Model	HBM		±4	kV
	Charge Device Model	CDM		±1	kV
Solder Reflow Temperature Profile		Please refer to Solder Reflow Temperature Profile			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Notes
Ambient Operating Temperature	T_A	-40	+105	°C	
Supply Voltages (3.3 V operation)	V_{DD1}, V_{DD2}	3.0	3.6	V	
Supply Voltages (5 V operation)	V_{DD1}, V_{DD2}	4.5	5.5	V	
Logic High Input Voltage	V_{IH}	0.7 x V_{DD}	V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0.0	0.3 x V_{DD}	V	

Electrical Specifications

The following specifications apply to ACML-7400 and are applicable to ambient temperature of -40° C ≤ T_A ≤ 105° C, input supply of 3.0 V ≤ V_{DD1} ≤ 3.6 V or 4.5 V ≤ V_{DD1} ≤ 5.5 V, and output supply of 3.0 V ≤ V_{DD2} ≤ 3.6 V or 4.5 V ≤ V_{DD2} ≤ 5.5 V. All typical specifications at T_A = +25° C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Notes
Input Supply Current, No data	$I_{DD1(0)}$		5.9*	10	mA		No Input	1,7	1
			6.8**			V_{DD1} = 5.5 V			
Input Supply Current, 25 MBd data rate	$I_{DD1(25)}$		16		mA	V_{DD1} = 3.3 V	12.5 MHz logic signal	1,7	2
			17			V_{DD1} = 5.0 V			
Input Supply Current, 100 MBd data rate	$I_{DD1(100)}$		30*	40	mA	V_{DD1} = 3.6 V	50 MHz logic signal	1,7	2
			31**	40		V_{DD1} = 5.5 V			
Output Supply Current, No data	$I_{DD2(0)}$		12*	16	mA		No Input	2,8	3
			13**			V_{DD1} = 5.5 V			
Output Supply Current, 25 MBd	$I_{DD2(25)}$		15		mA	V_{DD1} = 3.3 V	12.5 MHz logic signal	2,8	4
			17			V_{DD1} = 5.0 V			
Output Supply Current, 100 MBd data rate	$I_{DD2(100)}$		23*	32	mA	V_{DD1} = 3.6 V	50 MHz logic signal	2,8	4
			30**	40		V_{DD1} = 5.5 V			
Logic Input Current	I_{IN}	-10		10	µA				
Logic High Output Voltage	V_{OH}	V_{DD}-0.1	V_{DD}-0.02		V	I_{OUT} = -20 µA, V_{IN} = V_{DD1}			
		0.8*V_{DD}	V_{DD}-0.25		V	I_{OUT} = -4 mA, V_{IN} = V_{DD1}			
Logic Low Output Voltage	V_{OL}		0.02	0.1	V	I_{OUT} = 20 µA, V_{IN} = 0 V			
			0.25	0.8	V	I_{OUT} = 4 mA, V_{IN} = 0 V			

* Typical data based on 3.3 V supply, ** Typical data based on 5.0 V supply

The following specifications apply to ACML-7410 and are applicable to ambient temperature of -40° C ≤ T_A ≤ 105° C, input supply of 3.0 V ≤ V_{DD1} ≤ 3.6 V or 4.5 V ≤ V_{DD1} ≤ 5.5 V, and output supply of 3.0 V ≤ V_{DD2} ≤ 3.6 V or 4.5 V ≤ V_{DD2} ≤ 5.5 V. All typical specifications at T_A = +25° C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Notes
Input Supply Current, No data	$I_{DD1(0)}$		8.4*	11.5	mA		No Input	3,7	1
			9.4**			V_{DD1} = 5.5 V			
Input Supply Current, 25 MBd data rate	$I_{DD1(25)}$		15.5*		mA	V_{DD1} = 3.3 V	12.5 MHz logic signal	3,7	2
			17**			V_{DD1} = 5.0 V			
Input Supply Current, 100 MBd data rate	$I_{DD1(100)}$		28.5*	38	mA	V_{DD1} = 3.6 V	50 MHz logic signal	3,7	2
			30.5**	40		V_{DD1} = 5.5 V			
Output Supply Current, No data	$I_{DD2(0)}$		9.5*	14.5	mA		No Input	4,8	3
			10.4**			V_{DD1} = 5.5 V			
Output Supply Current, 25 MBd	$I_{DD2(25)}$		15*		mA	V_{DD1} = 3.3 V	12.5 MHz logic signal	4,8	4
			17**			V_{DD1} = 5.0 V			
Output Supply Current, 100 MBd data rate	$I_{DD2(100)}$		25*	34	mA	V_{DD1} = 3.6 V	50 MHz logic signal	4,8	4
			30**	40		V_{DD1} = 5.5 V			
Logic Input Current	I_{IN}	-10		10	µA				
Logic High Output Voltage	V_{OH}	V_{DD}-0.1	V_{DD}-0.02		V	I_{OUT} = -20 µA, V_{IN} = V_{DD1}			
		0.8*V_{DD}	V_{DD}-0.25		V	I_{OUT} = -4 mA, V_{IN} = V_{DD1}			
Logic Low Output Voltage	V_{OL}		0.02	0.1	V	I_{OUT} = 20 µA, V_{IN} = 0 V			
			0.25	0.8	V	I_{OUT} = 4 mA, V_{IN} = 0 V			

* Typical data based on 3.3 V supply, ** Typical data based on 5.0 V supply

The following specifications apply to ACML-7420 and are applicable to ambient temperature of -40° C ≤ T_A ≤ 105° C, input supply of 3.0 V ≤ V_{DD1} ≤ 3.6 V or 4.5 V ≤ V_{DD1} ≤ 5.5 V, and output supply of 3.0 V ≤ V_{DD2} ≤ 3.6 V or 4.5 V ≤ V_{DD2} ≤ 5.5 V. All typical specifications at T_A = +25° C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Notes
Input Supply Current, No data	$I_{DD1(0)}$		9.0*	13	mA		No Input	5,7	1
			9.9**			V_{DD1} = 5.5 V			
Input Supply Current, 25 MBd data rate	$I_{DD1(25)}$		15*		mA	V_{DD1} = 3.3 V	12.5 MHz logic signal	5,7	2
			17**			V_{DD1} = 5.0 V			
Input Supply Current, 100 MBd data rate	$I_{DD1(100)}$		27*	36	mA	V_{DD1} = 3.6 V	50 MHz logic signal	5,7	2
			30**	40		V_{DD1} = 5.5 V			
Output Supply Current, No data	$I_{DD2(0)}$		9.0*	13	mA		No Input	6,8	3
			9.9**			V_{DD1} = 5.5 V			
Output Supply Current, 25 MBd	$I_{DD2(25)}$		15*		mA	V_{DD1} = 3.3 V	12.5 MHz logic signal	6,8	4
			17**			V_{DD1} = 5.0 V			
Output Supply Current, 100 MBd data rate	$I_{DD2(100)}$		27*	36	mA	V_{DD1} = 3.6 V	50 MHz logic signal	6,8	4
			30**	40		V_{DD1} = 5.5 V			
Logic Input Current	I_{IN}	-10		10	µA				
Logic High Output Voltage	V_{OH}	V_{DD}-0.1	V_{DD}-0.02		V	I_{OUT} = -20 µA, V_{IN} = V_{DD1}			
		0.8*V_{DD}	V_{DD}-0.25		V	I_{OUT} = -4 mA, V_{IN} = V_{DD1}			
Logic Low Output Voltage	V_{OL}		0.02	0.1	V	I_{OUT} = 20 µA, V_{IN} = 0 V			
			0.25	0.8	V	I_{OUT} = 4 mA, V_{IN} = 0 V			

* Typical data based on 3.3 V supply, ** Typical data based on 5.0 V supply

Switching Specifications

The following specifications apply to ACML-7400, ACML-7410 and ACML-7420 and are applicable to ambient temperature of -40° C ≤ T_A ≤ 105° C, input supply of 3.0 V ≤ V_{DD1} ≤ 3.6 V or 4.5 V ≤ V_{DD1} ≤ 5.5 V, and output supply of 3.0 V ≤ V_{DD2} ≤ 3.6 V or 4.5 V ≤ V_{DD2} ≤ 5.5 V, unless further specified. All typical specifications are at T_A = +25° C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Notes
Maximum Data Rate		100			MBd	50 MHz Logic Signal		
Minimum Pulse Width				10	ns	50 MHz Logic Signal		
Propogation Delay Time to Logic Low Output	t_{PHL}	18	27	32	ns	4.5 V ≤ V_{DD1} = V_{DD2} ≤ 5.5 V, C_L = 15 pF	9	5
Propogation Delay Time to Logic High Output	t_{PLH}	18	27	32	ns		9	5
Pulse Width Distortion	PWD	-2	0	2	ns		11	6
Propagation Delay Channel Skew	t_{CSK}		0	3	ns		12	7
Propagation Delay Part Skew	t_{PSK}		1	5	ns			8
Propogation Delay Time to Logic Low Output	t_{PHL}	20	28	36	ns	C_L = 15 pF	9,10	5
Propogation Delay Time to Logic High Output	t_{PLH}	20	27.5	36	ns		9,10	5
Pulse Width Distortion	PWD	-3	0.5	3	ns		11	6
Propagation Delay Channel Skew	t_{CSK}		0	4	ns		12	7
Propagation Delay Part Skew	t_{PSK}		1	8	ns			8
Output Rise Time (10% – 90%)	t_R		3		ns	C_L = 15 pF		
Output Fall Time (90% - 10%)	t_F		3		ns	C_L = 15 pF		
Output Enable time	t_{ENABLE}		10		ns	V_{IN} = 0 V or V_{DD}		9
Output Disable time	$t_{DISABLE}$		10		ns	V_{IN} = 0 V or V_{DD}		10
Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	25	>40		kV/µs	V_{CM} = 1000 V, T_A = 25° C, V_{IN} = V_{DD} V_O > 0.8 x V_{DD}		11
Common Mode Transient Immunity at Logic Low Output	$\lvert CM_L \rvert$	25	>40		kV/µs	V_{CM} = 1000 V, T_A = 25° C, V_{IN} = 0 V, V_O < 0.8 V		11

Package Characteristics

All Typicals at T_A = 25° C.

Parameters	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Input-Output Momentary With-stand Voltage	V_{ISO}	5600			V_{RMS}	RH ≤ 50%, t = 1 min, T_A = 25°C	12, 13, 14
Input-Output Resistance	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 V dc	12
Input-Output Capacitance	C_{I-O}		1.9		pF	f = 1 MHz	12
Input Capacitance	C_I		4.3		pF		15
Package Power Dissipation	P_{PD}			750	mW	T_A = 25° C	

Notes:

1. $I_{DD1(0)}$ is the supply current consumption at V_{DD1} of ACML-7400, ACML-7410 and ACML-7420 when there is no signal to all inputs.
2. $I_{DD1(F)}$ is the supply current consumption at V_{DD1} of ACML-7400, ACML-7410 and ACML-7420 when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.
3. $I_{DD2(0)}$ is the supply current consumption at V_{DD2} of ACML-7400, ACML-7410 and ACML-7420 when there is no signal to all inputs.
4. $I_{DD2(F)}$ is the supply current consumption at V_{DD2} of ACML-7400, ACML-7410 and ACML-7420 when inputs are switching at the specified data rate, and outputs are switching at same data rate with no load.
5. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_{IN} signal to the 50% level of the falling edge of the V_{OUT} signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_{IN} signal to the 50% level of the rising edge of the V_{OUT} signal.
6. PWD is defined as t_{PHL} -t_{PLH}.
7. t_{CSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between channels of the same unit at any given temperature and supply voltages within the recommended operating conditions.
8. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and supply voltages within the recommended operating conditions.
9. t_{ENABLE} is the duration when V_{OE} is set to High state and output is restored per input signal ($V_O = V_{IN}$).
10. $t_{DISABLE}$ is the duration when V_{OE} is set to Low and V_O is switched to high impedance state.
11. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8\ V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_{OUT} < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
12. Device considered a two-terminal device: pins 1, 2, 3, 4, 5, 6, 7, 8 shorted together and pins 9, 10, 11, 12, 13, 14, 15 and 16 shorted together.
13. In accordance with UL1577, each ACML-7400, ACML-7410 AND ACML-7420 device is proof tested by applying an insulation test voltage 6800 V_{RMS} for 1 second.
14. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refers to your equipment level safety specification.
15. C_I is the capacitance measured at input pin.

Characteristic Curves

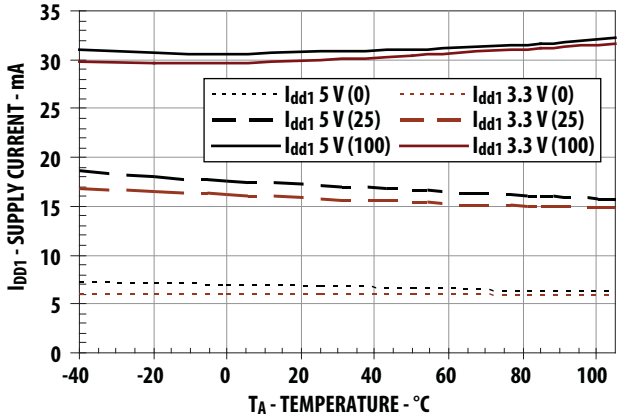


Figure 1. Typical I_{DD1} of ACML-7400 vs Temperature

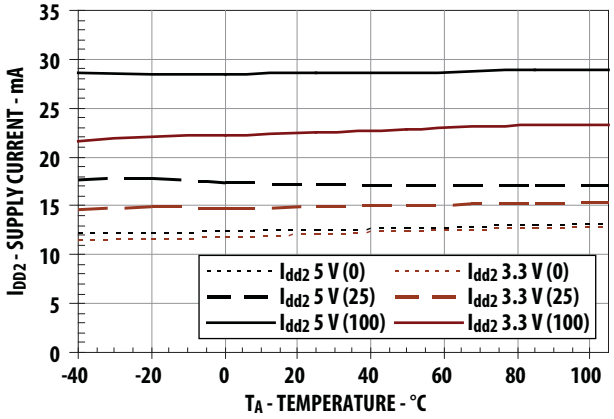


Figure 2. Typical I_{DD2} of ACML-7400 vs Temperature

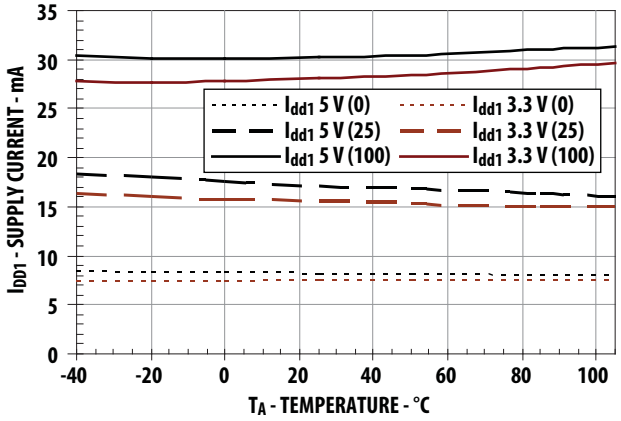


Figure 3. Typical I_{DD1} of ACML-7410 vs Temperature

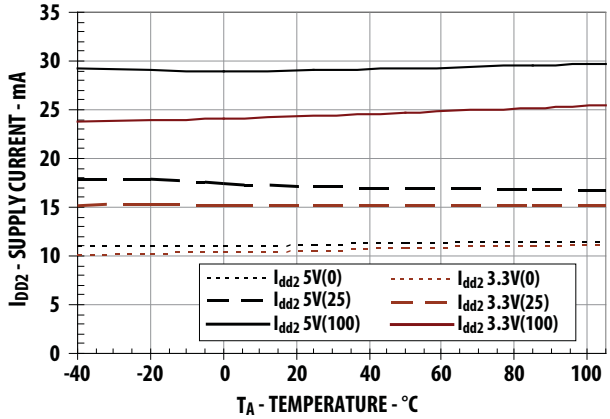


Figure 4. Typical I_{DD2} of ACML-7410 vs Temperature

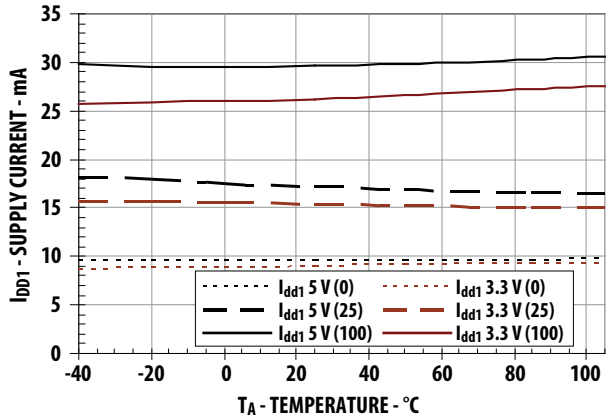


Figure 5. Typical I_{DD1} of ACML-7420 vs Temperature

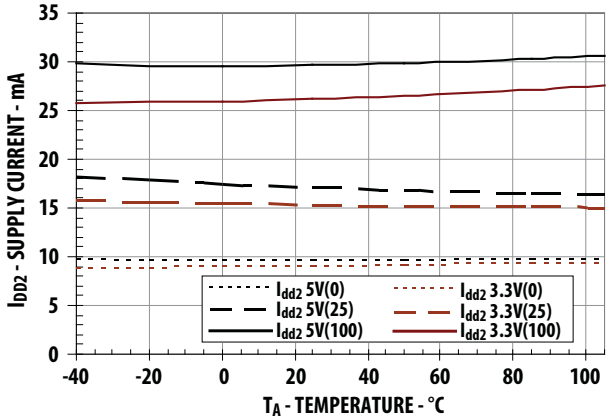


Figure 6. Typical I_{DD2} of ACML-7420 vs Temperature

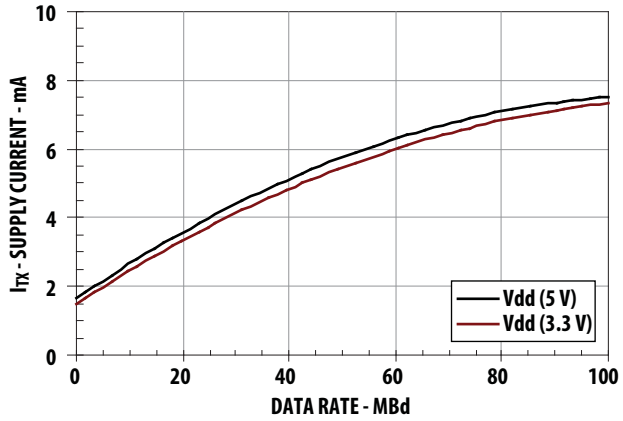


Figure 7. Typical Supply Current per Transmit Channel vs Data Rate

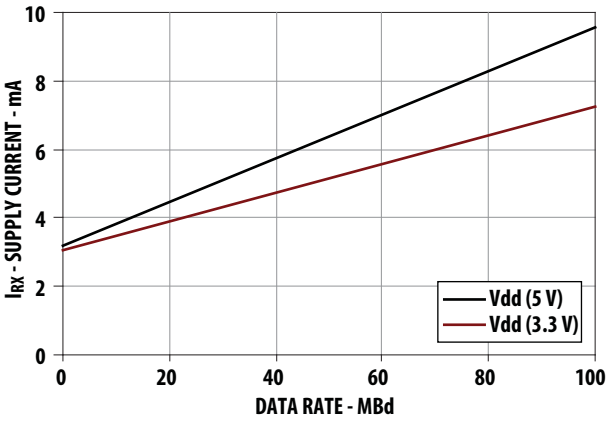


Figure 8. Typical Supply Current per Receive Channel vs Data Rate

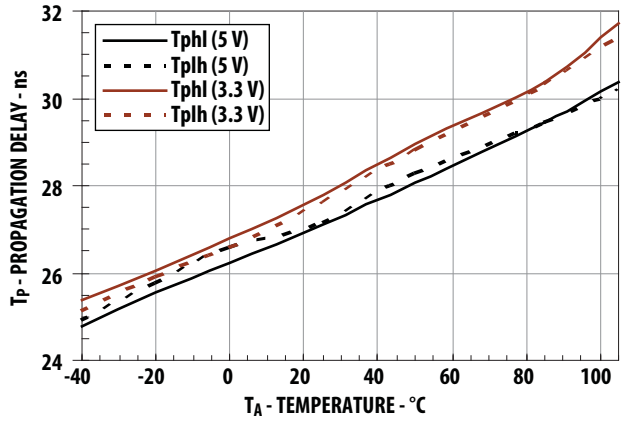


Figure 9. Typical Propagation Delay vs Temperature

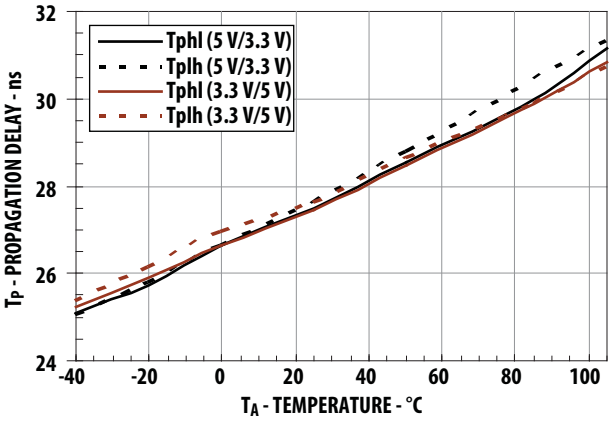


Figure 10. Typical Propagation Delay vs Temperature

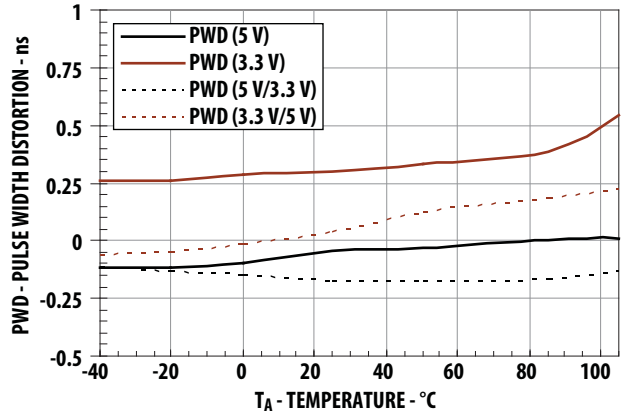


Figure 11. Typical Pulse Width Distortion vs Temperature

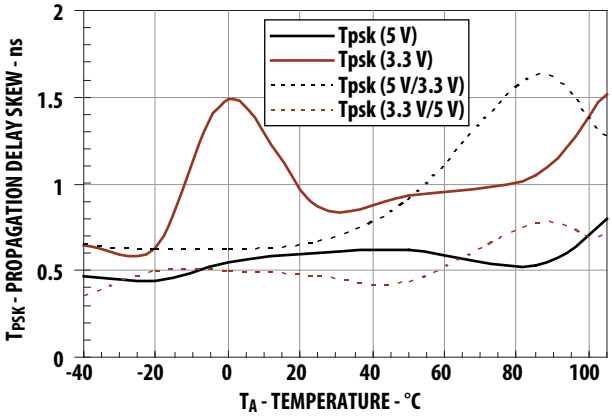


Figure 12. Typical Channel-Channel Delay Skew vs Temperature

Supply Current Consumption

It should be noted that the output supply current is specified under no load conditions. Additional supply current consumption from board or components loading can be computed based on:

$I_{DD} = CVF$

Where I_{DD} is the additional supply current consumption per output channel, C is the load capacitance, V is the supply voltage and F is the frequency of the signal

Bypassing and PC Board Layout

The ACML-7400 series digital isolators are extremely easy to use. No external interface circuitry is required because ACML-7400 series use high speed CMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in Figure 13, the only external components required for proper operation are two bypass capacitors for decoupling the power supply. Capacitor values should typically be 0.1 μF. For each capacitor, the total lead length between both ends of the capacitor and the power supply pins should be as short as possible.

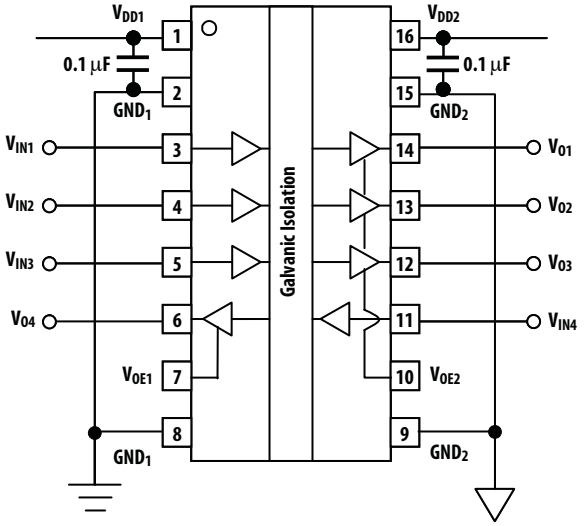


Figure 13. Typical Schematic of ACML-7410 on PC Board

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation Delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from a low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low. Please see Figure 14.

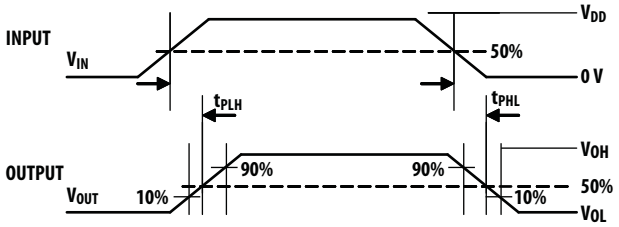


Figure 14. Threshold Levels of AC Parameters

Pulse-width distortion (PWD) is the difference between t_{PHL} and t_{PLH} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable. The PWD specification for ACML-7400 series is 3 ns maximum across recommended operating conditions.

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is sent through a group of isolators, differences in propagation delays will cause the data to arrive at the outputs of the isolators at different times. If this difference in propagation delay is large enough it will determine the maximum rate at which parallel data can be sent through the isolators.

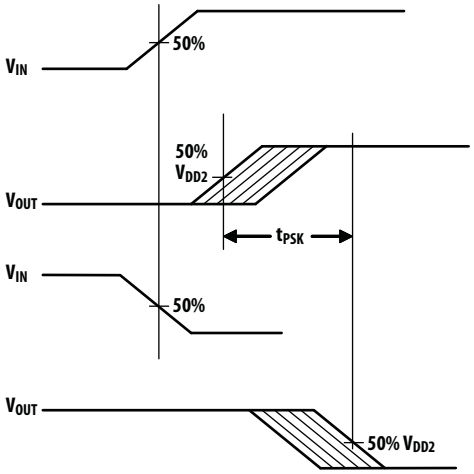


Figure 15. Illustration of T_{PSK}

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL} for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 15, if the inputs of a group of isolators are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL} and the longest propagation delay, either t_{PLH} and t_{PHL}.

The ACML-7400 series isolators offer the advantage of guaranteed specifications for propagation delays, pulse-width distortion, and propagation delay skew over the recommended temperature and power supply ranges.

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