ECMF02-2HSMX6

ESD protected common mode filter for USB3.0 interface

Features
- High common mode attenuation:
  - -10 dB @ 300 MHz
  - -20 dB @ 2.4 and 5 GHz
  - -15 dB from 500 MHz to 6 GHz
- Compliant with USB3.0 eye diagram
- Small and thin package 1.5 x 1.7 x 0.5 mm
- RoHS compliant.
- High reduction of parasitic elements through integration.
- ESD protection compliant with IEC 61000-4-2 level 4 standards (8 kV contact)

Benefits
- Suppress the common mode noise but keep signal integrity
- Low PCB space consumption.
- Save components count
- Make the application robust against ESD strikes from external environment

Description
The ECMF02-2HSMX6 is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like the USB3.0 transceiver.

Applications
Consumer and computer electronics featuring USB3.0 such as:
- Personal computer
- Notebook
- Tablet
- Set-top boxes
- PC graphic cards
- Telecom application

Figure 1. Pin out, top view

µQFN-6L 1.7 x 1.5 mm
1 Functional description

The ECMF02-2HSMX6 is an ESD protected common mode filter especially designed for USB3.0 Tx/Rx differential pair, for host and device. The USB3.0 is actually made of 3 differential pairs. The first differential pair supports the high speed USB mode (also called USB2.0 mode). The 2 other differential pairs are used to support the super speed USB mode in full duplex. Bit rate on super speed USB can reach 5 Gbps. The ECMF02-2HSMX6 is able to filter the common mode noise from 300 MHz to 6 GHz, helping to make the application compliant with the electromagnetic interference emission standard such as CISPR22 or FCC part 15, or EN55022 and avoiding antenna desense on mobile phones, WiFi/Bluetooth, GPS/GNSS frequencies. At the same time, the ECMF02-2HSMX6 keeps the high speed signal integrity and provides an efficient ESD protection.

Figure 2. Functional diagram

A typical application diagram is shown in Figure 3. ST offers a global approach to USB3.0 interface by providing a comprehensive range of dedicated products.

Figure 3. Typical application diagram
2 Electrical Characteristics

Table 1. Absolute maximum ratings (limiting values)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{PP}$</td>
<td>ESD discharge (pins 1 and 2)</td>
<td>Contact discharge</td>
<td>±8</td>
<td>kV</td>
</tr>
<tr>
<td></td>
<td>IEC 61000-4-2 level 4</td>
<td>Air discharge</td>
<td>±15</td>
<td>kV</td>
</tr>
<tr>
<td>$I_{DC}$</td>
<td>Maximum DC current</td>
<td></td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>$T_{OP}$</td>
<td>Operating temperature range</td>
<td></td>
<td>-40 to 85</td>
<td>°C</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Maximum junction temperature</td>
<td></td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage temperature range</td>
<td></td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Figure 4. Electrical characteristics (definitions)

Table 2. Electrical characteristics ($T_{amb} = 25$ °C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BR}$</td>
<td>Breakdown voltage</td>
<td>$I_R = 1$ mA</td>
<td>6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{RM}$</td>
<td>Reverse leakage</td>
<td>$V_{RM} = 3$ V</td>
<td></td>
<td>100</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$R_{DC}$</td>
<td>DC serial resistance</td>
<td></td>
<td>7</td>
<td>9</td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>
Figure 5 shows that USB3.0 devices and cables can interfere with radio frequency devices operating between 700 MHz and 5 GHz.

**Figure 5. USB3.0 frequency radiation measured with current loop**

**Figure 6. Differential attenuation versus frequency**

F₀ @-3 dB = 3.2 GHz
**Figure 7. Common mode attenuation versus frequency**

Note: STMicroelectronics has defined the USB3.0 SCC21 template to prevent antenna desense between 700 MHz and 5 GHz.

**Figure 8. Return loss versus frequency (Z_{COM} = 50 \, \Omega \cdot SDD11)**

Note: STMicroelectronics has defined the USB3.0 SCC21 template to prevent antenna desense between 700 MHz and 5 GHz.
Figure 9. Return loss versus frequency ($Z_{\text{COM}} = 50 \, \Omega$ - SDD22)
Figure 10. Typical ESD response to IEC 61000-4-2 +8kV contact

Figure 11. Typical ESD response to IEC 61000-4-2 -8kV contact
Figure 12. USB2.0 (480 Mbps) eye diagram without device

Figure 13. USB2.0 (480 Mbps) eye diagram with device

Figure 14. USB3.0 (5 Gbps) eye diagram without device

Figure 15. USB3.0 (5 Gbps) eye diagram with device

Figure 16. USB3.1 (10 Gbps) eye diagram without device

Figure 17. USB3.1 (10 Gbps) eye diagram with device
Figure 18. MHL (4.5 Gbps) eye diagram without device

Figure 19. MHL (4.5 Gbps) eye diagram with device

Figure 20. MHL (6 Gbps) eye diagram without device

Figure 21. MHL (6 Gbps) eye diagram with device

Figure 22. Display Port HBR2 (5.4 Gbps) eye diagram without device

Figure 23. Display Port HBR2 (5.4 Gbps) eye diagram with device
3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 24. μQFN-6L dimension definitions

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Dimensions</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Millimeters</td>
</tr>
<tr>
<td>A</td>
<td>0.45</td>
</tr>
<tr>
<td>A1</td>
<td>0.00</td>
</tr>
<tr>
<td>b</td>
<td>0.15</td>
</tr>
<tr>
<td>D</td>
<td>1.55</td>
</tr>
<tr>
<td>E</td>
<td>1.30</td>
</tr>
<tr>
<td>e</td>
<td>0.45</td>
</tr>
<tr>
<td>L1</td>
<td>0.35</td>
</tr>
<tr>
<td>L2</td>
<td>0.65</td>
</tr>
</tbody>
</table>
Figure 25. Footprint, dimensions in mm (inches)

- 0.25 (0.0098)
- 0.50 (0.0197)
- 0.30 (0.0118)
- 0.95 (0.0374)
- 0.65 (0.0256)

Dot identifying Pin A1 location

User direction of unreeling

Figure 26. Marking

- Dot, xx = marking
- z = manufacturing location
- yww = datecode
  - (y = year
  - ww = week)

Figure 27. Tape and reel specifications

All dimensions are typical values in mm

User direction of unreeling
4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

   Figure 28. Stencil opening dimensions

   b) General design rule
   - Stencil thickness (T) = 75 ~ 125 µm
   - Aspect Ratio = \( \frac{W}{T} \geq 1,5 \)
   - Aspect Area = \( \frac{L \times W}{2T(L + W)} \geq 0,66 \)

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

4.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.
4.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.
4.5 **Reflow profile**

Figure 30. ST ECOPACK® recommended soldering reflow profile for PCB mounting

Note: Minimize air convection currents in the reflow oven to avoid component movement.

4.6 **PCB layout recommendation**

Figure 31. PCB footprint recommendation

Zdiff according to the application

Via to GND plane
5 Ordering information

Figure 32. Ordering information scheme

Table 4. Ordering information

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking</th>
<th>Package</th>
<th>Weight</th>
<th>Base qty</th>
<th>Delivery mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECMF02-2HSMX6</td>
<td>KR</td>
<td>µQFN-6L</td>
<td>3.4 mg</td>
<td>3000</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

6 Revision history

Table 5. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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</thead>
<tbody>
<tr>
<td>13-Nov-2013</td>
<td>1</td>
<td>Initial release.</td>
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