

FEATURES

- DC to 11.3 Gbps per port, NRZ data rate**
- Multitime constant, programmable receive equalization**
 - Compensates 25 inches of FR408 at 10.3125 Gbps
 - Compensates 15 inches of FR408 at 11.3 Gbps
- 6-tap programmable transmit feedforward equalization (FFE)**
 - Compensates 15 inches of FR408 at 10.3125 Gbps
 - Compensates 10 inches of FR408 at 11.3 Gbps
- Low power**
 - 150 mW per channel at 2.5 V (outputs enabled)
- 12 × 12, fully differential, nonblocking array**
- Double rank connection programming**
- 2-pin selectable connection maps**
- Per lane lost of signal (LOS) detection**
- Flexible output termination supply range (1.8 V to 3.3 V)**
- DC- or ac-coupled differential CML inputs and outputs**
- Programmable CML output levels**
- Load from EEPROM for automatic power-on ready operation**
- Per lane input and output P/N pair inversion for routing ease**
- 50 Ω on-chip input/output termination**
- Supports 64-bit/66-bit, scrambled or not coded NRZ data up to 11.3 Gbps**
- Serial (I²C or SPI slave) control interface**
- 88-lead LFCSP, 12 mm × 12 mm, Pb-free package**
- −40°C to +85°C operating temperature range**

APPLICATIONS

- Fiber optic network switching
- 10 Gigabit Ethernet over backplane 10GBASE-KR 802.3ap
- XLAUI/CAUI (802.3ba)
- SONET OC-192/STM-64x
- 1x, 2x, 4x, 8x, and 10x Fibre Channel

GENERAL DESCRIPTION

The **ADN4612** is a 12 × 12 asynchronous, protocol agnostic, digital crosspoint switch with 12 differential PECL-/CML-compatible inputs and 12 differential CML outputs.

The **ADN4612** is optimized for nonreturn-to-zero (NRZ) signaling with data rates of up to 11.3 Gbps per port. Each port provides programmable input equalization, loss of signal (LOS) detection, programmable output swing, and output preemphasis/deemphasis.

FUNCTIONAL BLOCK DIAGRAM

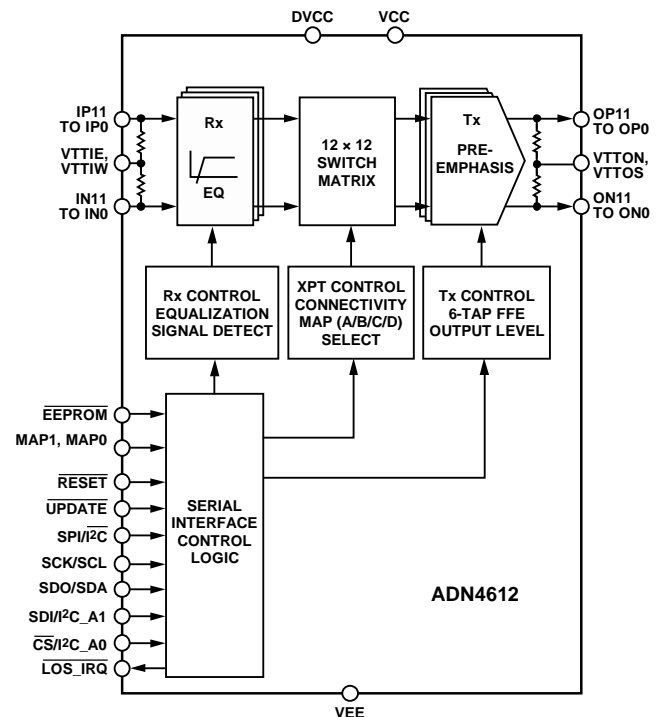


Figure 1.

The **ADN4612** nonblocking switch core implements a 12 × 12 crossbar and supports independent channel switching through the serial control interface. The **ADN4612** has low latency and very low channel-to-channel skew.

The **ADN4612** is packaged in an 88-lead LFCSP package and operates from −40°C to +85°C.

TABLE OF CONTENTS

| | | | |
|---|----|--|----|
| Features | 1 | Register Descriptions | 47 |
| Applications | 1 | Software Reset Register | 47 |
| Functional Block Diagram | 1 | Tx Enable Control Registers | 47 |
| General Description | 1 | Tx Reference Enable Register | 48 |
| Revision History | 3 | Squelch Control Register | 48 |
| Specifications | 4 | Rx and Tx Swap Sign Registers | 48 |
| Input/Output Specifications | 4 | XPT Broadcast Lane Number Register | 50 |
| Power Supply and Thermal Specifications | 5 | Tx 0 Driver Control Registers | 50 |
| Electrical Specifications—Control Logic Pins | 6 | Tx 0 Driver Enable Registers | 52 |
| I ² C Master and Slave Timing Specifications | 6 | Tx 0 Driver Resolution Registers | 53 |
| SPI Timing Specifications | 7 | Tx 1 Driver Control Registers | 53 |
| EEPROM Master I ² C Timing Specifications | 8 | Tx 1 Driver Enable Registers | 53 |
| RESET Timing Specifications | 9 | Tx 1 Driver Resolution Registers | 53 |
| Absolute Maximum Ratings | 10 | Tx 2 Driver Control Registers | 54 |
| Thermal Resistance | 10 | Tx 2 Driver Enable Registers | 54 |
| ESD Caution | 10 | Tx 2 Driver Resolution Registers | 54 |
| Pin Configuration and Function Descriptions | 11 | Tx 3 Driver Control Registers | 54 |
| Typical Performance Characteristics | 13 | Tx 3 Driver Enable Registers | 54 |
| Standard Test | 17 | Tx 3 Driver Resolution Registers | 54 |
| Equalization Test | 18 | Tx 4 Driver Control Registers | 54 |
| Preemphasis Test | 20 | Tx 4 Driver Enable Registers | 54 |
| Test Circuits | 22 | Tx 4 Driver Resolution Registers | 54 |
| Theory of Operation | 23 | Tx 5 Driver Control Registers | 55 |
| Introduction | 23 | Tx 5 Driver Enable Registers | 55 |
| Receivers | 24 | Tx 5 Driver Resolution Registers | 55 |
| Switch Core | 26 | Tx 6 Driver Control Registers | 55 |
| Transmitters | 27 | Tx 6 Driver Enable Registers | 55 |
| Preemphasis/Deemphasis Support for Legacy Rates | 33 | Tx 6 Driver Resolution Registers | 55 |
| Load from Memory | 34 | Tx 7 Driver Control Registers | 55 |
| I ² C Serial Control Interface | 37 | Tx 7 Driver Enable Registers | 55 |
| I ² C Data Write | 37 | Tx 7 Driver Resolution Registers | 55 |
| I ² C Data Read | 38 | Tx 8 Driver Control Registers | 56 |
| SPI Serial Control Interface | 39 | Tx 8 Driver Enable Registers | 56 |
| Write Operation | 39 | Tx 8 Driver Resolution Registers | 56 |
| Read Operation | 39 | Tx 9 Driver Control Registers | 56 |
| Applications Information | 40 | Tx 9 Driver Enable Registers | 56 |
| Applications Circuit | 41 | Tx 9 Driver Resolution Registers | 56 |
| Power Consumption | 41 | Tx 10 Driver Control Registers | 56 |
| Printed Circuit Board (PCB) Layout Guidelines | 42 | Tx 10 Driver Enable Registers | 56 |
| Register Map | 44 | Tx 10 Driver Resolution Registers | 56 |

| | | | |
|---|----|--|----|
| Tx 11 Driver Control Registers | 57 | Rx 11 to Rx 6 LOS Sticky Status Register..... | 66 |
| Tx 11 Driver Enable Registers | 57 | Rx 11 to Rx 6 LOS Assert and Deassert Level Control Register | 66 |
| Tx 11 Driver Resolution Registers | 57 | Rx 11 to Rx 6 LOS IRQ Enable Register | 67 |
| Rx 0 to Rx 5 Active and Passive Equalization Control Registers | 57 | Rx Offset Calibration Control Registers | 67 |
| Rx 5 to Rx 0 Enable Control Register | 59 | XPT Map A Tx Lane Select Registers..... | 68 |
| Rx 5 to Rx 0 Equalizer Enable Control Register | 59 | XPT Map B Tx Lane Select Registers | 69 |
| Rx 5 to Rx 0 LOS Enable Control Register | 59 | XPT Map C Tx Lane Select Registers..... | 70 |
| Rx 5 to Rx 0 LOS Time Control Registers | 60 | XPT Map D Tx Lane Select Registers | 71 |
| Rx 5 to Rx 0 LOS Status Register..... | 61 | XPT Map Tx Lane Status Registers | 73 |
| Rx 5 to Rx 0 LOS Sticky Status Register | 61 | Boot from EEPROM Control Register..... | 74 |
| Rx 5 to Rx 0 LOS Assert and Deassert Level Control Register | 61 | XPT Table Selection Control Register..... | 74 |
| Rx 5 to Rx 0 LOS IRQ Enable Register..... | 62 | Update XPT Table Register..... | 74 |
| Rx 6 to Rx 11 Active and Passive Equalization Control Registers | 62 | EEPROM Checksum Register | 75 |
| Rx 11 to Rx 6 Enable Control Register..... | 63 | EEPROM Status Register | 75 |
| Rx 11 to Rx 6 Equalizer Enable Control Register | 64 | Revision ID Register | 75 |
| Rx 11 to Rx 6 LOS Enable Control Register | 64 | Chip ID Register | 75 |
| Rx 11 to Rx 6 LOS Time Control Registers | 65 | Packaging and Ordering Information | 76 |
| Rx 11 to Rx 6 LOS Status Register | 66 | Outline Dimensions | 76 |
| | | Ordering Guide | 76 |

REVISION HISTORY

10/13—Revision A: Initial Version

SPECIFICATIONS

$V_{CC} = V_{TTO}^1 = 2.5\text{ V}$, $V_{TTI}^2 = V_{IP8} = DV_{CC} = 1.8\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 50\ \Omega$, data rate = 11.3 Gbps, data pattern = PRBS 15, ac-coupled inputs and outputs, differential input swing = 800 mV p-p, EQ setting = 0x12,³ PE boost = 1.94 dB,⁴ unless otherwise noted.

INPUT/OUTPUT SPECIFICATIONS

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|--|------|----------------|------|-------------|
| DYNAMIC PERFORMANCE | | | | | |
| Data Rate (NRZ) | | DC | | 11.3 | Gbps |
| Deterministic Jitter (No Channel) | Data rate = 10.3125 Gbps | | 11 | | ps p-p |
| | Data rate = 11.3 Gbps | | 14 | | ps p-p |
| Random Jitter (No Channel) | | | 0.5 | | ps rms |
| Residual Deterministic Jitter with Receive Equalization | Input trace = 25-inch FR408, data rate = 10.3125 Gbps, EQ setting = 0x94 | | 0.25 | | UI |
| | Input trace = 15-inch FR408, data rate = 11.3 Gbps, EQ setting = 0x72 | | 0.25 | | UI |
| Residual Deterministic Jitter with Transmit Preemphasis | Output trace = 15-inch FR408, data rate = 10.3125 Gbps, PE boost = 5.46 dB | | 0.24 | | UI |
| | Output trace = 10-inch FR408, data rate = 11.3 Gbps, PE boost = 6.02 dB | | 0.31 | | UI |
| Propagation Delay | 50% input to 50% output (maximum EQ) | | 520 | | ps |
| Lane-to-Lane Skew | Signal path and switch architecture is balanced and symmetric (maximum EQ) | | ±40 | | ps |
| Switching Time | 50% logic switching to 50% output data ⁵ | | 10 | | ns |
| Output Rise/Fall Time | 20% to 80%, test pattern = 000000011111111 | | 44 | | ps |
| INPUT CHARACTERISTICS | | | | | |
| Differential Input Voltage Swing | $V_{ICM}^6 = 1.8\text{ V}$, $V_{CC} = V_{MIN}$ to V_{MAX} , $T_A = T_{MIN}$ to T_{MAX} | <200 | | 2000 | mV p-p diff |
| Input Voltage Range | Single-ended absolute voltage level, V_{IL} minimum | | 1.0 | | V |
| | Single-ended absolute voltage level, V_{IH} maximum | | $V_{CC} + 0.3$ | | V |
| Differential Input Return Loss (SDD11) | At 2.125 GHz | | -24 | | dB |
| | At 5.5 GHz | | -10 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Differential; PE boost = 0 dB; default output level, at dc | 660 | 780 | 910 | mV p-p diff |
| Output Voltage Range | Single-ended absolute voltage level, V_{OL} | | $V_{CC} - 1.2$ | | V |
| | Single-ended absolute voltage level, V_{OH} | | V_{TTO}^1 | | V |
| Output Voltage Setting Resolution | Differential absolute voltage level minimum step size, Tx driver resolution bits = 11b (divide by 8) | | 12.5 | | mV p-p diff |
| Per Port Output Current | PE boost = 0 dB, default output level | | 16 | | mA |
| Differential Output Return Loss (SDD22) | At 2.125 GHz | | -20 | | dB |
| | At 5.5 GHz | | -9 | | dB |
| TERMINATION CHARACTERISTICS | | | | | |
| Resistance | Differential, $V_{CC} = V_{MIN}$ to V_{MAX} , $T_A = T_{MIN}$ to T_{MAX} | 90 | 100 | 110 | Ω |
| LOS CHARACTERISTICS | | | | | |
| Assert Level | Programmable; LOS_ASSERT = 0x2 | | 74 | | mV p-p diff |
| Deassert Level | Programmable; LOS_DEASSERT = 0x6 | | 133 | | mV p-p diff |
| LOS-to-Output Squelch | Time from active signal to idle | | 1.1 | | ns |
| LOS-to-Output Enable | Time from idle to active signal | | 31 | | ns |

¹ V_{TTO} is a generic variable that describes both V_{TTON} and V_{TTOS} . V_{TTON} and V_{TTOS} are independent voltages that are not required to equal each other.

² V_{TTI} is a generic variable that describes both V_{TTIE} and V_{TTIW} . V_{TTIE} and V_{TTIW} are independent voltages that are not required to equal each other.

³ Default EQ setting is used to compensate for loss of test fixture.

⁴ Default PE setting is used to compensate for loss of test fixture.

⁵ 50% logic level high-to-low transition of the UPDATE toggle pin or 50% logic level transition of the MAP1 and MAP0 pins while the UPDATE pin is held at logic low.

⁶ V_{ICM} is the input common-mode voltage.

POWER SUPPLY AND THERMAL SPECIFICATIONS

Table 2.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------------------|---|------------------|------|-------------------|--------|
| POWER SUPPLY OPERATING RANGE | $V_{EE} = 0\text{ V}$ | | | | |
| V_{CC} | | 2.25 | 2.5 | 2.75 | V |
| DV_{CC} | | 1.6 | 1.8 | 2.0 | V |
| V_{CC1P8} | | 1.6 | 1.8 | 2.0 | V |
| V_{TT1}^1 | | 1.6 | 1.8 | 2.75 ² | V |
| V_{TTO}^3 | | 1.6 ⁴ | 2.5 | 3.6 | V |
| POWER SUPPLY NOISE TOLERANCE | | | | | |
| V_{CC} | 10 Hz to 6.25 GHz | | 100 | | mV p-p |
| DV_{CC} | 10 Hz to 100 MHz | | 100 | | mV p-p |
| V_{CC1P8} | 10 Hz to 100 MHz | | 25 | | mV p-p |
| V_{TT1}^1 | 10 Hz to 6.25 GHz | | 100 | | mV p-p |
| V_{TTO}^3 | 10 Hz to 6.25 GHz | | 100 | | mV p-p |
| SUPPLY CURRENT | | | | | |
| I_{CC} | | | | | |
| $V_{CC} = 2.5\text{ V}$ | Default, all outputs disabled | | 120 | 140 | mA |
| | All outputs and main tap enabled, single driver (D0) enabled | | 391 | 430 | mA |
| | All outputs and main tap enabled, two drivers (D0, D1) enabled | | 537 | 590 | mA |
| | All outputs and main tap enabled, three drivers (D0 to D2) enabled | | 684 | 760 | mA |
| | All outputs and main tap and first post tap (D0 to D3) enabled | | 829 | 920 | mA |
| | All outputs, precursor, main tap, and first post tap (PC, D0 to D3) enabled | | 944 | 1070 | mA |
| I_{TTO}^5 | | | | | |
| $V_{TTO} = 2.5\text{ V}$ | Default, all outputs disabled | | 0 | <1 | mA |
| | All outputs enabled, 8 mA output current per lane | | 96 | 106 | mA |
| | All outputs enabled, 16 mA output current per lane | | 192 | 206 | mA |
| | All outputs enabled, 24 mA output current per lane | | 287 | 314 | mA |
| | All outputs enabled, 32 mA output current per lane | | 384 | 416 | mA |
| I_{TT1}^6 | | | 0 | | mA |
| I_{DVCC} | | | 8 | 12 | mA |
| I_{VCC1P8} | Default, all outputs disabled | | 7 | 8 | mA |
| | All outputs main tap enabled | | 40 | 43 | mA |
| THERMAL CHARACTERISTICS | | | | | |
| Operating Temperature Range | | -40 | | +85 | °C |
| θ_{JA} | Still air; JEDEC 4-layer test board, exposed pad soldered | | 24.0 | | °C/W |
| θ_{JC} | Still air; thermal resistance through exposed pad | | 1.7 | | °C/W |
| Maximum Junction Temperature | | | | 125 | °C |

¹ V_{TT1} is a generic variable that describes both V_{TTIE} and V_{TTIW} . V_{TTIE} and V_{TTIW} are independent voltages that are not required to equal each other.

² It is recommended that $V_{TT1} \leq V_{CC}$ to meet the input compliance.

³ V_{TTO} is a generic variable that describes both V_{TTON} and V_{TTOS} . V_{TTON} and V_{TTOS} are independent voltages that are not required to equal each other.

⁴ The single-ended absolute voltage level, V_{OL} , must be $\leq V_{CC} - 1.2\text{ V}$ when operating V_{TTO} at the minimum boundary of the supply range.

⁵ I_{TTO} is a generic variable that describes both I_{TTON} and I_{TTOS} . I_{TTON} and I_{TTOS} are independent currents that are not required to equal each other.

⁶ I_{TT1} is a generic variable that describes both I_{TTIE} and I_{TTIW} . I_{TTIE} and I_{TTIW} are independent currents that are not required to equal each other.

ELECTRICAL SPECIFICATIONS—CONTROL LOGIC PINS

Table 3.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|-----------------|---|------------------------|------------------|------------------------|------|
| I²C LOGIC CHARACTERISTICS | | | | | | |
| Input | | | | | | |
| High | V _{IH} | DV _{CC} = 1.8 V | 0.7 × DV _{CC} | | DV _{CC} | V |
| Low | V _{IL} | DV _{CC} = 1.8 V | V _{EE} | | 0.3 × DV _{CC} | V |
| Output | | | | | | |
| High | V _{OH} | I ² C only, 2 kΩ pull-up resistor to DV _{CC} I _{OH} = -1 mA | 0.8 × DV _{CC} | DV _{CC} | DV _{CC} | V |
| Low | V _{OL} | I _{OL} = +1 mA | V _{EE} | | 0.2 × DV _{CC} | V |

I²C MASTER AND SLAVE TIMING SPECIFICATIONS

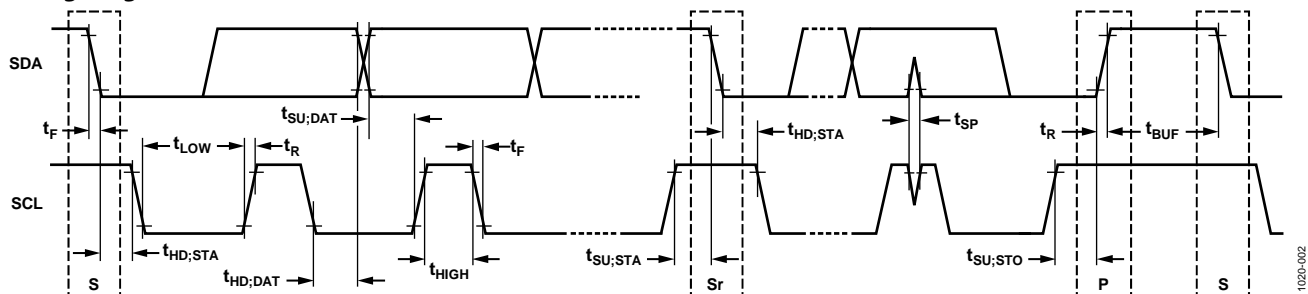
Table 4.

| Parameter ¹ | Symbol | Test Conditions/Comments | Min | Max | Unit |
|--|---------------------|--------------------------|-----|-----|------|
| SCL² CLOCK FREQUENCY | | | | | |
| Master Interface | f _{SCL} | Load from EEPROM only | 0 | 100 | kHz |
| Slave Interface | f _{SCL} | | 0 | 400 | kHz |
| START CONDITION | | | | | |
| Hold Time for a Start Condition | t _{HD;STA} | | 0.6 | | μs |
| Setup Time for a Repeated Start Condition | t _{SU;STA} | | 0.6 | | μs |
| SCL² CLOCK | | | | | |
| Low Period | t _{LOW} | | 1.3 | | μs |
| High Period | t _{HIGH} | | 0.6 | | μs |
| DATA (SDA³) | | | | | |
| Data Hold Time | t _{HD;DAT} | | 0 | | μs |
| Data Setup Time | t _{SU;DAT} | | 10 | | ns |
| SDA³ AND SCL² | | | | | |
| Rise Time | t _R | | 1 | 300 | ns |
| Fall Time | t _F | | 1 | 300 | ns |
| SETUP TIME FOR STOP CONDITION | | | | | |
| | t _{SU;STO} | | 0.6 | | μs |
| BUS TIME | | | | | |
| Bus Free Time Between a Stop Condition and a Start Condition | t _{BUF} | | 1 | | ns |
| Bus Idle Time After Reset | | | 10 | | ns |

¹ Detailed functionality of the I²C interface is described in the I²C Serial Control Interface section.

² SCL is the I²C serial clock function of the SCK/SCL pin.

³ SDA is the I²C serial data function of the SDO/SDA pin.

I²C Timing DiagramFigure 2. I²C Timing Diagram

11020-002

SPI TIMING SPECIFICATIONS

Table 5.

| Parameter ¹ | Symbol | Min | Max | Unit |
|---|-----------|-----|-----|------|
| SCK ² | | | | |
| Clock Frequency | f_{SCK} | 0 | 10 | MHz |
| SCK Pulse Width | | | | |
| High | t_2 | 40 | | ns |
| Low | t_3 | 40 | | ns |
| DATA (SDO ³ and SDI ⁴) | | | | |
| Data Access Time After SCK Falling Edge | t_4 | | 35 | ns |
| Data Setup Time Prior to SCK Rising Edge | t_5 | 20 | | ns |
| Data Hold Time After SCK Rising Edge | t_6 | 10 | | ns |
| \overline{CS} ⁵ | | | | |
| \overline{CS} to SCK Setup Time | t_1 | 10 | | ns |
| \overline{CS} to SCK Hold Time | t_7 | 10 | | ns |
| \overline{CS} to SDO High Impedance | t_8 | | 40 | ns |

¹ Detailed functionality of the SPI interface is described in the SPI Serial Control Interface section.

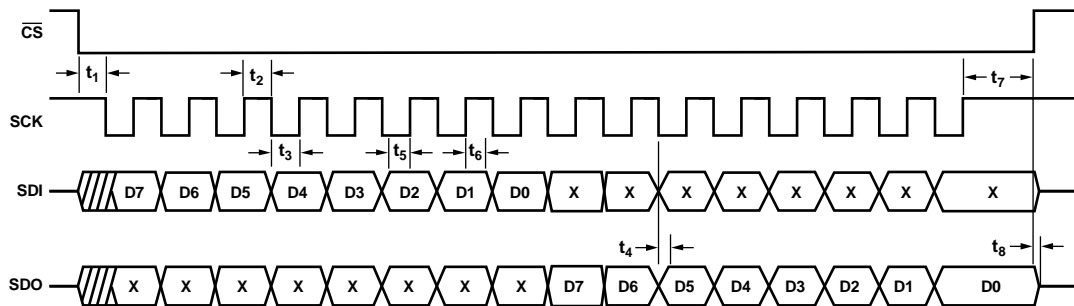
² SCK is the SPI serial clock function of the SCK/SCL pin.

³ SDO is the SPI serial data function of the SDO/SDA pin.

⁴ SDI is the SPI serial data function of the SDI/I²C_A1 pin.

⁵ \overline{CS} is the SPI chip select function of the \overline{CS}/I^2C_{A0} pin.

SPI Timing Diagram



NOTES

- SDI IS THE SPI SERIAL DATA FUNCTION OF THE SDI/I²C_A1 PIN.
- SDO IS THE SPI SERIAL DATA FUNCTION OF THE SDO/SDA PIN.

Figure 3. SPI Timing Diagram

11020-003

EEPROM MASTER I²C TIMING SPECIFICATIONS

Table 6.

| Parameter ¹ | Symbol | Typical | Unit |
|--|----------------|---------|------|
| EEPROM | | | |
| Load from EEPROM Timeout | | 2000 | μs |
| RESET to EEPROM Setup Time | t ₁ | 200 | μs |
| EEPROM Pulse Width | t ₂ | 2 | μs |
| START CONDITION | | | |
| EEPROM Low Transition to Start Condition | t ₃ | 3 | μs |
| STOP CONDITION | | | |
| Stop Condition to LOS_IRQ Low Transition | t ₄ | 10 | μs |
| LOS_IRQ | | | |
| LOS_IRQ Pulse Width | t ₅ | 2 | μs |

¹ Detailed functionality of this interface is described in the Load from Memory section.

EEPROM Timing Diagram

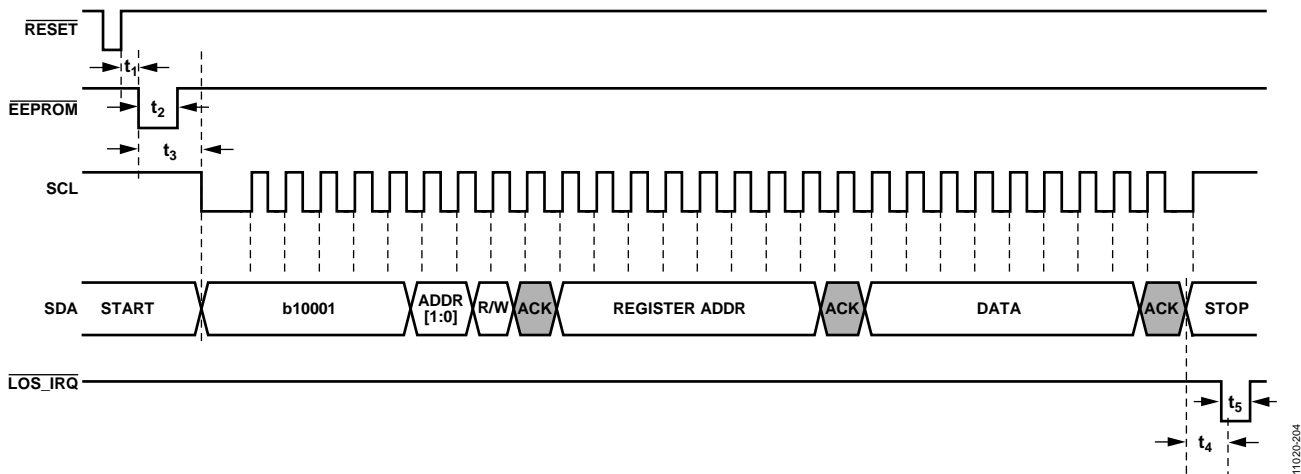


Figure 4. Load from EEPROM Timing Diagram

11020-204

RESET TIMING SPECIFICATIONS

Table 7.

| Parameter | Symbol | Min | Max | Unit |
|-------------|--------------------|-----|-----|---------------|
| RESET | | | | |
| Pulse Width | t_{RESET} | 100 | | μs |
| Hold Time | t_{HOLD} | 100 | | μs |

RESET Timing Diagram

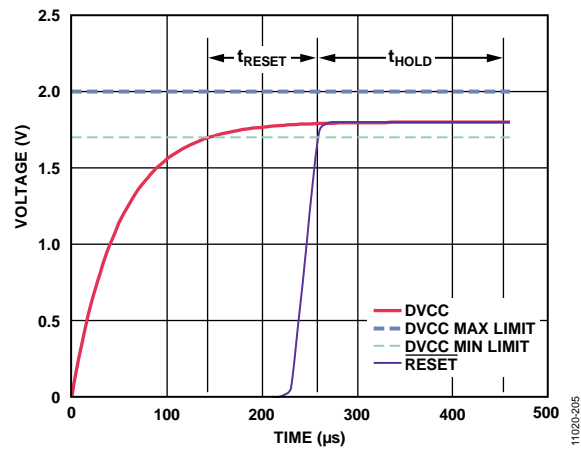


Figure 5. RESET Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 8.

| Parameter | Rating |
|---|---|
| VCC to VEE | 2.75 V |
| DVCC to VEE | 2.0 V |
| VTTIE, VTTIW | $V_{CC} + 0.6 V$ |
| VTON, VTOS | 3.6 V |
| Internal Power Dissipation ¹ | 4.9 W |
| Differential Input Voltage | 2.0 V |
| Logic Input Voltage | $V_{EE} - 0.3 V < V_{IN} < DV_{CC} + 0.6 V$ |
| Temperature | |
| Storage Temperature Range | -65°C to +125°C |
| Lead Temperature | 300°C |
| Junction Temperature | 125°C |

¹ Internal power dissipation is for the device in free air. $T_A = 27^\circ\text{C}$; $\theta_{JA} = 24.0^\circ\text{C/W}$ in still air.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified in still air using a JEDEC 4-layer test board with the exposed pad soldered. θ_{JC} is tested in still air with the thermal resistance through the exposed pad.

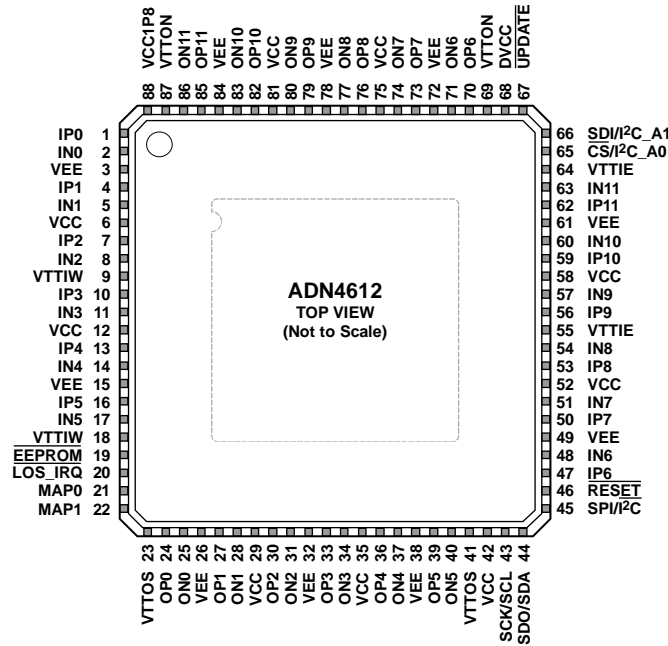
Table 9. Thermal Resistance

| Package Type | θ_{JA} | θ_{JC} | Unit |
|---------------|---------------|---------------|--------------------|
| 88-Lead LFCSP | 24.0 | 1.7 | $^\circ\text{C/W}$ |

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
 1. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE MUST BE ELECTRICALLY CONNECTED TO VEE.

Figure 6. Pin Configuration

Table 10. Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|---------------------------------------|-------------------------|---------|---|
| 6, 12, 29, 35, 42, 52, 58, 75, 81 | VCC | Power | Core Power Supplies. |
| 88 | VCC1P8 | Power | Analog 1.8 V Reference Supply. |
| 68 | DVCC | Power | Digital Power Supply. |
| 3, 15, 26, 32, 38, 49, 61, 72, 78, 84 | VEE | Power | Negative Supplies. |
| 9, 18 | VTTIW | Power | Westside Input Termination Supplies. |
| 55, 64 | VTTIE | Power | Eastside Input Termination Supplies. |
| 69, 87 | VTTON | Power | Northside Output Termination Supplies. |
| 23, 41 | VTTOS | Power | Southside Output Termination Supplies. |
| 19 | EEPROM | Control | Load from EEPROM (Active Low). |
| 20 | LOS_IRQ | Control | Loss of Signal Detect Interrupt Request Output (Active Low). |
| 21 | MAP0 | Control | Map Select LSB. |
| 22 | MAP1 | Control | Map Select MSB. |
| 43 | SCK/SCL | Control | SPI Serial Clock (SCK)/I ² C Serial Clock (SCL). This is a multifunction pin. |
| 44 | SDO/SDA | Control | SPI Serial Data Output (SDO)/I ² C Serial Data (SDA). This is a multifunction pin. |
| 45 | SPI/I ² C | Control | SPI Mode Select (SPI)/I ² C Mode Select (I ² C). This is a multifunction pin. |
| 46 | RESET | Control | Reset (Active Low). |
| 65 | CS/I ² C_A0 | Control | SPI Chip Select, Active Low (CS)/I ² C Address LSB (I ² C_A0). This is a multifunction pin. |
| 66 | SDI/I ² C_A1 | Control | SPI Serial Data Input (SDI)/I ² C Address MSB (I ² C_A1). This is a multifunction pin. |
| 67 | UPDATE | Control | Switch Configuration Update Strobe (Active Low). |
| 1 | IPO | I | High Speed Input. |
| 2 | INO | I | High Speed Input Complement. |
| 4 | IP1 | I | High Speed Input. |
| 5 | IN1 | I | High Speed Input Complement. |
| 7 | IP2 | I | High Speed Input. |
| 8 | IN2 | I | High Speed Input Complement. |
| 10 | IP3 | I | High Speed Input. |
| 11 | IN3 | I | High Speed Input Complement. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|------|--|
| 13 | IP4 | I | High Speed Input. |
| 14 | IN4 | I | High Speed Input Complement. |
| 16 | IP5 | I | High Speed Input. |
| 17 | IN5 | I | High Speed Input Complement. |
| 47 | IP6 | I | High Speed Input. |
| 48 | IN6 | I | High Speed Input Complement. |
| 50 | IP7 | I | High Speed Input. |
| 51 | IN7 | I | High Speed Input Complement. |
| 53 | IP8 | I | High Speed Input. |
| 54 | IN8 | I | High Speed Input Complement. |
| 56 | IP9 | I | High Speed Input. |
| 57 | IN9 | I | High Speed Input Complement. |
| 59 | IP10 | I | High Speed Input. |
| 60 | IN10 | I | High Speed Input Complement. |
| 62 | IP11 | I | High Speed Input. |
| 63 | IN11 | I | High Speed Input Complement. |
| 24 | OP0 | O | High Speed Output. |
| 25 | ON0 | O | High Speed Output Complement. |
| 27 | OP1 | O | High Speed Output. |
| 28 | ON1 | O | High Speed Output Complement. |
| 30 | OP2 | O | High Speed Output. |
| 31 | ON2 | O | High Speed Output Complement. |
| 33 | OP3 | O | High Speed Output. |
| 34 | ON3 | O | High Speed Output Complement. |
| 36 | OP4 | O | High Speed Output. |
| 37 | ON4 | O | High Speed Output Complement. |
| 39 | OP5 | O | High Speed Output. |
| 40 | ON5 | O | High Speed Output Complement. |
| 70 | OP6 | O | High Speed Output. |
| 71 | ON6 | O | High Speed Output Complement. |
| 73 | OP7 | O | High Speed Output. |
| 74 | ON7 | O | High Speed Output Complement. |
| 76 | OP8 | O | High Speed Output. |
| 77 | ON8 | O | High Speed Output Complement. |
| 79 | OP9 | O | High Speed Output. |
| 80 | ON9 | O | High Speed Output Complement. |
| 82 | OP10 | O | High Speed Output. |
| 83 | ON10 | O | High Speed Output Complement. |
| 85 | OP11 | O | High Speed Output. |
| 86 | ON11 | O | High Speed Output Complement. |
| | EP | | Exposed Pad. The exposed pad on the bottom of the package must be electrically connected to VEE. |

TYPICAL PERFORMANCE CHARACTERISTICS

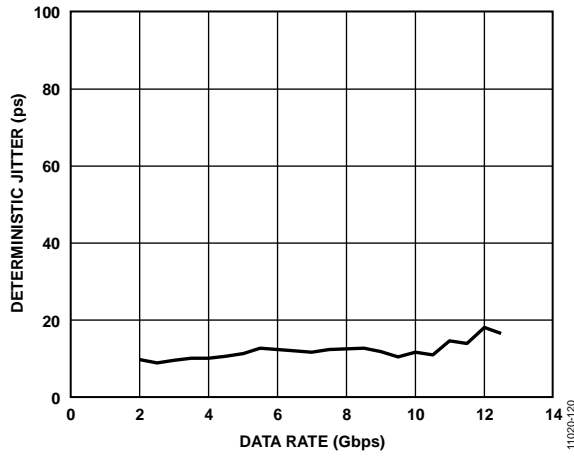


Figure 7. Deterministic Jitter vs. Data Rate

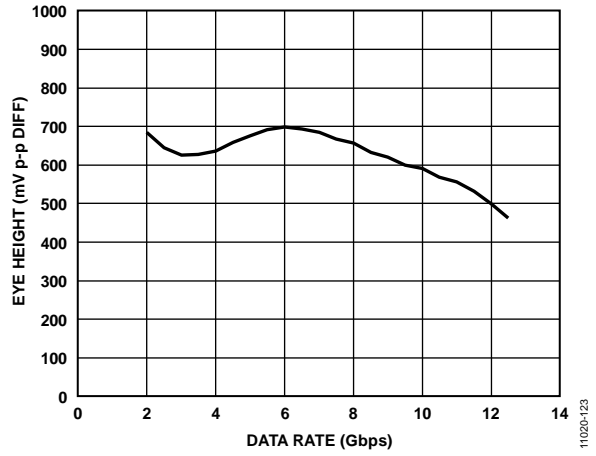


Figure 10. Eye Height vs. Data Rate

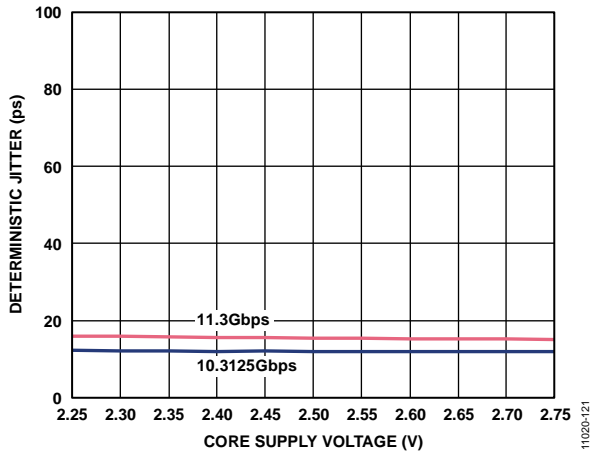


Figure 8. Deterministic Jitter vs. Core Supply Voltage (V_{CC})

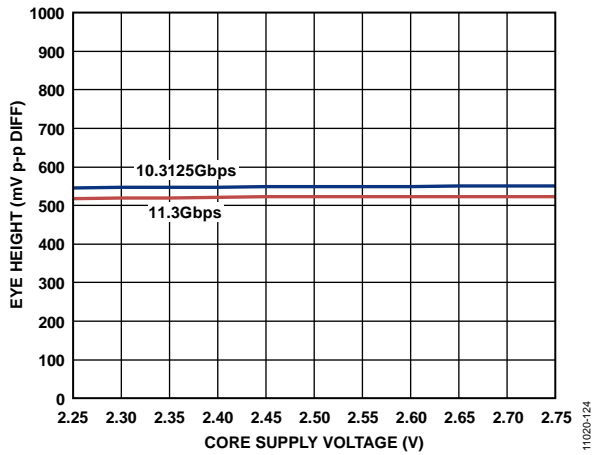


Figure 11. Eye Height vs. Core Supply Voltage (V_{CC})

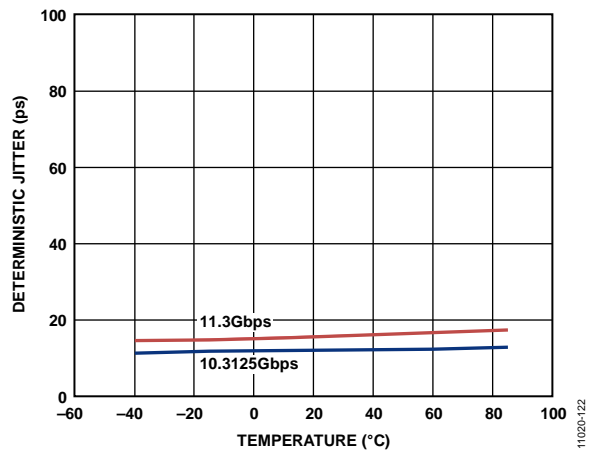


Figure 9. Deterministic Jitter vs. Temperature

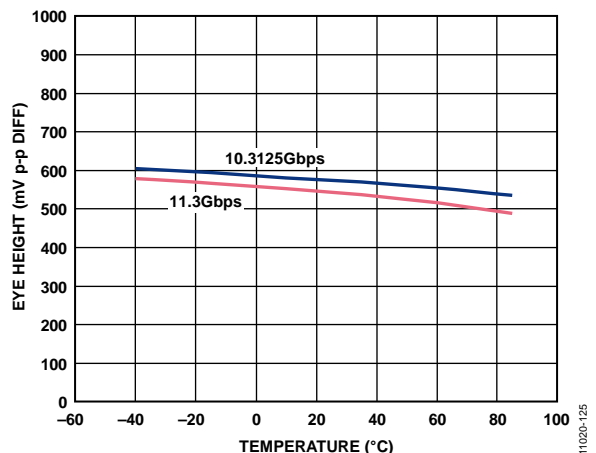


Figure 12. Eye Height vs. Temperature

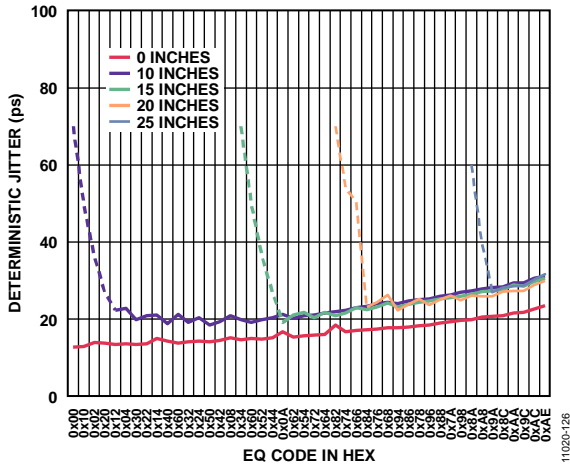


Figure 13. Deterministic Jitter vs. EQ Code in Hexadecimal for Various Input FR408 Channel Lengths; Data Rate = 10.3125 Gbps

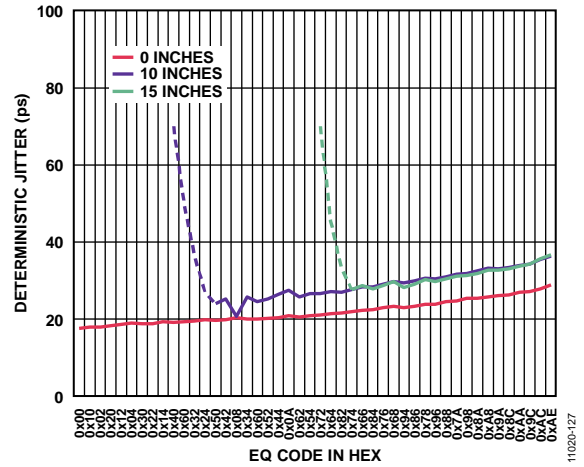


Figure 16. Deterministic Jitter vs. EQ Code in Hexadecimal for Various Input FR408 Channel Lengths; Data Rate = 11.3 Gbps

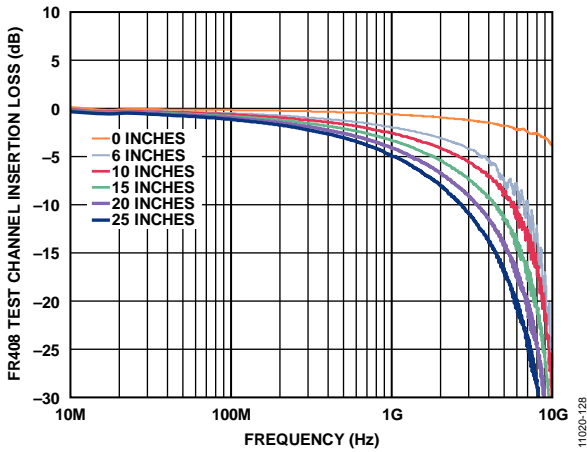


Figure 14. S21 Test Traces

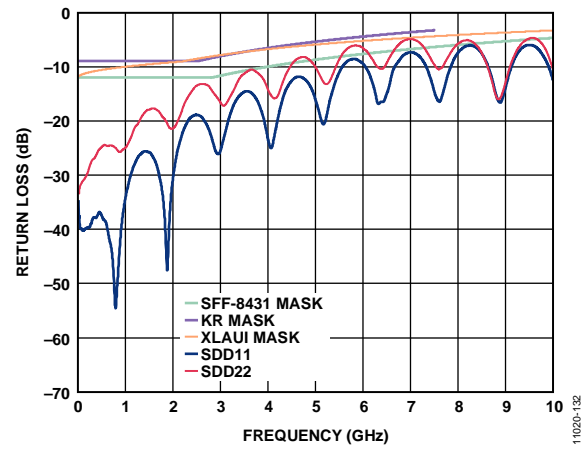


Figure 17. Return Loss (SDD11/SDD22)

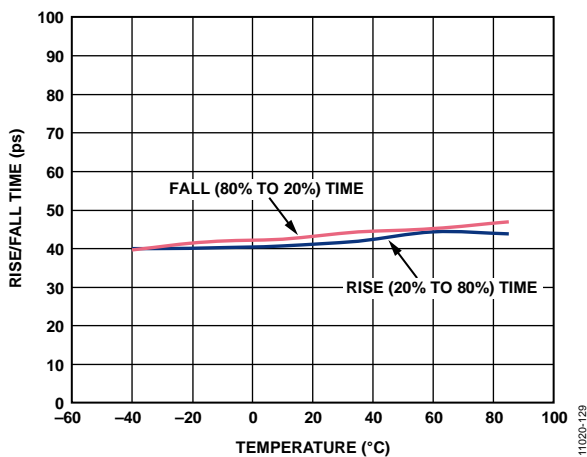


Figure 15. Rise/Fall Time vs. Temperature

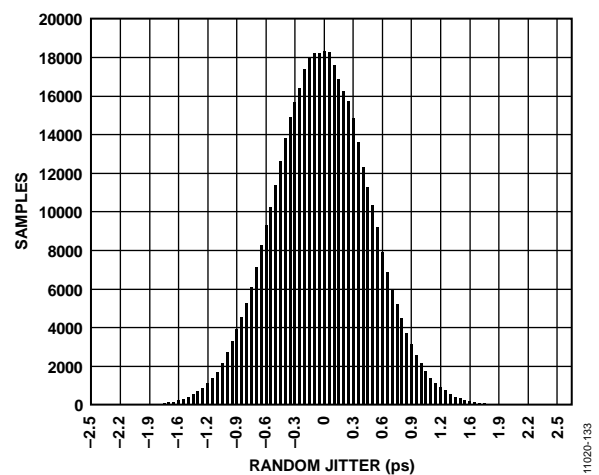


Figure 18. Random Jitter Histogram

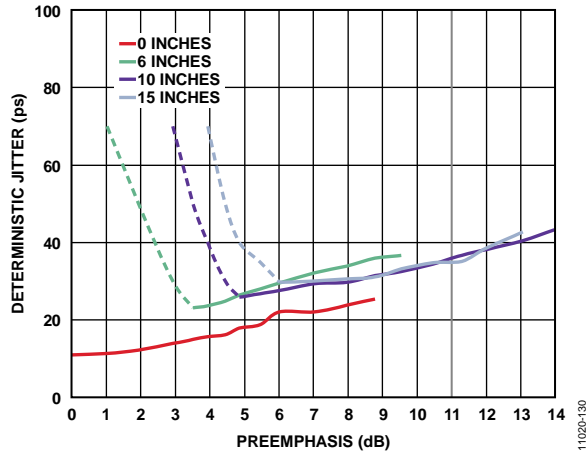


Figure 19. Deterministic Jitter vs. Preemphasis for Various Output FR408 Channel Lengths; Data Rate = 10.3125 Gbps

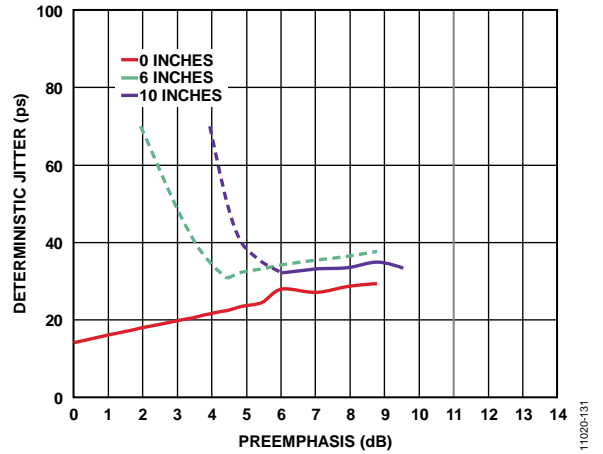


Figure 22. Deterministic Jitter vs. Preemphasis for Various Output FR408 Channel Lengths; Data Rate = 11.3 Gbps

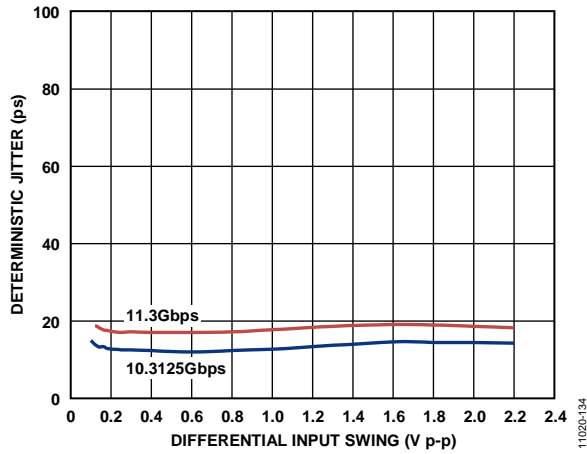


Figure 20. Deterministic Jitter vs. Differential Input Swing

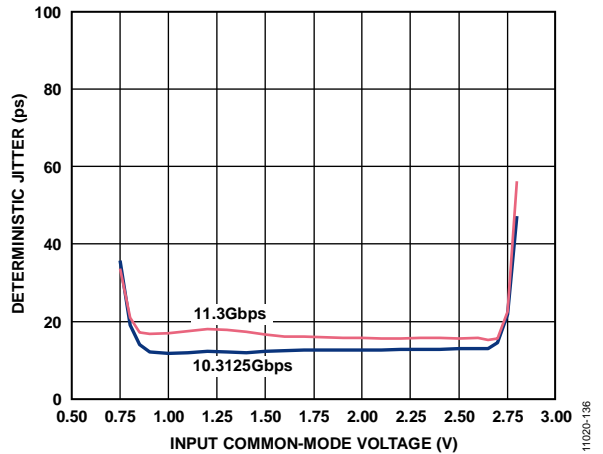


Figure 23. Deterministic Jitter vs. Input Common-Mode Voltage

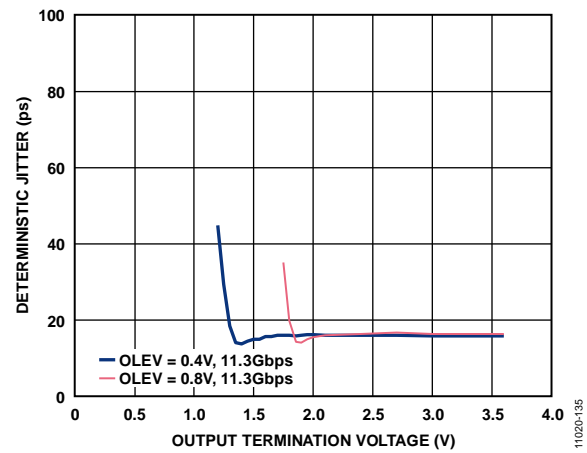


Figure 21. Deterministic Jitter vs. Output Termination Voltage (V_{T0})

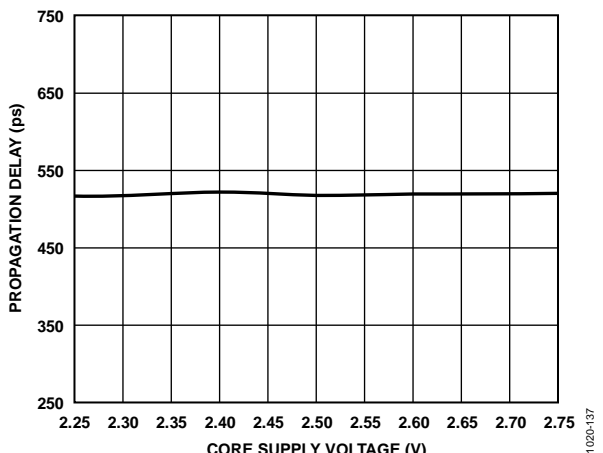


Figure 24. Propagation Delay vs. Core Supply Voltage (V_{cc})

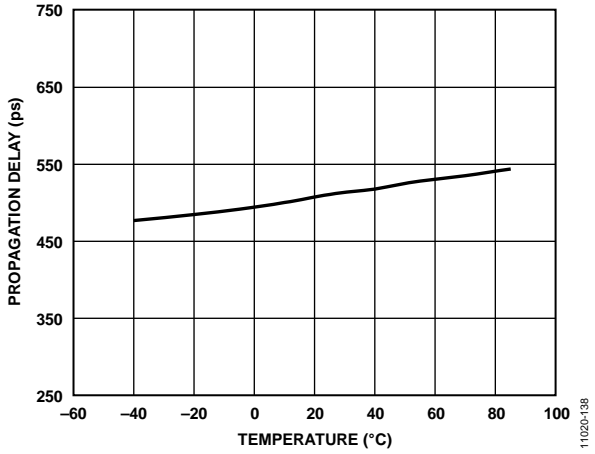


Figure 25. Propagation Delay vs. Temperature

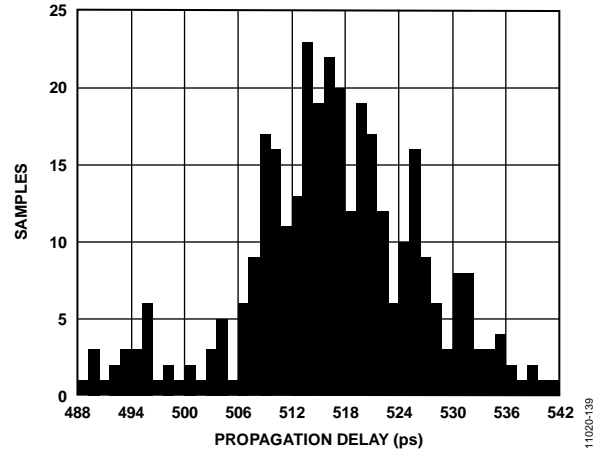


Figure 26. Propagation Delay Histogram

STANDARD TEST

$V_{CC} = V_{TTO} = 2.5\text{ V}$, $V_{TTI} = V_{CCIP8} = DV_{CC} = 1.8\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 50\ \Omega$, data rate = 11.3 Gbps, data pattern = PRBS 15, ac-coupled inputs and outputs, differential input swing = 800 mV p-p, EQ setting = 0x12 (note that the default EQ setting is used to compensate for the loss of the test fixture), PE boost = 1.94 dB (note that the default PE settings are used to compensate for the loss of the test fixture), unless otherwise noted.

For the standard test circuit used for Figure 27 to Figure 30, see Figure 47.

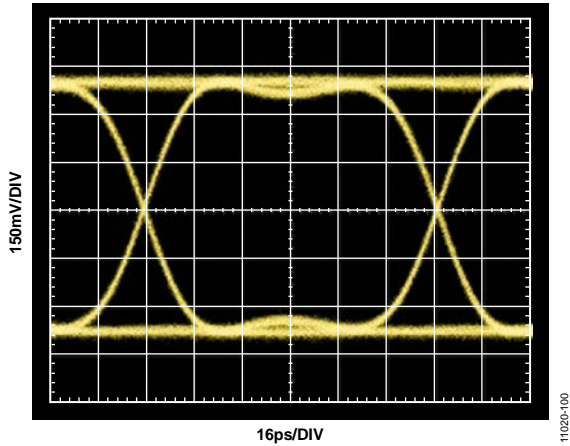


Figure 27. 10.3125 Gbps Input Eye (TP1 from Figure 47)

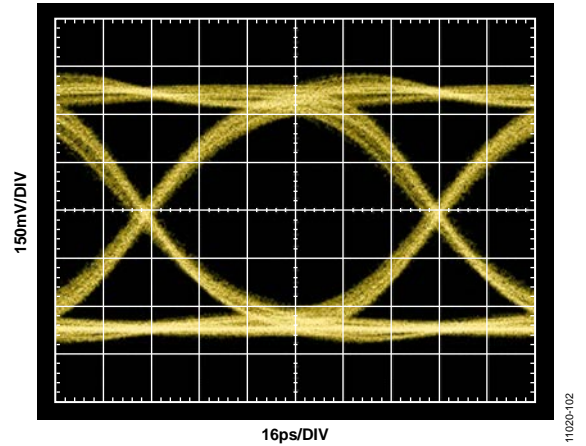


Figure 29. 10.3125 Gbps Output Eye (TP2 from Figure 47)

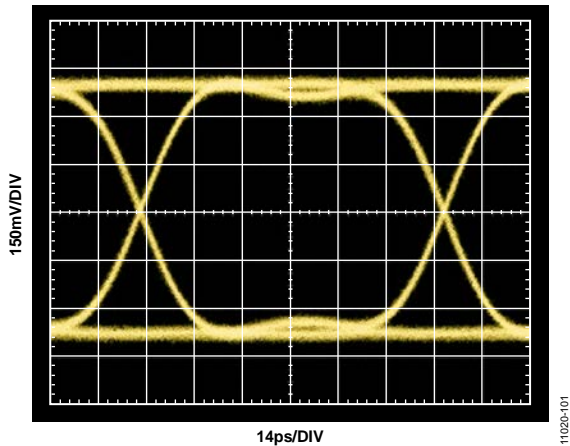


Figure 28. 11.3 Gbps Input Eye (TP1 from Figure 47)

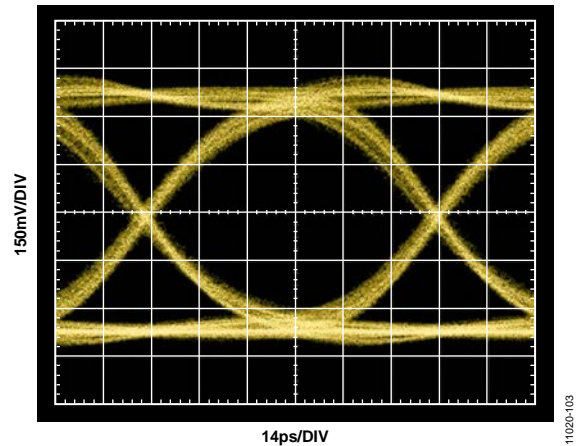


Figure 30. 11.3 Gbps Output Eye (TP2 from Figure 47)

EQUALIZATION TEST

$V_{CC} = V_{TTO} = 2.5\text{ V}$, $V_{TTI} = V_{CCIP8} = DV_{CC} = 1.8\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 50\ \Omega$, data rate = 11.3 Gbps, data pattern = PRBS 15, ac-coupled inputs and outputs, differential input swing = 800 mV p-p, EQ setting = 0x12 (note that the default EQ setting is used to compensate for the loss of the test fixture), PE boost = 1.94 dB (note that the default PE settings are used to compensate for the loss of the test fixture), unless otherwise noted.

For the equalization test circuit used for Figure 31 to Figure 38, see Figure 48.

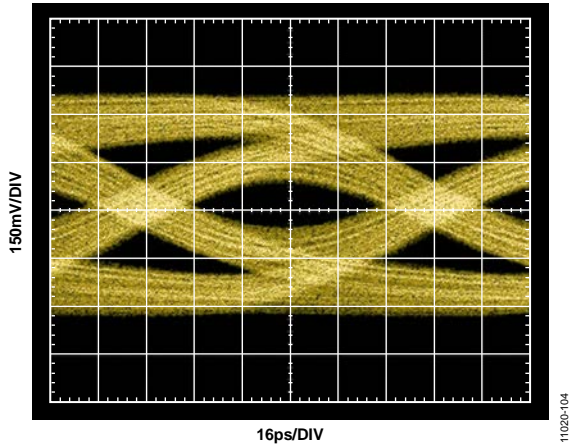


Figure 31. 10.3125 Gbps Input Eye; 15-Inch FR408 Input Channel (TP2 from Figure 48)

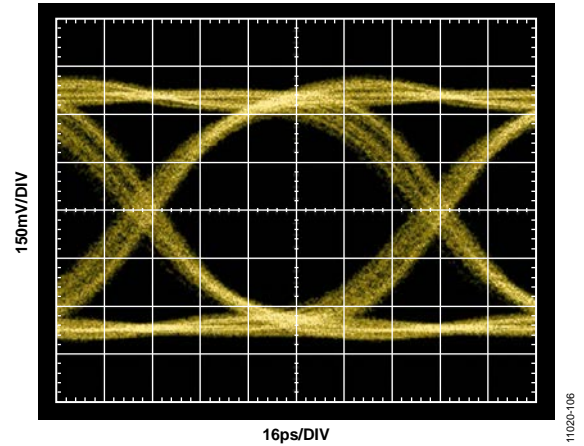


Figure 33. 10.3125 Gbps Output Eye; 15-Inch FR408 Input Channel, EQ = 0x72 (TP3 from Figure 48)

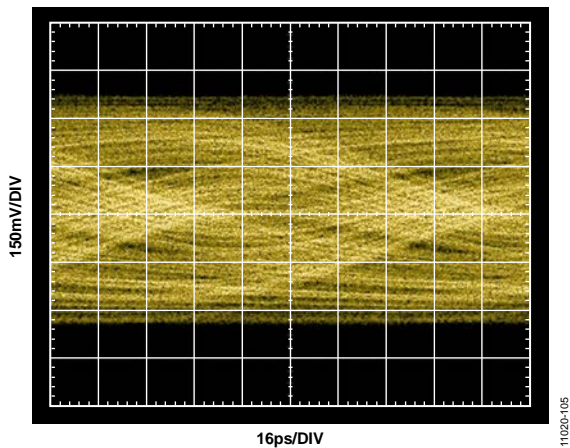


Figure 32. 10.3125 Gbps Input Eye; 25-Inch FR408 Input Channel (TP2 from Figure 48)

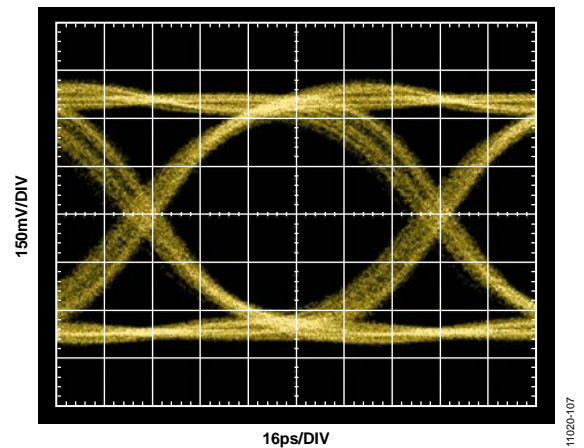


Figure 34. 10.3125 Gbps Output Eye; 25-Inch FR408 Input Channel, EQ = 0x94 (TP3 from Figure 48)

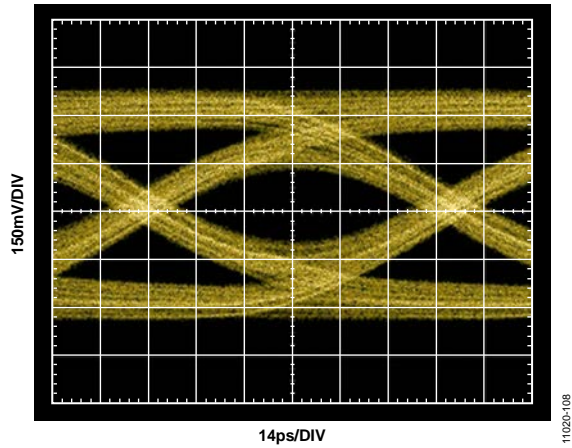


Figure 35. 11.3 Gbps Input Eye; 10-Inch FR408 Input Channel (TP2 from Figure 48)

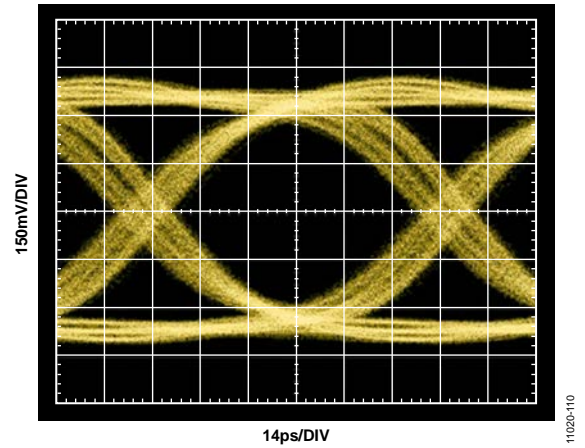


Figure 37. 11.3 Gbps Output Eye; 10-Inch FR408 Input Channel, EQ = 0x52 (TP3 from Figure 48)

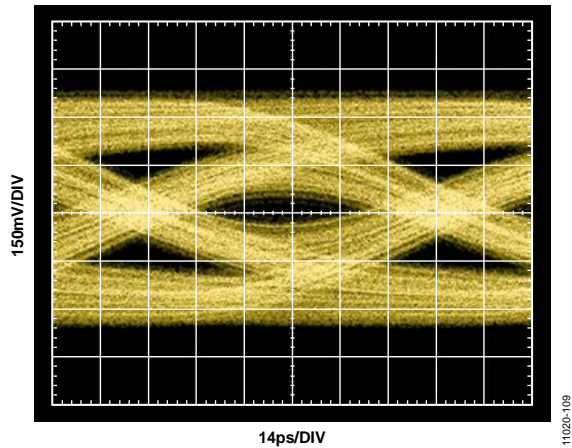


Figure 36. 11.3 Gbps Input Eye; 15-Inch FR408 Input Channel (TP2 from Figure 48)

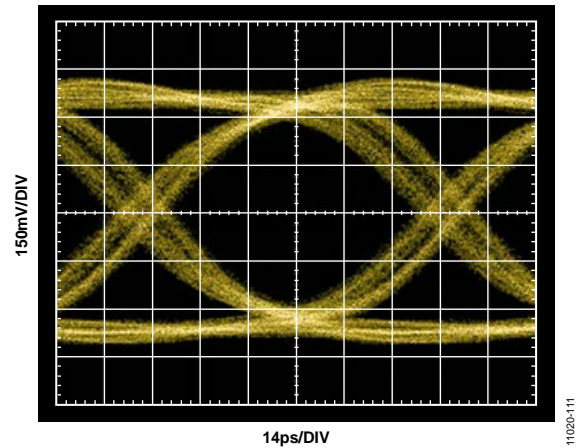


Figure 38. 11.3 Gbps Output Eye; 15-Inch FR408 Input Channel, EQ = 0x72 (TP3 from Figure 48)

PREEMPHASIS TEST

$V_{CC} = V_{TTO} = 2.5\text{ V}$, $V_{TTI} = V_{CCIP8} = DV_{CC} = 1.8\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 50\ \Omega$, data rate = 11.3 Gbps, data pattern = PRBS 15, ac-coupled inputs and outputs, differential input swing = 800 mV p-p, EQ setting = 0x12 (note that the default EQ setting is used to compensate for the loss of the test fixture), PE boost = 1.94 dB (note that the default PE settings are used to compensate for the loss of the test fixture), unless otherwise noted.

For the preemphasis test circuit used for Figure 39 to Figure 46, see Figure 49.

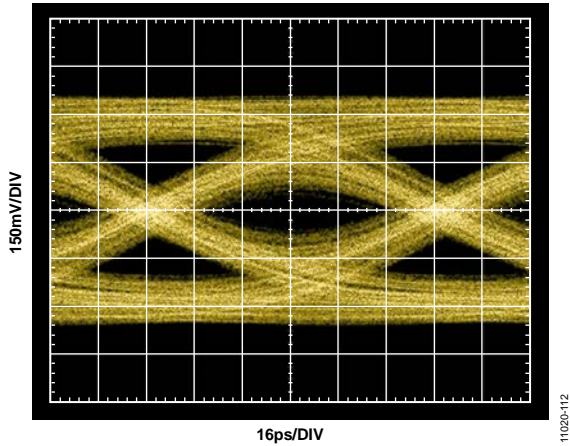


Figure 39. 10.3125 Gbps Output Eye; 10-Inch FR408 Output Channel, PE = 0 dB (TP3 from Figure 49)

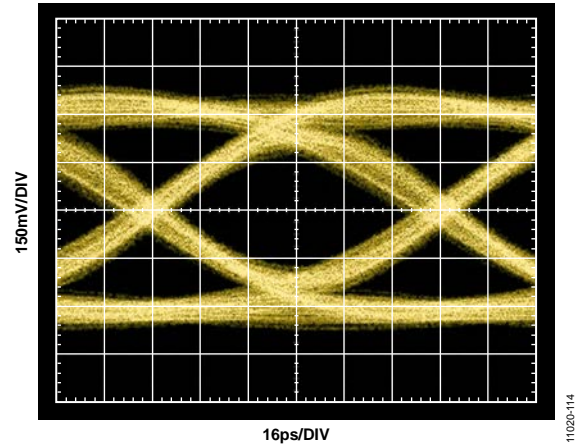


Figure 41. 10.3125 Gbps Output Eye; 10-Inch FR408 Output Channel, PE = 5.5 dB (TP3 from Figure 49)

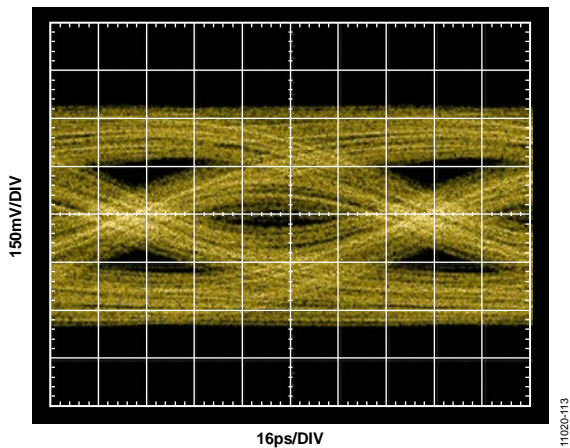


Figure 40. 10.3125 Gbps Output Eye; 15-Inch FR408 Output Channel, PE = 0 dB (TP3 from Figure 49)

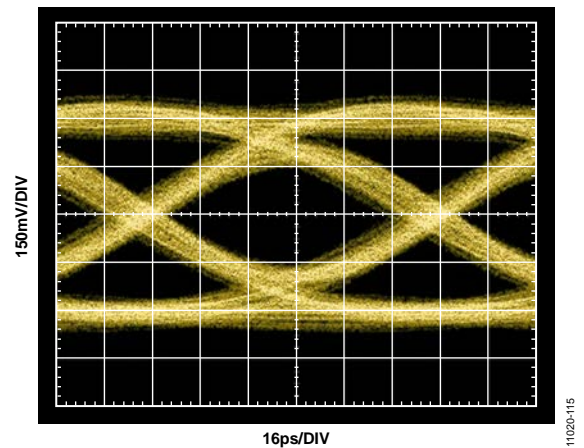


Figure 42. 10.3125 Gbps Output Eye; 15-Inch FR408 Output Channel, PE = 8.0 dB (TP3 from Figure 49)

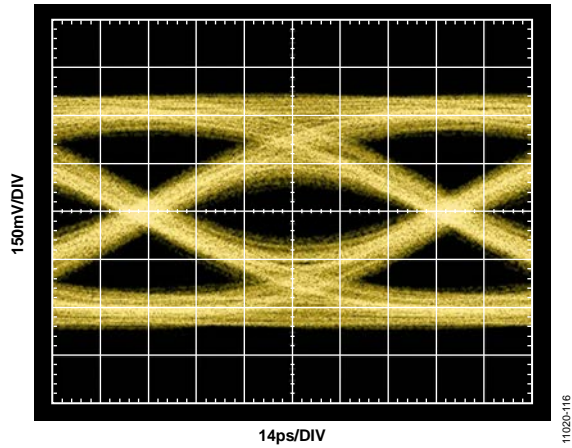


Figure 43. 11.3 Gbps Output Eye; 6-Inch FR408 Output Channel, PE = 0 dB (TP3 from Figure 49)

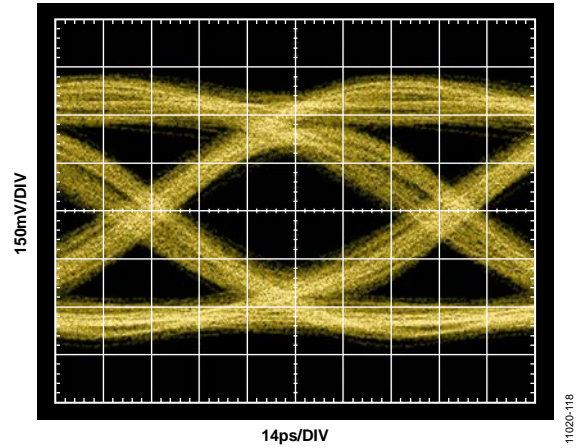


Figure 45. 11.3 Gbps Output Eye; 6-Inch FR408 Output Channel, PE = 4.9 dB (TP3 from Figure 49)

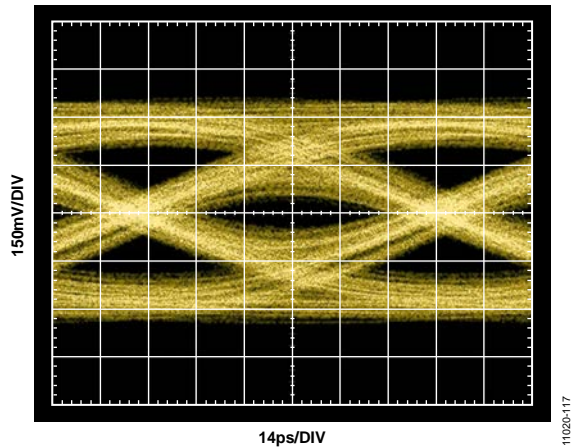


Figure 44. 11.3 Gbps Output Eye; 10-Inch FR408 Output Channel, PE = 0 dB (TP3 from Figure 49)

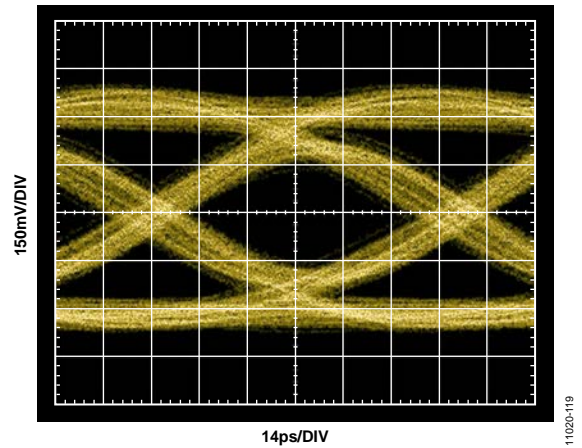


Figure 46. 11.3 Gbps Output Eye; 10-Inch FR408 Output Channel, PE = 6.0 dB (TP3 from Figure 49)

TEST CIRCUITS

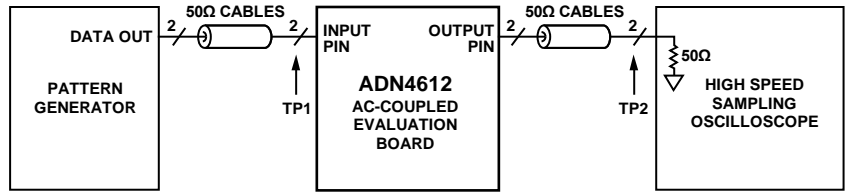


Figure 47. Standard Test Circuit

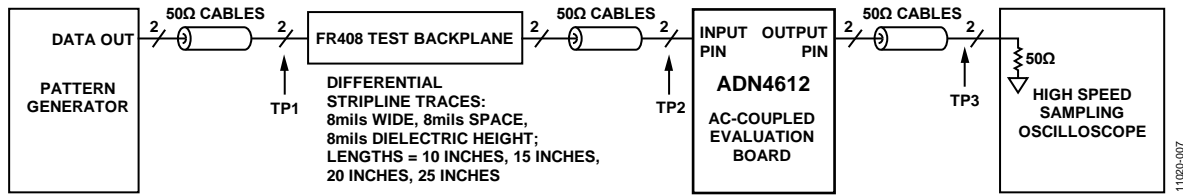


Figure 48. Equalization Test Circuit

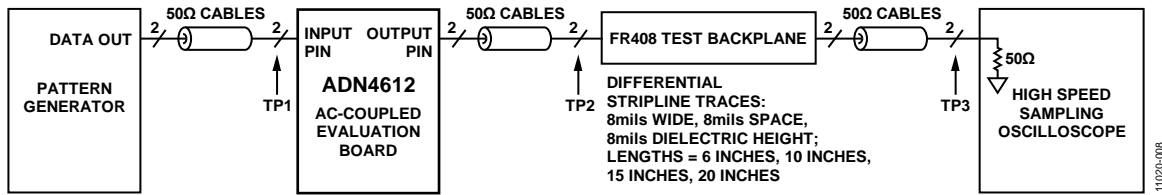


Figure 49. Preemphasis Test Circuit

THEORY OF OPERATION

INTRODUCTION

The ADN4612 is a 12 × 12, buffered, asynchronous crosspoint switch that provides input equalization, output preemphasis, and output level programming capabilities (see Figure 50).

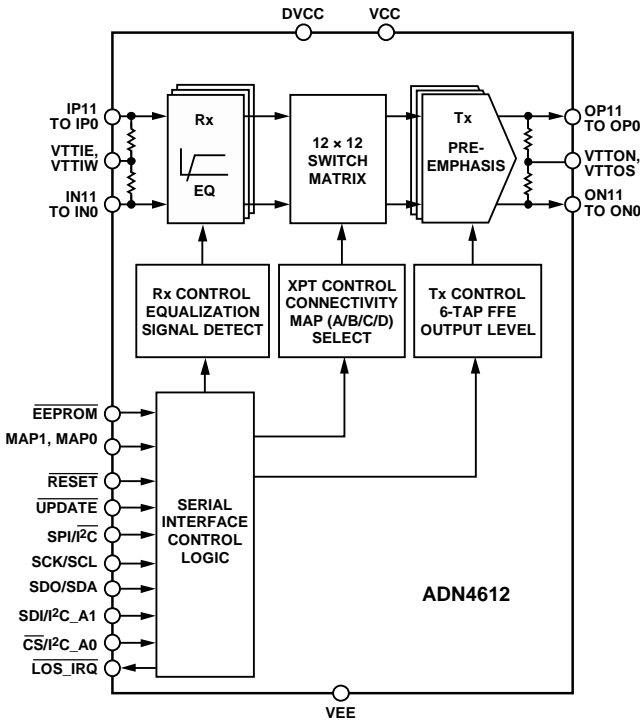


Figure 50. Block Diagram

The receivers integrate a programmable multizero transfer function, continuous time linear equalizer (CTLE) that is used to compensate for typical backplane or cable losses. Each receiver also includes a programmable loss of signal (LOS) detect circuit to monitor signal transmission faults.

The nonblocking, crosspoint switch core supports multicast and broadcast operation, allowing the ADN4612 to work in redundancy and port replication applications. Crosspoint connectivity can be stored in four programmable connection maps, which can be selected by either register control or external toggle pins.

Each transmitter includes extensive programmable output swings and a six-tap feedforward equalizer (FFE) to provide precursor and postcursor equalization.

The I/O on-chip termination resistors are tied to supplies, set by the user, to permit operation over a wide range of dc- and ac-coupled I/O configurations.

Both the receivers and transmitters each implement a sign swapping option (P/N swap) per lane; thus, the sign of the signal at the input/output pins can be inverted by the user, eliminating the need for board level crossovers.

The ADN4612 address registers can be accessed through a serial control interface. The serial interface supports both I²C and SPI protocols, selected by using the SPI/I²C dedicated control pin. The ADN4612 serial control pins function differently depending on which programming interface is selected, as described in Table 11.

An integrated I²C master can automatically load all receiver, transmitter, and switch configuration registers from an external serial EEPROM. This feature enables power-on ready operation and alleviates system controller overhead.

Table 11. Serial Interface Pin Control

| Pin No. | Mnemonic | Pin Function | |
|---------|-------------------------|--|--|
| | | I ² C Mode (SPI/I ² C = 0) | SPI Mode (SPI/I ² C = 1) |
| 19 | EEPROM | Load from EEPROM (active low) | Load from EEPROM (active low) |
| 20 | LOS_IRQ | Loss of signal detect interrupt (active low) | Loss of signal detect interrupt (active low) |
| 21 | MAP0 | XPT map select (LSB) | XPT map select (LSB) |
| 22 | MAP1 | XPT map select (MSB) | XPT map select (MSB) |
| 43 | SCK/SCL | I ² C serial clock | SPI serial clock |
| 44 | SDO/SDA | I ² C serial data | SPI serial data output |
| 45 | SPI/I ² C | I ² C mode select | SPI mode select |
| 46 | RESET | Device register reset (active low) | Device register reset (active low) |
| 65 | CS/I ² C_A0 | I ² C address (LSB) | SPI chip select |
| 66 | SDI/I ² C_A1 | I ² C address (MSB) | SPI serial data input |
| 67 | UPDATE | XPT update strobe (active low) | XPT update strobe (active low) |

RECEIVERS

The ADN4612 receivers incorporate 50 Ω on-chip termination, ESD protection, and a multizero equalization function that is capable of compensating for signal degradation at 11.3 Gbps from over 25 inches of FR408 backplane trace. The receive path also incorporates a LOS function that squelches the associated transmitter when the differential input voltage falls below a specified threshold value.

Input Structure and Allowed Input Levels

The ADN4612 tolerates a wide input common-mode range, which is found in the input characteristics section in Table 1.

To avoid activating the ESD protection devices, do not allow the maximum single-ended voltage level at the input to exceed the V_{IH} value listed in Table 1.

For dc-coupled applications, the maximum single-ended voltage level is determined by the V_{TTI} termination supply. For ac-coupled applications, the V_{TTI} termination supply level sets the input common-mode level of the signal (V_{ICM}). Therefore, to maintain proper input compliance, $V_{ICM} + V_{INPP,SE}/2 < V_{CC} + 0.3 V$.

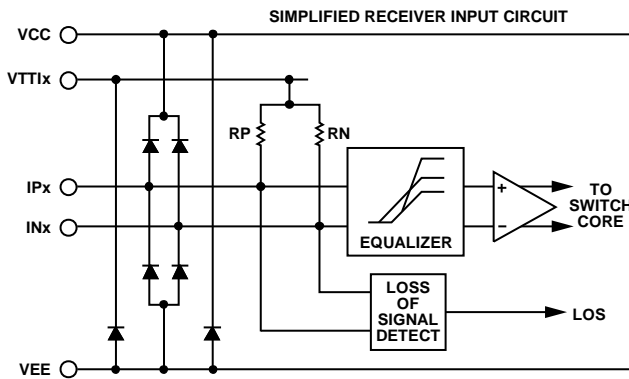


Figure 51. Simplified Input Circuit

Equalization

Every input lane offers a low power, asynchronous, programmable receive equalizer for NRZ data of up to 11.3 Gbps. The equalizer is a two-stage CTLE where each stage is individually programmable to allow optimum jitter performance over a broad range of input

channel lengths. Register-based control provides the user with a broad base of 255 equalizer settings. Register Address 0x80 to Register Address 0x85 control the equalizer settings for Receiver Input 0 to Receiver Input 5. Register Address 0x90 to Register Address 0x95 control the equalizer settings for Receiver Input 6 to Receiver Input 11. The four LSBs program the active equalizer (EQA) settings. The four MSBs program the passive equalizer (EQP) settings.

It is recommended that the EQ response be optimized to best match the inverse of the channel attenuation. Table 12 lists some recommended values for EQP and EQA based on measured results with a FR408 test board. Figure 52 shows the magnitude of the frequency response of a sample FR408 test board with various trace lengths.

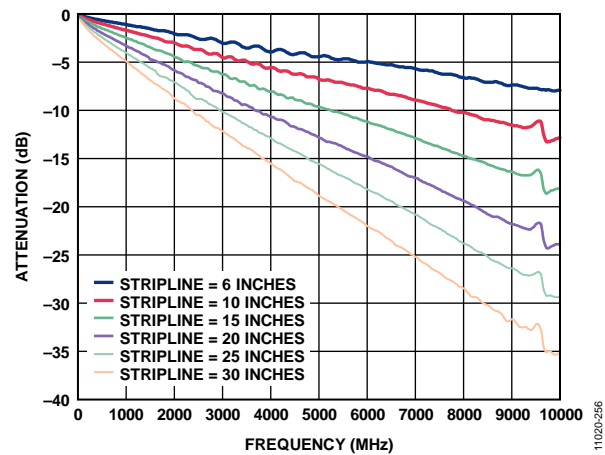


Figure 52. Sample Test Trace Attenuation

Receiver Lane Inversion—P/N Swap

The receiver P/N inversion is a feature that allows the user to implement the equivalent of a board level crossover, without additional via impedance discontinuities that degrade the high frequency integrity of the signal path. The P/N lane inversion is available independently for each of the 12 input channels, which are controlled by writing a Logic 1 to the appropriate Rx sign bit location of the Rx swap sign registers (Register Address 0x08 and Register Address 0x09).

Table 12. Recommended Equalizer Settings

| FR408 Trace (Inches) | Attenuation at 5.65 GHz (dB) | EQP (Code) | EQP (dB) | EQA (Code) | EQA (dB) | Total EQ (dB) | Minimum DC Swing (mV p-p Differential) | Maximum Rate (Gbps) |
|----------------------|------------------------------|------------|----------|------------|----------|---------------|--|---------------------|
| <1 | <-2 | 0 | 0 | 0 | 1.0 | 1.0 | 200 | 11.3 |
| 6 | -5 | 4 | 2.5 | 0 | 1.0 | 3.5 | 200 | 11.3 |
| 10 | -7 | 6 | 4.0 | 0 | 1.0 | 5.0 | 400 | 11.3 |
| 15 | -10 | 8 | 5.5 | 4 | 3.0 | 8.5 | 600 | 11.3 |
| 20 | -13 | A | 8.0 | 4 | 3.0 | 11.0 | 600 | 10.3125 |
| 25 | -16 | A | 8.0 | 6 | 4.0 | 12.0 | 800 | 10.3125 |
| 30 | -20 | A | 8.0 | A | 6.0 | 14.0 | 600 | 8.5 |

Receiver and Equalizer Disable

The ADN4612 receiver and equalizer circuits are disabled by default. To enable these circuits, write a Logic 1 as follows:

- For the Receiver Input 5 to Receiver Input 0 enable control, write to Register Address 0x86.
- For the Receiver Input 11 to Receiver Input 6 enable control, write to Register Address 0x96.
- For the Receiver Input 5 to Receiver Input 0 equalizer enable, write to Register Address 0x87.
- For the Receiver Input 11 to Receiver Input 6 equalizer enable, write to Register Address 0x97.

For applications with very short input traces, it may be desirable to disable the equalizer; otherwise, it is recommended that the receiver equalizer circuits be enabled.

Offset Calibration Circuit

The ADN4612 receivers incorporate an offset calibration circuit to minimize offsets in the receiver architecture, thereby reducing the amount of duty cycle distortion (DCD) contribution to residual deterministic jitter. The offset calibration circuit operates on dc-balanced data streams only.

The offset calibration circuit is disabled for all receiver inputs by default. Enable the offset calibration circuit by writing a Logic 1 to the appropriate bit location, as follows:

- For the Receiver Input 5 to Receiver Input 0 offset calibration enable, write to Register Address 0xA0.
- For the Receiver Input 11 to Receiver Input 6 offset calibration enable, write to Register Address 0xA8.

Loss of Signal (LOS) Detect

Each receiver includes a low power, LOS detector. The loss of signal circuit monitors the received data stream and generates a system interrupt when the received signal amplitude falls below the LOS assert level for an interval that is longer than the LOS delay setting. When the receiver detects a LOS event, it squelches its associated transmitter, lowering the output current to submicroamps. This prevents the high gain, wide bandwidth signal path from turning low level system noise on an undriven input pair into a source of hostile crosstalk at the transmitter. The squelch feature is disabled by default and can be enabled by writing a Logic 1 to the LSB (Bit 0) of Register Address 0x05. The LOS detector circuits are also disabled by default and can be enabled on a per input basis by writing a Logic 1 to the appropriate bit locations, as follows:

- For the Receiver Input 5 to Receiver Input 0 LOS detector enable, write to Register Address 0x88.
- For the Receiver Input 11 to Receiver Input 6 LOS detector enable, write to Register Address 0x98.

When the received signal amplitude exceeds the LOS deassert level, the lane is enabled. The LOS assert and deassert levels are configured for two groups of six inputs each. The LOS assert

and deassert levels for Receiver Input 5 to Receiver Input 0 are programmable using Register Address 0x8E, and Receiver Input 11 to Receiver Input 6 are programmable using Register Address 0x9E. To ensure proper LOS operation, the LOS deassert threshold level cannot be set lower than the LOS assert threshold level.

The LOS delay settings are programmable on a per input basis, using the Rx LOS time control registers (Register Address 0x89, Register Address 0x8A, Register Address 0x8B, Register Address 0x99, Register Address 0x9A, and Register Address 0x9B).

The LOS delay time settings, together with the assert and deassert threshold levels, are listed in Table 13.

Table 13. LOS Assert/Deassert Levels and Delay Settings

| Code (Hex) | LOS Assert Level (mV p-p Differential) | LOS Deassert Level (mV p-p Differential) | LOS Delay |
|------------|--|--|---------------|
| 0x0 | 0 | 0 | 2.5 ns |
| 0x1 | 25 | 25 | 5.0 ns |
| 0x2 | 50 | 50 | 10.0 ns |
| 0x3 | 75 | 75 | 20.0 ns |
| 0x4 | 100 | 100 | 40.0 ns |
| 0x5 | 125 | 125 | 80.0 ns |
| 0x6 | 150 | 150 | 160.0 ns |
| 0x7 | 175 | 175 | 320.0 ns |
| 0x8 | 200 | 200 | 640.0 ns |
| 0x9 | 225 | 225 | 1.28 μ s |
| 0xA | 250 | 250 | 2.56 μ s |
| 0xB | 275 | 275 | 5.12 μ s |
| 0xC | 300 | 300 | 10.24 μ s |
| 0xD | N/A ¹ | N/A ¹ | 20.48 μ s |
| 0xE | N/A ¹ | N/A ¹ | 40.96 μ s |
| 0xF | N/A ¹ | N/A ¹ | 81.92 μ s |

¹ N/A means not applicable.

The LOS_IRQ pin can be used to generate an interrupt for the system control software. The LOS_IRQ pin is an open-drain, active low output that allows multiple LOS_IRQ signals to be wire-ORed. Note that an external pull-up resistor of 1 k Ω is required for this configuration. The logic level on the LOS_IRQ pin represents the logical NOR of all LOS sticky status bits for all enabled receivers.

In a standard implementation, when the LOS_IRQ pin goes low, the system software registers the interrupt and polls the LOS sticky status registers to determine which input lost the signal, and whether that signal has been restored. The LOS interrupt for an individual receiver is ignored by default. LOS interrupt monitoring for a given receiver is enabled by writing a Logic 1 to the appropriate bit location in the LOS interrupt enable registers. The LOS interrupt enable for Receiver Input 5 to Receiver Input 0 is programmable using Register Address 0x8F and, for Receiver Input 11 to Receiver Input 6, using Register Address 0x9F.

An LOS sticky status bit value of Logic 1 indicates that a LOS event has occurred on a given receiver. The LOS sticky status values are accessed using Register Address 0x8D and Register Address 0x9D. The LOS sticky bits are cleared by writing Logic 0 to the LOS sticky bit register addresses.

The LOS status bits are updated continuously to indicate the instantaneous status for each enabled receiver. The LOS status values can be accessed through Register Address 0x8C and Register Address 0x9C. The LOS_IRQ pin remains low after a LOS event until all sticky registers are cleared and all active status registers read as 0.

SWITCH CORE

The ADN4612 switch core is a fully nonblocking, 12 × 12 array that allows multicast and broadcast configurations. The configuration of the switch core is programmed through the serial control interface. The crosspoint configuration map controls the connectivity of the switch core and consists of a double rank register architecture, as shown in Figure 53. Each rank consists of six 8-bit registers. The second rank registers contain the current state of the crosspoint, and the first rank registers contain the next state.

Each entry in the connection map stores four bits per output that indicate which of the 12 inputs are connected to a given output. An entire connectivity matrix can be programmed at one time by passing data from the first rank registers into the second rank registers by writing a Logic 1 to the XPT_Update register (Register Address 0xDF), which is a write only register. Alternatively, strobe the UPDATE pin low. UPDATE is level sensitive; therefore, a falling edge transition initiates the XPT update. Holding the UPDATE pin low causes the second rank to become transparent.

The first rank registers are four separate, volatile memory banks, each containing six 8-bit registers that store connection configurations for the crosspoint; Map A is the default register table (Register Address 0xB0 to Register Address 0xB5). Map B is located from Register Address 0xB8 to Register Address 0xBD. Map C is located from Register Address 0xC0 to Register Address 0xC5. Map D is located from Register Address 0xC8 to Register Address 0xD5.

Register Address 0xCD. All maps are read/write accessible. By default, the active map is selected by the MAP1 and MAP0 external pin controls (see Table 14).

The external pin controls can be overridden by writing Logic 1 to Bit 4 (XPT_TABLE_SELECT_EN) of the XPT_Table_Map register (Register Address 0xDE).

Table 14. Map Select Pin Control

| Pin Control (MAP1, MAP0) | Selected Map |
|--------------------------|--------------|
| 00b | A |
| 01b | B |
| 10b | C |
| 11b | D |

The crosspoint is configured by addressing the register assigned to the desired output and writing the binary coded value that represents the desired input connection. The data is stored in the first rank of latches in Map A, Map B, Map C, or Map D. This process is repeated until each of the desired input-to-output connections is programmed.

In situations where all outputs are to be programmed to a single input, a broadcast command is available. A broadcast command is issued by writing the binary value of the desired input to the XPT_Broadcast register (Register Address 0x0F). The broadcast is applied to the selected map only. The XPT_Broadcast register is a write only register.

The current state of the crosspoint connectivity is available by reading the XPT map transmitter lane status registers (Register Address 0xD0 to Register Address 0xD5), which correspond to Transmitter Output 0 to Transmitter Output 11.

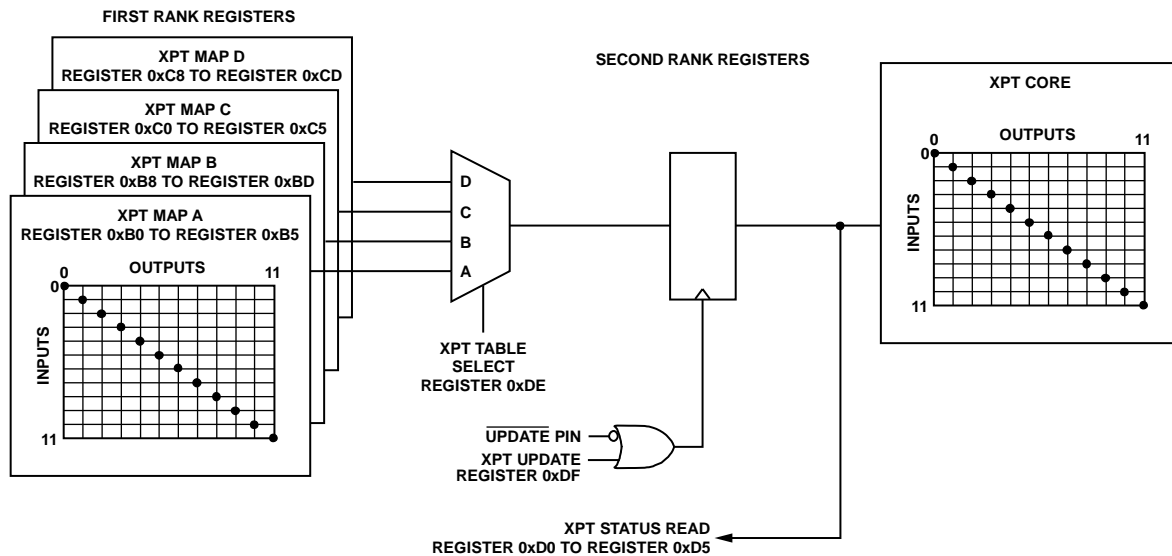


Figure 53. Crosspoint Connection Map Block Diagram

TRANSMITTERS

Output Structure

The ADN4612 transmitter outputs incorporate 50 Ω termination resistors, ESD protection, and a CML style driver with a programmable tail current (see Figure 55). Each channel includes a fully programmable, six-tap FFE. The flexible programmability of the FFE enables a broad range of output filter shapes to compensate for signal impairments, such as intersymbol interference (ISI), caused by channel attenuation.

Multitap Feedforward Equalizer

A block diagram of the FFE is shown in Figure 54. The FFE consists of eight output current driver elements (PC and D0 to D6) with a maximum of 16 mA per driver and five delay line elements (τ) arranged to create a six-tap FFE with individually programmable coefficients. A summing junction at the output combines the output currents of all the drivers into the load.

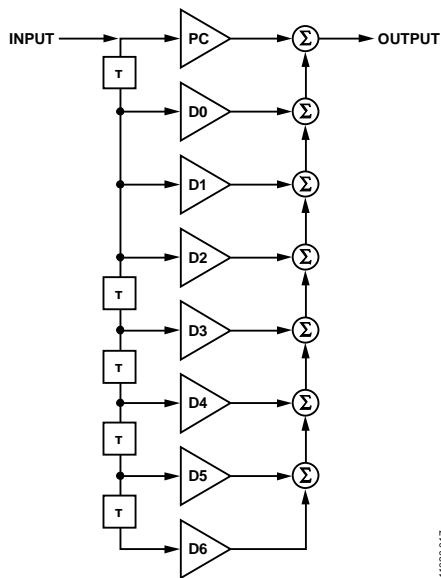


Figure 54. Output FFE Block Diagram

The main tap comprises three independent output driver elements (D0, D1, and D2). The precursor tap (PC) and the four postcursor taps (D3, D4, D5, and D6) are each individual output drivers. The tap delay, τ, is optimized for 11.3 Gbps data rates. This flexible implementation enables both preemphasis and deemphasis. The FFE architecture also facilitates shifting the location of the main tap to create multiple precursors.

Each driver is controlled by a 4-bit output level value and sign code, a 2-bit resolution value, and a 2-bit enable. The output current per tap (in mA) is listed in Table 15 for the corresponding output level and resolution codes. The MSB of the output level is the sign bit and the three LSBs represent a 3-bit magnitude. To convert the table from mA to mV p-p differential, use the following equation:

$$V_{Dx} = (2 \times I_{Dx}) \times (50 \Omega || 50 \Omega)$$

Table 15. Driver Element Current (mA) and Resolution Codes

| Driver Current Level Codes (Binary) | Resolution Codes | | | |
|-------------------------------------|------------------|------------------|---------------------|--------------------|
| | 00b (Full Scale) | 01b (Half Scale) | 10b (Quarter Scale) | 11b (Eighth Scale) |
| 0000 | +2 | +1 | +0.5 | +0.25 |
| 0001 | +4 | +2 | +1.0 | +0.5 |
| 0010 | +6 | +3 | +1.5 | +0.75 |
| 0011 | +8 | +4 | +2.0 | +1.0 |
| 0100 | +10 | +5 | +2.5 | +1.25 |
| 0101 | +12 | +6 | +3.0 | +1.5 |
| 0110 | +14 | +7 | +3.5 | +1.75 |
| 0111 | +16 | +8 | +4.0 | +2.0 |
| 1000 | -2 | -1 | -0.5 | -0.25 |
| 1001 | -4 | -2 | -1.0 | -0.5 |
| 1010 | -6 | -3 | -1.5 | -0.75 |
| 1011 | -8 | -4 | -2.0 | -1.0 |
| 1100 | -10 | -5 | -2.5 | -1.25 |
| 1101 | -12 | -6 | -3.0 | -1.5 |
| 1110 | -14 | -7 | -3.5 | -1.75 |
| 1111 | -16 | -8 | -4.0 | -2.0 |

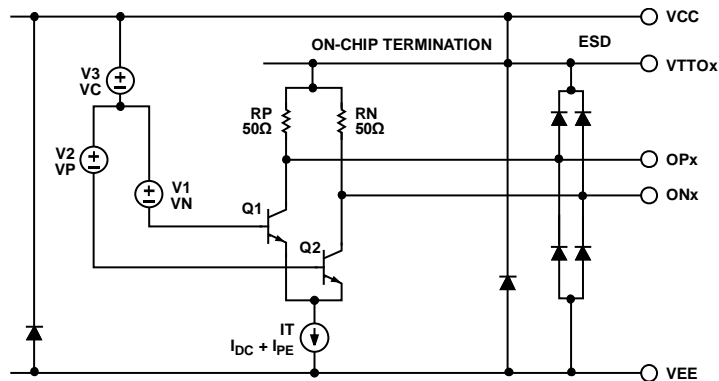


Figure 55. Simplified Output Circuit

Transmitter Disable/Enable

Each transmitter is equipped with disable/enable control (see Table 16). Disable is a full power-down state: the transmitter current is reduced to 0 mA, and the output pins (OPx and ONx) pull to V_{TTO} . All transmitters are disabled by default.

To enable a transmitter, write a Logic 1 to the appropriate bit location in the Tx enable registers (Register Address 0x02 and Register Address 0x03).

Table 16. Transmitter Disable/Enable Control

| Bit Setting (Binary) | Transmitter Enable/Disable Control |
|----------------------|------------------------------------|
| 0 | Disable (default) |
| 1 | Enable |

Transmitter Lane Inversion—P/N Swap

The transmit P/N inversion is a feature that allows the user to implement the equivalent of a board level crossover in a much smaller area and without additional via impedance discontinuities that degrade the high frequency integrity of the signal path (see Table 17). The P/N lane inversion is available independently for each of the 12 output channels, which are controlled by writing a Logic 1 to the appropriate transmitter sign bit location of the Tx swap sign registers (Register Address 0x0A and Register Address 0x0B).

Table 17. Signal Path Polarity (Swap Sign) Control

| Bit Setting (Binary) | Signal Path Polarity |
|----------------------|------------------------|
| 0 | Noninverting (default) |
| 1 | Inverting |

Table 19. Output Level Settings

| D0 Resolution Code (Binary) | D0 Current Code (Binary) | D0 Current (mA) | D1 Resolution Code (Binary) | D1 Current Code (Binary) | D1 Current (mA) | ITTO/Lane (D0 + D1) (mA) | Output Level (mV p-p Differential) |
|-----------------------------|--------------------------|-----------------|-----------------------------|--------------------------|-----------------|--------------------------|------------------------------------|
| 00 | 0000 | 2.0 | 00 | 0000 | 2.0 | 4.0 | 200 |
| 00 | 0000 | 2.0 | 01 | 0010 | 3.0 | 5.0 | 250 |
| 01 | 0010 | 3.0 | 01 | 0010 | 3.0 | 6.0 | 300 |
| 00 | 0001 | 4.0 | 01 | 0010 | 3.0 | 7.0 | 350 |
| 00 | 0001 | 4.0 | 00 | 0001 | 4.0 | 8.0 | 400 |
| 00 | 0001 | 4.0 | 01 | 0100 | 5.0 | 9.0 | 450 |
| 01 | 0100 | 5.0 | 01 | 0100 | 5.0 | 10.0 | 500 |
| 00 | 0010 | 6.0 | 01 | 0100 | 5.0 | 11.0 | 550 |
| 00 | 0010 | 6.0 | 00 | 0010 | 6.0 | 12.0 | 600 |
| 00 | 0010 | 6.0 | 01 | 0110 | 7.0 | 13.0 | 650 |
| 01 | 0110 | 7.0 | 01 | 0110 | 7.0 | 14.0 | 700 |
| 00 | 0011 | 8.0 | 01 | 0110 | 7.0 | 15.0 | 750 |
| 00 | 0011 | 8.0 | 00 | 0011 | 8.0 | 16.0 | 800 |
| 00 | 0100 | 10.0 | 01 | 0110 | 7.0 | 17.0 | 850 |
| 00 | 0100 | 10.0 | 00 | 0011 | 8.0 | 18.0 | 900 |
| 00 | 0100 | 10.0 | 00 | 0100 | 10.0 | 20.0 | 1000 |
| 00 | 0101 | 12.0 | 00 | 0100 | 10.0 | 22.0 | 1100 |
| 00 | 0101 | 12.0 | 00 | 0101 | 12.0 | 24.0 | 1200 |
| 00 | 0110 | 14.0 | 00 | 0101 | 12.0 | 26.0 | 1300 |
| 00 | 0110 | 14.0 | 00 | 0110 | 14.0 | 28.0 | 1400 |
| 00 | 0111 | 16.0 | 00 | 0110 | 14.0 | 30.0 | 1500 |
| 00 | 0111 | 16.0 | 00 | 0111 | 16.0 | 32.0 | 1600 |

Driver Element Enable Bits

The current driver elements (PC, D0 to D6) for each transmitter are equipped with enable/disable control. The D0 and D1 current driver elements are enabled by default.

To enable a driver element for a given transmitter output, write a bit setting of 11b to the appropriate Tx driver enable register. To disable a driver element for a given transmitter output, write a bit setting of 00b to the appropriate Tx driver enable register.

Table 18. Driver Enable/Disable Control

| Bit Setting (Binary) | Driver Enable/Disable Control |
|----------------------|---|
| 00 | Full disable; both driver and predriver are off |
| 11 | Full enable; both driver and predriver are on |

Output Level Programming

The main tap current driver elements, D0 and D1, configure the output level of the transmitter. Register-based control allows the user to set the transmitter output levels on a per lane basis to a broad range of amplitude levels. A subsegment of amplitude level settings is listed in Table 19. The differential output level (OLEV) amplitude is calculated using the following formula:

$$OLEV \text{ mV p-p Differential} = (2 \times (I_{D0} + I_{D1})) \times (50 \Omega || 50 \Omega)$$

Using the Resolution Code Value Settings

The resolution code value sets the CML output driver LSB step size, which, in turn, sets the voltage LSB step size. The full-scale range (that is, maximum output voltage) of each driver is reduced by increasing the resolution code, as listed in Table 20.

Table 20. Resolution Code Settings

| Resolution Code (Binary) | I _{OUT} LSB (mA) | V _{OUT} LSB (mV p-p Differential) | Full-Scale Current Range (mA) |
|--------------------------|---------------------------|--|-------------------------------|
| 00 | ±2.0 | ±100 | ±16.0 |
| 01 | ±1.0 | ±50 | ±8.0 |
| 10 | ±0.5 | ±25 | ±4.0 |
| 11 | ±0.25 | ±12.5 | ±2.0 |

The resolution setting is independently programmable for each current driver element. The ability to control the LSB step size for each current driver element allows for the programmability of a wide range of transmit FIR filter shapes or tap coefficient settings to generate a transmit equalization response that closely matches the inverse of the channel loss, minimizing the overall residual jitter in the signal. Examples of transmit FIR frequency response are shown in Figure 57 to Figure 59.

Channel Compensation Using FFE

Signal impairments can be caused by a variety of physical phenomena, including but not limited to dielectric absorption, skin effect loss, and reflections due to impedance mismatches. Similarly, the impulse response of a channel can have a variety of shapes. An example of a channel impulse response is shown in Figure 56.

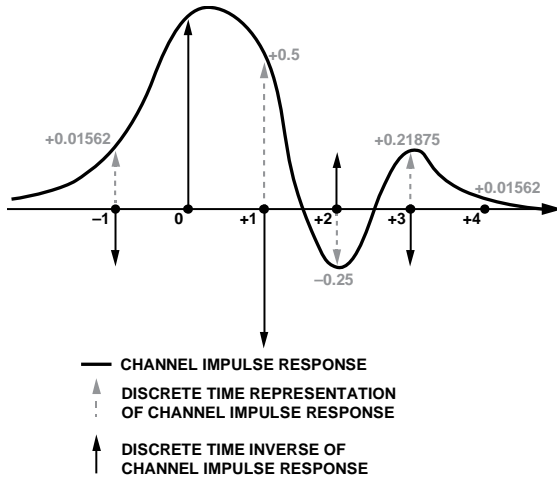


Figure 56. Example Channel Impulse Response

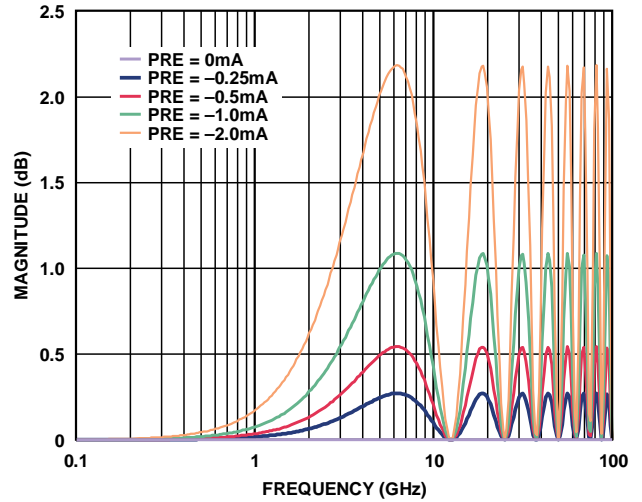


Figure 57. Transmit FIR Response (Precursor Only)

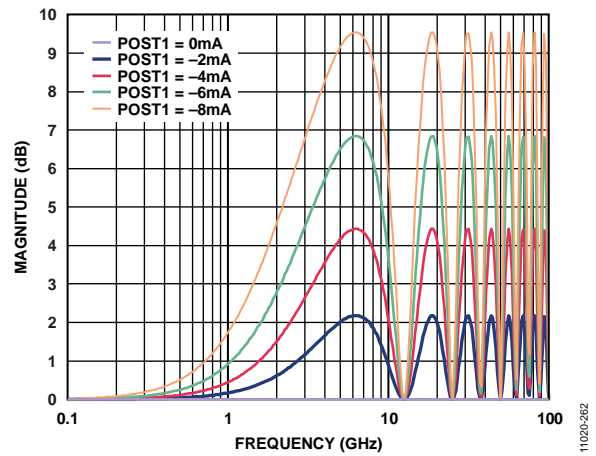


Figure 58. Transmit FIR Response (Single Postcursor Only)

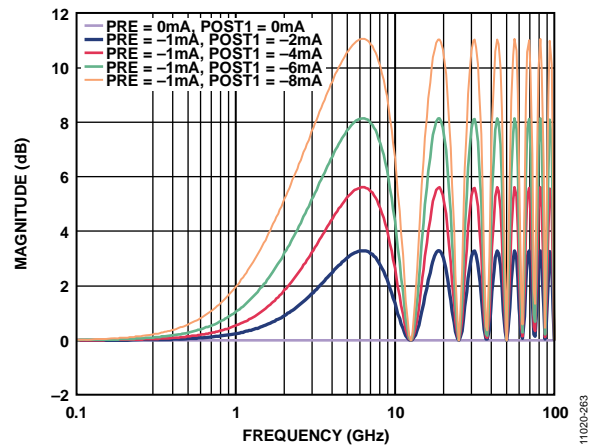


Figure 59. Transmit FIR Response (Precursor and Single Postcursor Taps)

Example—Tap Coefficient Calculation

To compensate for the degradation caused by a channel, the desired result is to maximize the signal energy in Tap 0 and remove ISI from all other taps. Therefore, set the tap coefficients of each tap (current driver element) of the FFE to the inverse of the corresponding values of the channel impulse response. Assume that the discrete time representation of the channel impulse response shown in Figure 56 results in the normalized values shown at each sample point.

The following steps illustrate how to calculate the theoretical ADN4612 transmit FIR tap coefficient values to match the inverse of the discrete time impulse response values:

1. Choose a main Tap 0 value (D0 + D1). For this example, a main tap value of 16 mA is selected (a_0).
2. Normalize the tap coefficient weights to the main tap value, and calculate it to match the inverse of the channel impulse response. For example,

$$\text{Precursor Tap } (a_{-1}) = -0.01562 = x/16 \text{ mA}$$

Solving for the value of x results in a precursor current driver tap value setting of $-0.25 \text{ mA} = (16 \text{ mA} \times -0.01562)$.

3. Repeat this process for each postcursor tap that is required to cancel out the effects of the channel.

$$a_1 = -0.5 = x/16 \text{ mA}; x = -8 \text{ mA}$$

$$a_2 = 0.25 = x/16 \text{ mA}; x = 4 \text{ mA}$$

$$a_3 = -0.21875 = x/16 \text{ mA}; x = -3.5 \text{ mA}$$

$$a_4 = -0.01562 = x/16 \text{ mA}; x = -0.25 \text{ mA}$$

The theoretical example results are summarized in Table 21.

Set all the ADN4612 precursor and postcursor driver elements to the calculated current settings to shape the FIR filter response to cancel out the effect of the channel loss on the signal. Figure 57 through Figure 59 illustrate how the ADN4612 FIR frequency response changes with precursor and first postcursor tap settings.

Table 21. Summary of Tap Coefficient Example

| Discrete Time Sample | Impulse Value | FFE Tap | FFE Tap Coefficient Value | FFE Tap Current (mA) | FFE Tap Voltage (mV p-p Differential) |
|----------------------|---------------|-----------------|---------------------------|----------------------|---------------------------------------|
| $x[n - 1]$ | +0.01562 | PC (a_{-1}) | -0.01562 | -0.25 | -12.5 |
| $x[n + 1]$ | +0.5 | D3 (a_{+1}) | -0.5 | -8 | -400 |
| $x[n + 2]$ | -0.25 | D4 (a_{+2}) | +0.25 | +4 | +200 |
| $x[n + 3]$ | +0.21875 | D5 (a_{+3}) | -0.21875 | -3.5 | -175 |
| $x[n + 4]$ | +0.01562 | D6 (a_{+4}) | -0.01562 | -0.25 | -12.5 |

Preemphasis/Deemphasis Using A Two-Tap FFE

In cases where dielectric absorption is the dominant cause of signal impairment, only a single postcursor tap may be effective in compensating for the majority of the ISI error caused by the high frequency attenuation. Figure 60 shows the impulse response of a two-tap FFE filter. This filter implements a first-order, high-pass filter where the value of M is the main tap coefficient and the value of D is the first postcursor tap. Figure 61 shows the resulting single-ended step response of this filter.

The dc (low frequency) amplitude is given by the sum of the main tap and the first postcursor tap. Because the value of the postcursor tap is negative, $V_{SW-DC} = (D0 + D1 + D2 - D3)$. The boosted (high frequency) signal amplitude is given by the difference between the main tap and the delayed tap: $V_{SW-PE} = (D0 + D1 + D2 - (-D3))$. Therefore, the theoretical high-pass boost in dB is given by

$$Boost = 20\log[(V_{SW-PE})/(V_{SW-DC})]$$

Table 23 provides the theoretical high-pass preemphasis values for a given output level setting. Table 24 provides the theoretical high-pass deemphasis values for a given output.

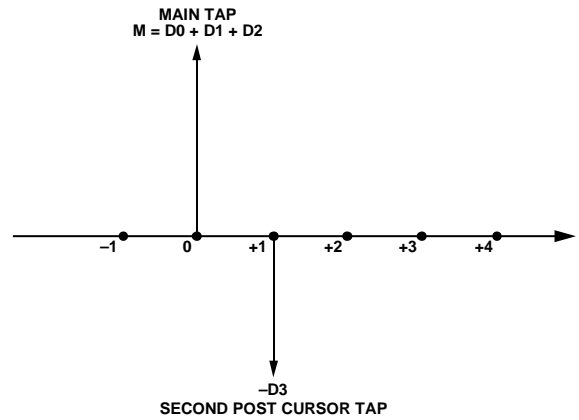


Figure 60. Impulse Response of a Two-Tap FFE

11020-019

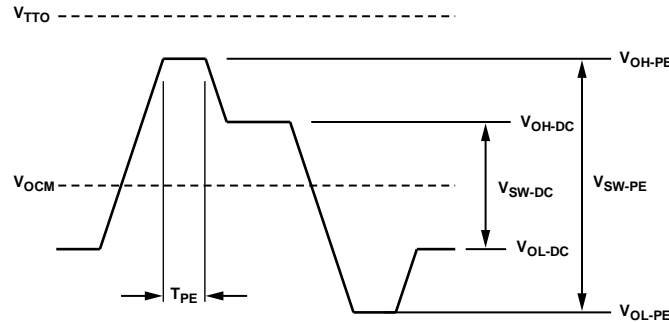


Figure 61. Step Response of Two-Tap FFE

11020-020

Table 22. Symbol Definitions

| Symbol | Formula | Definition |
|------------------------------|--|---|
| I_{DC} | Programmable: $(M - D)$ | Output current that sets output level |
| I_{PE} | Programmable: (D) | Output current for a preemphasized delayed tap |
| I_{TTO} | $M + D $ | Total transmitter output current |
| V_{DPP-DC} | $25 \Omega \times I_{DC} \times 2$ | Peak-to-peak differential voltage swing of a waveform that is not preemphasized |
| V_{DPP-PE} | $25 \Omega \times I_{TTO} \times 2$ | Peak-to-peak differential voltage swing of a preemphasized waveform |
| V_{SW-DC} | $V_{DPP-DC}/2 = V_{OH-DC} - V_{OL-DC}$ | DC single-ended voltage swing |
| V_{SW-PE} | $V_{DPP-PE}/2 = V_{OH-PE} - V_{OL-PE}$ | Preemphasized single-ended voltage swing |
| $\Delta V_{OCM_DC-COUPLED}$ | $25 \Omega \times I_{TTO}/2$ | Output common-mode shift, dc-coupled outputs |
| $\Delta V_{OCM_AC-COUPLED}$ | $50 \Omega \times I_{TTO}/2$ | Output common-mode shift, ac-coupled outputs |
| V_{OCM} | $V_{TTO} - \Delta V_{OCM} = (V_{OH-DC} + V_{OL-DC})/2$ | Output common-mode voltage |
| V_{OH-DC} | $V_{TTO} - \Delta V_{OCM} + V_{DPP-DC}/2$ | DC single-ended output high voltage |
| V_{OL-DC} | $V_{TTO} - \Delta V_{OCM} - V_{DPP-DC}/2$ | DC single-ended output low voltage |
| V_{OH-PE} | $V_{TTO} - \Delta V_{OCM} + V_{DPP-PE}/2$ | Maximum single-ended output voltage |
| V_{OL-PE} | $V_{TTO} - \Delta V_{OCM} - V_{DPP-PE}/2$ | Minimum single-ended output voltage |
| t_{PE} | Fixed | FFE tap delay |

Table 23. Preemphasis Settings¹

| D2 Res. Code | D2 Current Code | D3 Res. Code | D3 Current Code | Preemphasis (dB) ² | | | | | | | | | | |
|--------------|-----------------|--------------|-----------------|-------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|------------------------|------------------------|------------------------|
| | | | | OLEV 200 ³ | OLEV 300 ³ | OLEV 400 ³ | OLEV 500 ³ | OLEV 600 ³ | OLEV 700 ³ | OLEV 800 ³ | OLEV 900 ³ | OLEV 1000 ³ | OLEV 1100 ³ | OLEV 1200 ³ |
| 11b | 0000b | 11b | 1000b | 1.02 | 0.70 | 0.53 | 0.42 | 0.35 | 0.30 | 0.27 | 0.24 | 0.21 | 0.20 | 0.18 |
| 11b | 0001b | 11b | 1001b | 1.94 | 1.34 | 1.02 | 0.83 | 0.70 | 0.60 | 0.53 | 0.47 | 0.42 | 0.39 | 0.35 |
| 11b | 0010b | 11b | 1010b | 2.77 | 1.94 | 1.49 | 1.21 | 1.02 | 0.88 | 0.78 | 0.70 | 0.63 | 0.57 | 0.53 |
| 11b | 0011b | 11b | 1011b | 3.52 | 2.50 | 1.94 | 1.58 | 1.34 | 1.16 | 1.02 | 0.92 | 0.83 | 0.76 | 0.70 |
| 11b | 0100b | 11b | 1100b | 4.22 | 3.03 | 2.36 | 1.94 | 1.64 | 1.43 | 1.26 | 1.13 | 1.02 | 0.93 | 0.86 |
| 11b | 0101b | 11b | 1101b | 4.86 | 3.52 | 2.77 | 2.28 | 1.94 | 1.69 | 1.49 | 1.34 | 1.21 | 1.11 | 1.02 |
| 11b | 0110b | 11b | 1110b | 5.46 | 3.99 | 3.15 | 2.61 | 2.22 | 1.94 | 1.72 | 1.54 | 1.40 | 1.28 | 1.18 |
| 11b | 0111b | 11b | 1111b | 6.02 | 4.44 | 3.52 | 2.92 | 2.50 | 2.18 | 1.94 | 1.74 | 1.58 | 1.45 | 1.34 |
| 10b | 0100b | 10b | 1100b | 7.04 | 5.26 | 4.22 | 3.52 | 3.03 | 2.65 | 2.36 | 2.13 | 1.94 | 1.78 | 1.64 |
| 10b | 0101b | 10b | 1101b | 7.96 | 6.02 | 4.86 | 4.08 | 3.52 | 3.10 | 2.77 | 2.50 | 2.28 | 2.09 | 1.94 |
| 10b | 0110b | 10b | 1110b | 8.79 | 6.72 | 5.46 | 4.61 | 3.99 | 3.52 | 3.15 | 2.85 | 2.61 | 2.40 | 2.22 |
| 10b | 0111b | 10b | 1111b | 9.54 | 7.36 | 6.02 | 5.11 | 4.44 | 3.93 | 3.52 | 3.19 | 2.92 | 2.69 | 2.50 |
| 01b | 0100b | 01b | 1100b | 10.88 | 8.52 | 7.04 | 6.02 | 5.26 | 4.68 | 4.22 | 3.84 | 3.52 | 3.25 | 3.03 |
| 01b | 0101b | 01b | 1101b | 12.04 | 9.54 | 7.96 | 6.85 | 6.02 | 5.38 | 4.86 | 4.44 | 4.08 | 3.78 | 3.52 ⁴ |
| 01b | 0110b | 01b | 1110b | 13.06 | 10.46 | 8.79 | 7.60 | 6.72 | 6.02 | 5.46 | 5.00 | 4.61 | 4.28 ⁴ | 3.99 ⁴ |
| 01b | 0111b | 01b | 1111b | 13.98 | 11.29 | 9.54 | 8.30 | 7.36 | 6.62 | 6.02 | 5.52 | 5.11 ⁴ | 4.75 ⁴ | 4.44 ⁴ |
| 00b | 0100b | 00b | 1100b | N/A | 12.74 | 10.88 | 9.54 | 8.52 | 7.71 | 7.04 ⁴ | 6.49 ⁴ | 6.02 ⁴ | 5.62 ⁴ | 5.26 ⁴ |
| 00b | 0101b | 00b | 1101b | N/A | 13.98 | 12.04 | 10.63 | 9.54 ⁴ | 8.67 ⁴ | 7.96 ⁴ | 7.36 ⁴ | 6.85 ⁴ | 6.41 ⁴ | 6.02 ⁴ |
| 00b | 0110b | 00b | 1110b | N/A | N/A | 13.06 | 11.60 ⁴ | 10.46 ⁴ | 9.54 ⁴ | 8.79 ⁴ | 8.15 ⁴ | 7.60 ⁴ | 7.13 ⁴ | 6.72 ⁴ |
| 00b | 0111b | 00b | 1111b | N/A | N/A | 13.98 | 12.46 ⁴ | 11.29 ⁴ | 10.33 ⁴ | 9.54 ⁴ | 8.87 ⁴ | 8.30 ⁴ | 7.80 ⁴ | 7.36 ⁴ |

¹ Where N/A appears in this table, it means not applicable.² Preemphasis settings are applicable to both ac-coupled and dc-coupled applications.³ OLEV values of 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, and 1200 are in units of mV p-p differential (see Table 19).⁴ Preemphasis settings require the VTTON or VTTOS supply of 3.3 V to meet output compliance (see the Output Compliance section).Table 24. Deemphasis Settings¹

| D3 Res. Code | D3 Current Code | Deemphasis (dB) ² | | | | | | | | | | |
|--------------|-----------------|------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|------------------------|------------------------|------------------------|
| | | OLEV 200 ³ | OLEV 300 ³ | OLEV 400 ³ | OLEV 500 ³ | OLEV 600 ³ | OLEV 700 ³ | OLEV 800 ³ | OLEV 900 ³ | OLEV 1000 ³ | OLEV 1100 ³ | OLEV 1200 ³ |
| 11b | 1000b | 1.09 | 0.72 | 0.54 | 0.43 | 0.36 | 0.31 | 0.27 | 0.24 | 0.22 | 0.20 | 0.18 |
| 11b | 1001b | 2.18 | 1.45 | 1.09 | 0.87 | 0.72 | 0.62 | 0.54 | 0.48 | 0.43 | 0.39 | 0.36 |
| 11b | 1010b | 3.30 | 2.18 | 1.63 | 1.31 | 1.09 | 0.93 | 0.81 | 0.72 | 0.65 | 0.59 | 0.54 |
| 11b | 1011b | 4.44 | 2.92 | 2.18 | 1.74 | 1.45 | 1.24 | 1.09 | 0.97 | 0.87 | 0.79 | 0.72 |
| 11b | 1100b | N/A | 3.67 | 2.74 | 2.18 | 1.82 | 1.56 | 1.36 | 1.21 | 1.09 | 0.99 | 0.91 |
| 11b | 1101b | N/A | 4.44 | 3.30 | 2.63 | 2.18 | 1.87 | 1.63 | 1.45 | 1.31 | 1.19 | 1.09 |
| 11b | 1110b | N/A | 5.22 | 3.86 | 3.07 | 2.55 | 2.18 | 1.91 | 1.69 | 1.52 | 1.38 | 1.27 |
| 11b | 1111b | N/A | 6.02 | 4.44 | 3.52 | 2.92 | 2.50 | 2.18 | 1.94 | 1.74 | 1.58 | 1.45 |
| 10b | 1100b | N/A | 7.71 | 5.62 | 4.44 | 3.67 | 3.14 | 2.74 | 2.43 | 2.18 | 1.98 | 1.82 |
| 10b | 1101b | N/A | 9.54 | 6.85 | 5.38 | 4.44 | 3.78 | 3.30 | 2.92 | 2.63 | 2.38 | 2.18 |
| 10b | 1110b | N/A | N/A | 8.15 | 6.35 | 5.22 | 4.44 | 3.86 | 3.42 | 3.07 | 2.79 | 2.55 |
| 10b | 1111b | N/A | N/A | 9.54 | 7.36 | 6.02 | 5.11 | 4.44 | 3.93 | 3.52 | 3.19 | 2.92 |
| 01b | 1100b | N/A | N/A | 12.74 | 9.54 | 7.71 | 6.49 | 5.62 | 4.96 | 4.44 | 4.02 | 3.67 |
| 01b | 1101b | N/A | N/A | N/A | 12.04 | 9.54 | 7.96 | 6.85 | 6.02 | 5.38 | 4.86 | 4.44 |
| 01b | 1110b | N/A | N/A | N/A | N/A | 11.60 | 9.54 | 8.15 | 7.13 | 6.35 | 5.73 | 5.22 |
| 01b | 1111b | N/A | N/A | N/A | N/A | 13.98 | 11.29 | 9.54 | 8.30 | 7.36 | 6.62 | 6.02 |
| 00b | 1100b | N/A | N/A | N/A | N/A | N/A | N/A | 12.74 | 10.88 | 9.54 | 8.52 | 7.71 |
| 00b | 1101b | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 13.98 | 12.04 | 10.63 | 9.54 |
| 00b | 1110b | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 13.06 | 11.60 |
| 00b | 1111b | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 13.98 |

¹ Where N/A appears in this table, it means not applicable.² Deemphasis settings are applicable to both ac-coupled and dc-coupled applications.³ OLEV values of 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, and 1200 are in units of mV p-p differential (see Table 19).

PREEMPHASIS/DEEMPHASIS SUPPORT FOR LEGACY RATES

Advancing the position of the first postcursor in the cascading of delay taps from Position D3 to Position D6 lowers the frequency at which the maximum PE boost is delivered, from 6.25 GHz to 1.56 GHz, as shown in Figure 62. A current driver element (D3, D4, D5, or D6) can be configured as the first postcursor tap, allowing the ADN4612 to offer transmit channel preemphasis compensation for legacy applications (6.25 Gbps and slower); see Table 25.

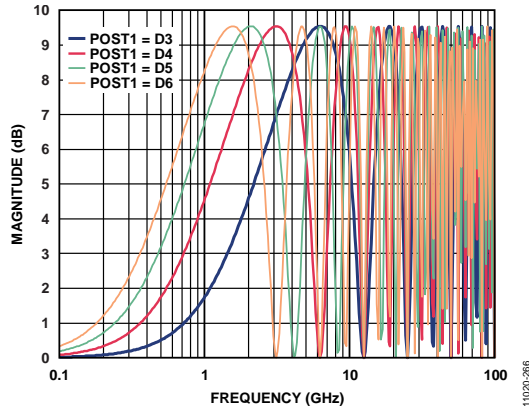


Figure 62. Transmit Gain vs. Frequency for Alternate First Postcursor Taps

Table 25. Alternate First Postcursor Tap Table

| First Postcursor Tap | Maximum Transmit Boost Frequency (GHz) | Maximum Data Rates (Gbps) |
|----------------------|--|---------------------------|
| D3 | 6.25 | 12.5 |
| D4 | 3.125 | 6.25 |
| D5 | 2.0 | 4.0 |
| D6 | 1.5625 | 3.125 |

Table 26. Output Compliance

| Tx Driver Element Code (Hex) | | | | Single-Ended Output Levels and PE Boost | | | | Output Current | AC-Coupled Outputs ¹ | | | | DC-Coupled Outputs ¹ | | | | | |
|------------------------------|----|------------------|------------------|---|-------------------------|--------------|---------|-----------------------|---------------------------------|------------------------|--------------------------|------------------------|---------------------------------|------------------------|--------------------------|------------------------|------------------------|------------------------|
| | | | | | | | | | V _{TTO} = 3.3 V | | V _{TTO} = 2.5 V | | V _{TTO} = 3.3 V | | V _{TTO} = 2.5 V | | | |
| D0 | D1 | D2 | D3 | V _{SW-DC} ² (mV) | V _{SW-PE} (mV) | PE Boost (%) | PE (dB) | I _{TTO} (mA) | ΔV _{OCM} (mV) | V _{OH-PE} (V) | V _{OL-PE} (V) | V _{OH-PE} (V) | V _{OL-PE} (V) | ΔV _{OCM} (mV) | V _{OH-PE} (V) | V _{OL-PE} (V) | V _{OH-PE} (V) | V _{OL-PE} (V) |
| 0 | 0 | N/A ³ | N/A ³ | 100 | 100 | 0.00 | 0.00 | 4 | 100 | 3.25 | 3.15 | 2.45 | 2.35 | 50 | 3.3 | 3.2 | 2.5 | 2.4 |
| 0 | 0 | 1 | 9 | 100 | 300 | 200.00 | 9.54 | 12 | 300 | 3.15 | 2.85 | 2.35 | 2.05 | 150 | 3.3 | 3.0 | 2.5 | 2.2 |
| 0 | 0 | 3 | B | 100 | 500 | 400.00 | 13.98 | 20 | 500 | 3.05 | 2.55 | 2.25 | 1.75 | 250 | 3.3 | 2.8 | 2.5 | 2.0 |
| 1 | 1 | N/A ³ | N/A ³ | 200 | 200 | 0.00 | 0.00 | 8 | 200 | 3.2 | 3.0 | 2.40 | 2.20 | 100 | 3.3 | 3.1 | 2.5 | 2.3 |
| 1 | 1 | 1 | 9 | 200 | 400 | 100.00 | 6.02 | 16 | 400 | 3.1 | 2.7 | 2.30 | 1.90 | 200 | 3.3 | 2.9 | 2.5 | 2.1 |
| 1 | 1 | 3 | B | 200 | 600 | 200.00 | 9.54 | 24 | 600 | 3 | 2.4 | 2.20 | 1.60 | 300 | 3.3 | 2.7 | 2.5 | 1.9 |
| 2 | 2 | N/A ³ | N/A ³ | 300 | 300 | 0.00 | 0.00 | 12 | 300 | 3.15 | 2.85 | 2.35 | 2.05 | 150 | 3.3 | 3.0 | 2.5 | 2.2 |
| 2 | 2 | 1 | 9 | 300 | 500 | 66.67 | 4.44 | 20 | 500 | 3.05 | 2.55 | 2.25 | 1.75 | 250 | 3.3 | 2.8 | 2.5 | 2.0 |
| 2 | 2 | 3 | B | 300 | 700 | 133.33 | 7.36 | 28 | 700 | 2.95 | 2.25 | 2.15 | 1.45 | 350 | 3.3 | 2.6 | 2.5 | 1.8 |
| 3 | 3 | N/A ³ | N/A ³ | 400 | 400 | 0.00 | 0.00 | 16 | 400 | 3.1 | 2.7 | 2.3 | 1.9 | 200 | 3.3 | 2.9 | 2.5 | 2.1 |
| 3 | 3 | 1 | 9 | 400 | 600 | 50.00 | 3.52 | 24 | 600 | 3.0 | 2.4 | 2.2 | 1.6 | 300 | 3.3 | 2.7 | 2.5 | 1.9 |
| 3 | 3 | 3 | B | 400 | 800 | 100.00 | 6.02 | 32 | 800 | 2.9 | 2.1 | 2.1 | 1.3 | 400 | 3.3 | 2.5 | 2.5 | 1.7 |
| 4 | 4 | N/A ³ | N/A ³ | 500 | 500 | 0.00 | 0.00 | 20 | 500 | 3.05 | 2.55 | 2.25 | 1.75 | 250 | 3.3 | 2.8 | 2.5 | 2.0 |
| 4 | 4 | 1 | 9 | 500 | 700 | 40.00 | 2.92 | 28 | 700 | 2.95 | 2.25 | 2.15 | 1.45 | 350 | 3.3 | 2.6 | 2.5 | 1.8 |
| 5 | 5 | N/A ³ | N/A ³ | 600 | 600 | 0.00 | 0.00 | 24 | 600 | 3.0 | 2.4 | 2.2 | 1.6 | 300 | 3.3 | 2.7 | 2.5 | 1.9 |
| 5 | 5 | 1 | 9 | 600 | 800 | 33.33 | 2.50 | 32 | 800 | 2.9 | 2.1 | 2.1 | 1.3 | 400 | 3.3 | 2.5 | 2.5 | 1.7 |

¹ A blank column heading indicates that the values listed are independent of the V_{TTO} level.

² See Table 22 for symbol definitions.

³ N/A means not applicable.

Output Compliance

When operating at a low V_{TTO} supply level and configuring high output swings, pay careful attention to both the differential and common-mode signal levels. The choice of output voltage swing, preemphasis setting, supply voltages (V_{CC} and V_{TTO}), and output coupling (ac or dc) affect peak and settled single-ended voltage swings, and the common-mode shift measured across the output termination resistors.

$$\Delta V_{OCM} = V_{CC} - V_{OCM} = I_{TTO}/2 \times 50 \Omega \text{ (ac-coupled)}$$

$$\Delta V_{OCM} = V_{CC} - V_{OCM} = I_{TTO}/2 \times 25 \Omega \text{ (dc-coupled)}$$

These choices also affect output current and, consequently, power consumption. For certain combinations of supply voltage and output coupling, output voltage swing in combination with precursor and postcursor driver element settings may violate the single-ended absolute output low voltage, as specified in Table 1.

Under these conditions, the performance is degraded; therefore, these settings are not recommended. Table 26 shows the change in the common-mode output (ΔV_{OCM} = V_{CC} - V_{OCM}) with an output level and a preemphasis setting. Single-ended output levels are calculated for V_{TTON} and V_{TTO5} supplies of 3.3 V and 2.5 V to illustrate practical challenges of reducing the supply voltage. The minimum V_{OL} cannot be less than the absolute minimum level specified in Table 1. The minimum V_{OL} level for a given voltage swing can be calculated using the following equations:

$$V_{OL-SE} = V_{TTO} - 0.75 \times V_{DPP-PE} \text{ (ac-coupled)}$$

$$V_{OL-SE} = V_{TTO} - 0.5 \times V_{DPP-PE} \text{ (dc-coupled)}$$

Example 1— $V_{CC} = 2.5\text{ V}$, $V_{TTO} = 2.5\text{ V}$, $PE = 0\text{ dB}$

In a typical application, the user can select a default output level of 400 mV single-ended (800 mV p-p differential) and may want the option to choose preemphasis settings of 0 dB and 9.5 dB. With preemphasis disabled (0 dB), a dc-coupled transmitter causes a 200 mV common-mode shift across the termination resistors, whereas an ac-coupled transmitter causes twice the common-mode shift (400 mV). When dc-coupled, the single-ended output voltage swings between 2.5 V and 2.1 V; and when ac-coupled, it swings between 2.3 V and 1.9 V. In both cases, these levels are greater than the minimum V_{OL} limit of 1.3 V ($V_{OL} = V_{CC} - 1.2\text{ V}$).

Example 2— $V_{CC} = 2.5\text{ V}$, $V_{TTO} = 2.5\text{ V}$ and 3.3 V , $PE = 9.5\text{ dB}$

With a PE setting of 9.5 dB, the ac-coupled transmitter has peak single-ended swings from 1.9 V and 0.7 V, whereas the dc-coupled transmitter outputs swing between 2.5 V and 1.3 V. In the case of the ac-coupled transmitter, the minimum single-ended output voltage (V_{OL-PE}) exceeds the minimum V_{OL} limit of 1.3 V by 600 mV, violating the device specification. Increasing the V_{TTO} supply to 3.3 V shifts the swing levels above the minimum V_{OL} limit by the increase in the V_{TTO} supply level (800 mV). The minimum V_{OL} is then 1.5 V for the ac-coupled case and 2.1 V for the dc-coupled case. This transmitter configuration then complies with the output voltage range specification.

LOAD FROM MEMORY

To enable power-on ready operation and alleviate system controller overhead, the ADN4612 can optionally load its configuration from an external serial EEPROM. All user available registers (except the read only registers) can be automatically loaded using the I²C bus.

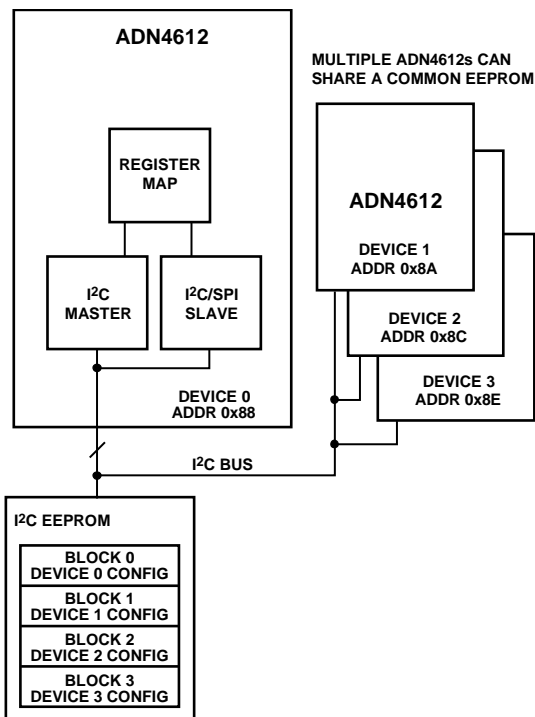


Figure 63. Load from Memory Block Diagram

Enabling Load from Memory

With the $\overline{\text{RESET}}$ pin held at a logic high, the $\overline{\text{EEPROM}}$ pin can be strobed low to enable the load from the memory cycle. $\overline{\text{EEPROM}}$ is level sensitive; therefore, a falling edge transition initiates the load from the EEPROM operation. The $\overline{\text{EEPROM}}$ pin can return to a logic high level before the completion of the load from the memory cycle. Alternatively, holding $\overline{\text{EEPROM}}$ low causes the operation to be transparent. In this scenario, after the ADN4612 is powered up, the load from the EEPROM cycle commences when the $\overline{\text{RESET}}$ pin settles to a logic high.

When a load from the EEPROM is initiated, the SPI/I²C slave interfaces on the ADN4612 are disabled and the ADN4612 I²C master interface is enabled. The SCK/SCL pin provides the I²C master clock and the $\overline{\text{SDO/SDA}}$ pin accepts the I²C input and output data. The $\overline{\text{CS/I}^2\text{C_A0}}$ and $\overline{\text{SDI/I}^2\text{C_A1}}$ pins must be configured to the user defined LSB values of the EEPROM device address to ensure proper device communication.

Load from the Memory Cycle

The ADN4612 reads only the first 225 bytes of the EEPROM. The first 224 bytes represent the contents to be loaded into Register 0x00 to Register 0xDF. Byte 225 contains the checksum stored in the EEPROM.

The ADN4612 calculates the checksum for the first 224 bytes it reads back and compares it to the checksum in the EEPROM. The ADN4612 calculated checksum is accessible by reading the EEPROM checksum register (Register Address 0xEE). If the ADN4612 checksum matches the checksum stored in the EEPROM, the load from the EEPROM was successful. The load from the EEPROM pass or fail status is recorded in the EEPROM status register (Register Address 0xEF).

In addition, the LSB of the EEPROM status register indicates whether the load cycle is complete. Logic 1 represents successful completion of the load cycle. Logic 0 represents the occurrence of a timeout violation during the loading cycle. In the event of a timeout or the successful completion of the load from a memory cycle, the ADN4612 I²C master interface disables, and the ADN4612 slave interface reenables, allowing the user communication access to the device (see Table 6 for EEPROM timing specifications).

SPI Master Control Interface

The load from a memory cycle requires an I²C communication bus between the ADN4612 and the EEPROM device; however, the ADN4612 can still be controlled by the SPI interface after the load from the memory cycle is complete. It is recommended that the $\overline{\text{CS/I}^2\text{C_A0}}$ pin return to logic high after the load from the memory cycle and before the first SPI read or write command. This allows the user to ensure that the proper setup time elapses before the initiation of a SPI read/write command (see Table 5).

Multidevice Load from Memory

The ADN4612 integrated I²C master supports multimaster bus arbitration as outlined in the I²C specification. Therefore, up to four ADN4612 devices can share a common EEPROM to reduce board area and simplify the EEPROM loading process. A system controller can also access the bus, if desired; however, the system controller must adhere to the multimaster specification.

There are multiple ways to initiate the configuration of multiple ADN4612 devices from a single EEPROM device. A system controller can simultaneously generate the falling edge transition for each ADN4612 device EEPROM pin, as shown in Figure 64. If a simultaneous falling edge is detected on all ADN4612 EEPROM pins, the ADN4612 I²C master interfaces begin bus arbitration. The ADN4612 device with the lowest value device address is awarded access to the I²C bus. After the first ADN4612 device completes the load cycle, the next ADN4612 device with the lowest device address begins its load cycle. The process continues until all ADN4612 devices complete the load from memory.

Alternatively, the LOS_IRQ pin from the first ADN4612 device can be used to drive the EEPROM pin for the next ADN4612 device, creating a daisy-chain loading configuration as shown in Figure 65. When a load from the memory cycle is initiated, the LOS_IRQ pin is redefined for the entire cycle. At the start of the cycle, the LOS_IRQ pin is driven to a logic high.

When the I²C master completes the load operation for the given ADN4612 device, a low pulse is generated on the LOS_IRQ pin, which can be used to trigger the load from the memory cycle on the next ADN4612 device. The LOS_IRQ pin cannot be used for LOS detection when used in this configuration.

EEPROM Memory Size and Data Organization

To configure a single ADN4612 device, the EEPROM must contain a memory block that supports a minimum of 256 words, each of eight bits per word. The minimum memory block size must increase to support the configuration of multiple ADN4612 devices. EEPROM devices with a memory capacity of 512 (4k), 1024 (8k), and 2048 (16k) words are typically organized into pages of 256 (2k) word blocks, as shown in Table 27. The ADN4612 configuration data for each device must be allocated to the EEPROM memory within a single word page.

Table 27. Typical EEPROM Memory Capacity

| EEPROM Memory Capacity ¹ | Word Pages | Words/Page ¹ | Word Size (Bits) | ADN4612 Devices Supported |
|-------------------------------------|------------|-------------------------|------------------|---------------------------|
| 256 (2k) | 1 | 256 (2k) | 8 | 1 |
| 512 (4k) | 2 | 256 (2k) | 8 | 2 |
| 1024 (8k) | 3 | 256 (2k) | 8 | 3 |
| 2048 (16k) | 4 | 256 (2k) | 8 | 4 |

¹ k represents kwords.

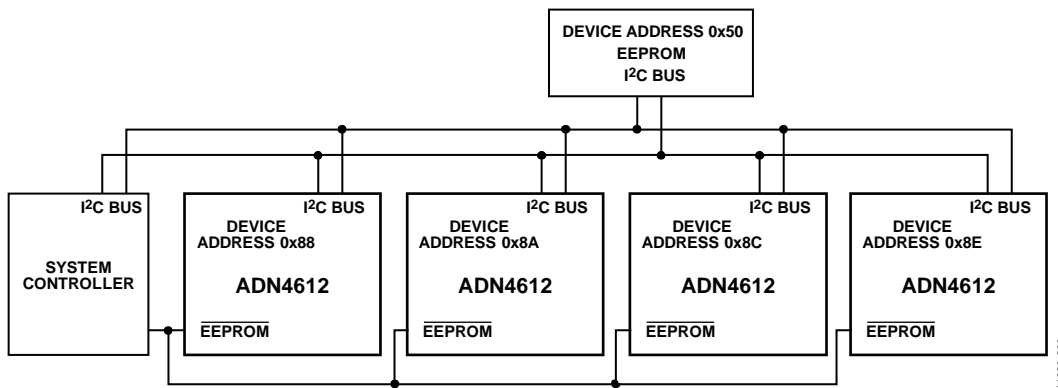


Figure 64. Multidevice Load from Memory (Basic Configuration) Block Diagram

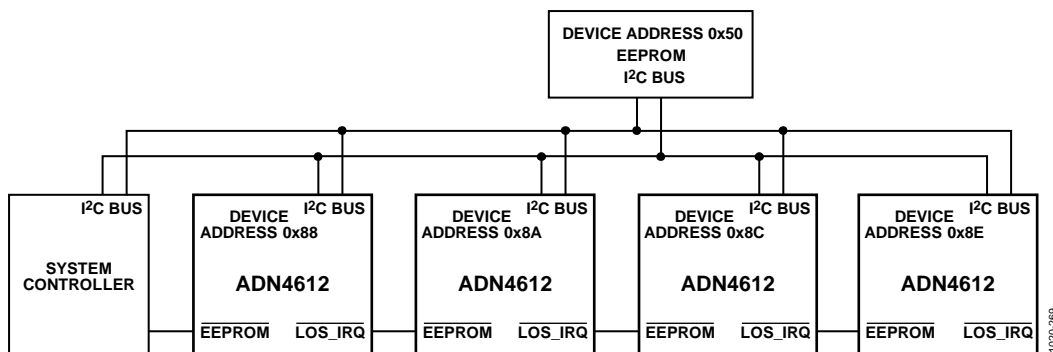


Figure 65. Multidevice Load from Memory (Daisy-Chain Configuration) Block Diagram

When the load from the memory cycle is initiated, the ADN4612 I²C master performs 225 continuous I²C reads starting at EEPROM Word Address 0x0. The word address automatically increments by 1 for each consecutive read. The first 224 bytes represent the content to be loaded into Register Address 0x00 to Register Address 0xDF. The contents of Byte 225 contain the checksum stored in the EEPROM.

The ADN4612 LSB device address information sent during communication determines the appropriate EEPROM word page address that contains the contents to be loaded for the given ADN4612 device (see Table 28).

Table 28. I²C Device and EEPROM Page Address

| I ² C_A1 (Binary) | I ² C_A0 (Binary) | I ² C Device Address (Binary) | EEPROM Word Page (Binary) |
|------------------------------|------------------------------|--|---------------------------|
| 0 | 0 | 1000100 | 00 |
| 0 | 1 | 1000101 | 01 |
| 1 | 0 | 1000110 | 10 |
| 1 | 1 | 1000111 | 11 |

Table 29 provides an example for allocating EEPROM word memory to configure four ADN4612 devices.

Table 29. EEPROM Memory Allocation for Multiple ADN4612 Devices

| EEPROM Word Page | EEPROM Word Address | EEPROM Data Content | |
|------------------|---------------------|---|---|
| 00 | 000 | ADN4612 Device 1 register data for Register Address 0x0 | |
| | 001 | ADN4612 Device 1 register data for Register Address 0x1 | |
| | ... | ... | |
| | 225 | EEPROM checksum for ADN4612 Device 1 | |
| | 01 | 000 | ADN4612 Device 2 register data for Register Address 0x0 |
| 01 | 001 | ADN4612 Device 2 register data for Register Address 0x1 | |
| | ... | ... | |
| | 225 | EEPROM checksum for ADN4612 Device 2 | |
| | 02 | 000 | ADN4612 Device 3 register data for Register Address 0x0 |
| | 02 | 001 | ADN4612 Device 3 register data for Register Address 0x1 |
| ... | | ... | |
| 225 | | EEPROM checksum for ADN4612 Device 3 | |
| 03 | | 000 | ADN4612 Device 4 register data for Register Address 0x0 |
| 03 | | 001 | ADN4612 Device 4 register data for Register Address 0x1 |
| | ... | ... | |
| | 225 | EEPROM checksum for ADN4612 Device 4 | |

I²C SERIAL CONTROL INTERFACE

The ADN4612 register set is controlled through a 2-wire I²C interface. To access the I²C serial interface, hold the SPI/I²C pin at logic low. The ADN4612 I²C interface can be run in the standard mode (100 kHz) and fast mode (400 kHz). The SDA line changes value only when the SCL pin (SCK/SCL) is low, with two exceptions:

- To indicate the beginning or continuation of a transfer, the SDA pin is driven low while the SCL pin is high.
- To indicate the end of a transfer, the SDA line is driven high while the SCL line is high.

Therefore, it is important to control the SCL clock to toggle only when the SDA line is stable unless indicating a start, repeated start, or stop condition.

To establish I²C communication with the ADN4612, the I²C address lines (I²C_A1 and I²C_A0) must be configured to the user assigned I²C device address, as shown in Table 30.

Table 30. Example of I²C Device Address Assignment

| I ² C_A1 (Binary) | I ² C_A0 (Binary) | I ² C Device Address (Binary) |
|------------------------------|------------------------------|--|
| 0 | 0 | 1000100 |
| 0 | 1 | 1000101 |
| 1 | 0 | 1000110 |
| 1 | 1 | 1000111 |

I²C DATA WRITE

To write data to the ADN4612 register set, a microcontroller or any other I²C master must send the appropriate control signals to the ADN4612 slave device. The signals are controlled by the I²C master, unless otherwise noted (see Figure 66). The list of required steps follows:

1. Send a start condition (while holding the SCL line high and pulling the SDA line low).
2. Send the ADN4612 device address (seven bits), whose bits are controlled by the I²C_A1 and I²C_A0 input pin functions (SDI/I²C_A1 and $\overline{\text{CS}}$ /I²C_A0 pins). This transfer is MSB first.
3. Send the write indicator bit, which is set to 0.
4. Wait for the ADN4612 to acknowledge (ACK) the request.
5. Send the register address (eight bits) to which the data is to be written. This transfer is MSB first.
6. Wait for the ADN4612 to acknowledge (ACK) the request.
7. Send the data (eight bits) to be written to the register address that was set in Step 5. This transfer is MSB first.
8. Wait for the ADN4612 to acknowledge (ACK) the request.
9. Perform one or more of the following steps:
 - a. Send a stop condition (while holding the SCL line high and pulling the SDA line high), and release control of the bus.
 - b. Send a repeated start condition (while holding the SCL line high and pulling the SDA line low), and continue with Step 2 of the write procedure (see the I²C Data Write section) to perform a write.
 - c. Send a repeated start condition (while holding the SCL line high and pulling the SDA line low), and continue with Step 2 of this procedure to perform a read from another address.
 - d. Return to Step 7 and continue to write to the next sequential register address.

The ADN4612 write process is shown in Figure 66. The SCL signal is shown, along with a general write operation and a specific example. Note that the SDA line changes only when the SCL line is low, except when sending a start, stop, or repeated start condition (Step 1 and Step 9 in this example).

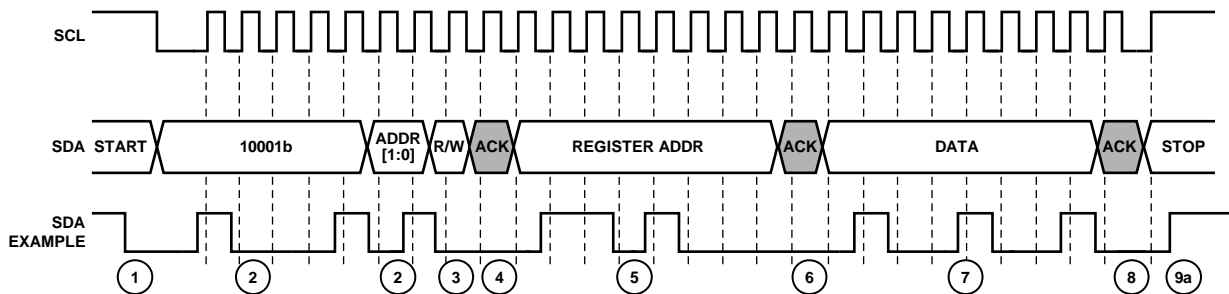


Figure 66. I²C Write Diagram

I²C DATA READ

To read data from the ADN4612 register set, a microcontroller or any other I²C master must send the appropriate control signals to the ADN4612 slave device. The signals are controlled by the I²C master, unless otherwise specified (see Figure 67). The list of required steps follows:

1. Send a start condition (while holding the SCL line high and pulling the SDA line low).
2. Send the ADN4612 device address (seven bits), whose bits are controlled by the I²C_A1 and I²C_A0 input pins. This transfer is MSB first.
3. Send the write indicator bit, which is set to 0.
4. Wait for the ADN4612 to acknowledge (A) the request.
5. Send the register address (eight bits) from which data is to be read. This transfer is MSB first. The register address is kept in the memory of the ADN4612 until the part is reset or the register address is written over with the same procedure (Step 1 to Step 6).
6. Wait for the ADN4612 to acknowledge (A) the request.
7. Send a repeated start condition (while holding the SCL line high and pulling the SDA line low).
8. Send the ADN4612 device address (seven bits) whose bits are controlled by the I²C_A1 and I²C_A0 input pins. This transfer is MSB first.
9. Send the read indicator bit, which is set to 1.
10. Wait for the ADN4612 to acknowledge (A) the request.
11. The ADN4612 then serially transfers the data (eight bits) held in the register indicated by the address set in Step 5.
12. Acknowledge (A) the data.

13. Perform one or more of the following:
 - a. Send a stop condition (while holding the SCL line high and pulling the SDA line high), and release control of the bus.
 - b. Send a repeated start condition (while holding the SCL line high and pulling the SDA line low), and continue with Step 2 of the write procedure (see the I²C Data Write section) to perform a write.
 - c. Send a repeated start condition (while holding the SCL line high and pulling the SDA line low), and continue with Step 2 of this procedure to perform a read from another address.
 - d. Return to Step 11 and continue to read from the next sequential register address.

See Figure 67 for the read process of the ADN4612. The SCL signal is shown, along with a general read operation and a specific example.

In Figure 67, the corresponding step numbers are shown in the circles located under the waveform. The SCL line is driven by the I²C master and never by the ADN4612 slave. As for the SDA line, the data in the shaded polygons is driven by the ADN4612, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case that is shown in Figure 67 is that of Step 13a.

Note that the SDA line changes only when the SCL line is low, except when sending a start, stop, or repeated start condition, as in Step 1, Step 7, and Step 13. In Figure 67, A represents an acknowledge, and Sr represents a repeated start. A repeated start is where the SDA line is brought high before SCL is raised, and then SDA is dropped while SCL is still high.

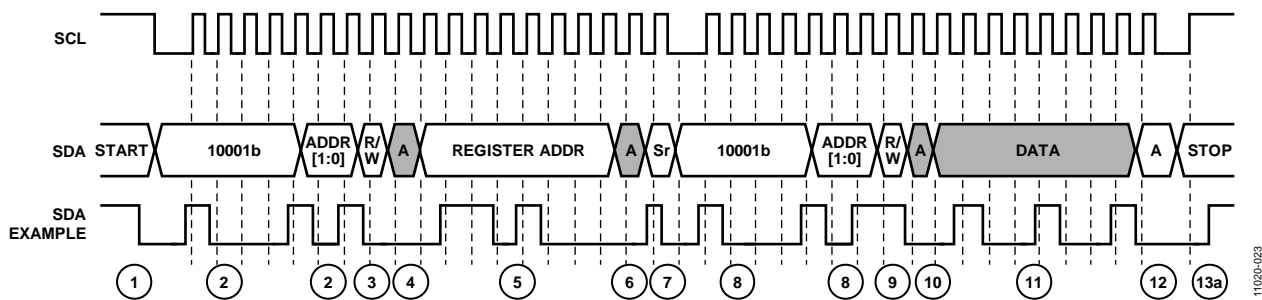


Figure 67. I²C Read Diagram

11020-023

SPI SERIAL CONTROL INTERFACE

The SPI serial interface of the ADN4612 consists of the following four wires: \overline{CS} , SCK, SDI, and SDO. To access the SPI, the SPI/I²C pin must be held at logic high. The \overline{CS} pin (\overline{CS}/I^2C_A0) selects the device when more than one device is connected to the serial clock and data lines. When in SPI control mode, \overline{CS} must be held at logic low to enable write/read capability to the device.

SCK clocks data in and out of the part. The SDI line writes to the registers, and the SDO line reads data back from the registers. Data on the SDI line is clocked on the rising edge of SCK, and data on SDO changes on the falling edge of SCK.

The device operates in slave mode and requires an externally applied serial clock to the SCK input. The design of the serial interface allows the device to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

There are two types of serial operations: read and write. Command words are used to distinguish between a read operation and a write operation (see Table 31).

Table 31. SPI Command Words

| Serial Operation | Command Word |
|------------------|-------------------|
| Write | 0x02 (0000 0010b) |
| Read | 0x03 (0000 0011b) |

WRITE OPERATION

Figure 68 shows a write operation to the ADN4612. Data is clocked into the registers on the rising edge of SCK. When the \overline{CS} line is high, the SDI and SDO lines are in three-state mode. Only when the \overline{CS} pin goes from a high to low logic state does the device accept any data on the SDI line. The 8-bit write command must precede the register address byte. The register address byte is then followed by the data byte, as shown in Figure 68.

To allow continuous writes, the address pointer register auto-increments by 1 without having to load the address pointer register each time. Subsequent data bytes are written into sequential registers. Note that not all registers in the 256-byte address space exist, and not all registers can be written to. Enter 0s for nonexistent address fields when implementing a continuous write operation. Address 0xDD to Address 0xFF are reserved; do not overwrite these addresses.

READ OPERATION

To read back from a register, first send the read command, followed by the desired register address (see Figure 69). Subsequent clock cycles, with \overline{CS} asserted low, stream data starting from the desired register address onto SDO, MSB first. SDO changes on the falling edge of SCK. Multiple data reads are possible in SPI interface mode because the address pointer register is auto-incremented.

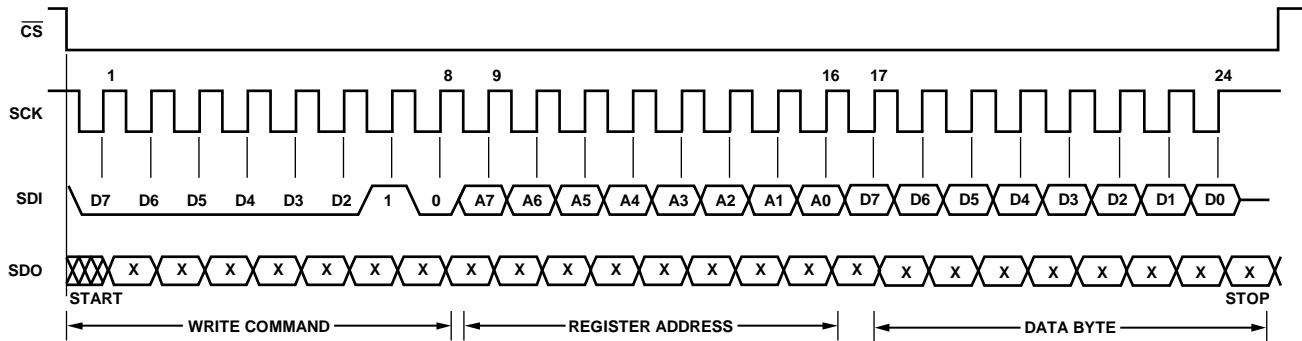


Figure 68. SPI—Writing to the Address Pointer Register, Followed by a Single Byte of Data to the Selected Register

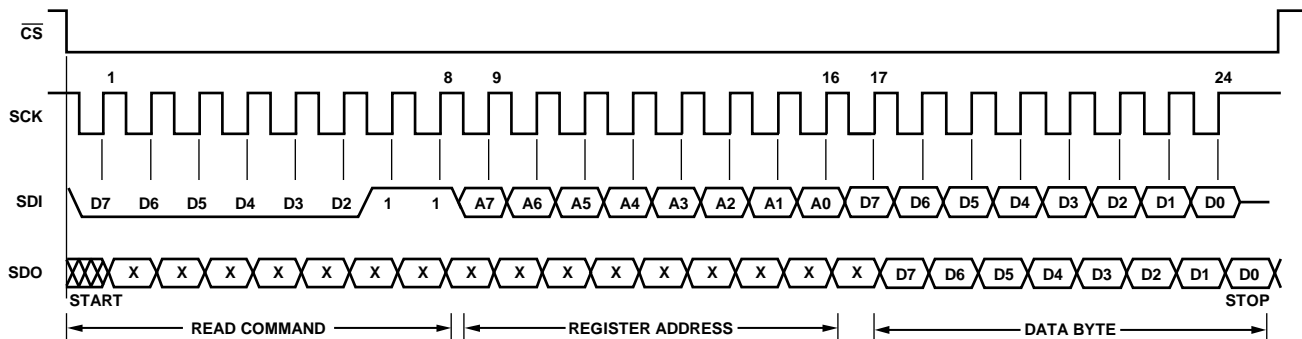


Figure 69. SPI—Reading a Single Byte of Data from a Selected Register

APPLICATIONS INFORMATION

The ADN4612 is an asynchronous and protocol-agnostic digital switch and, therefore, is applicable to a wide range of applications including network routing, redundancy switching, and data storage network switching.

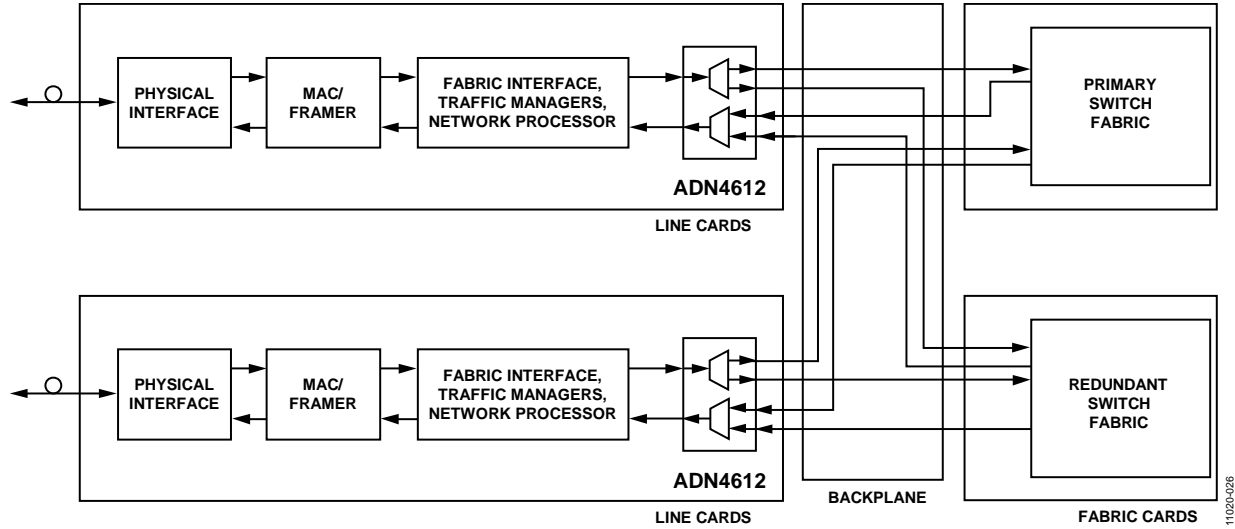


Figure 70. Using the ADN4612 for Switch Redundancy

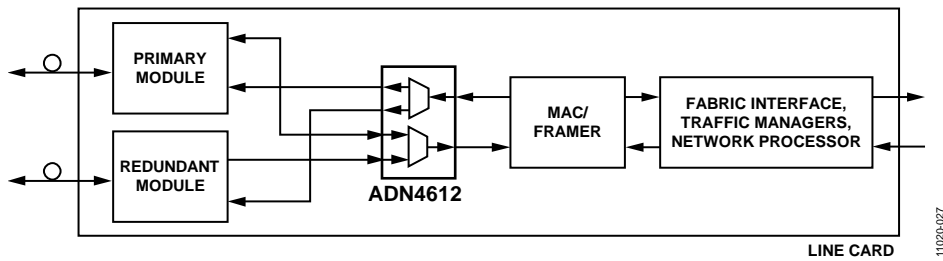


Figure 71. Using the ADN4612 for Module Redundancy

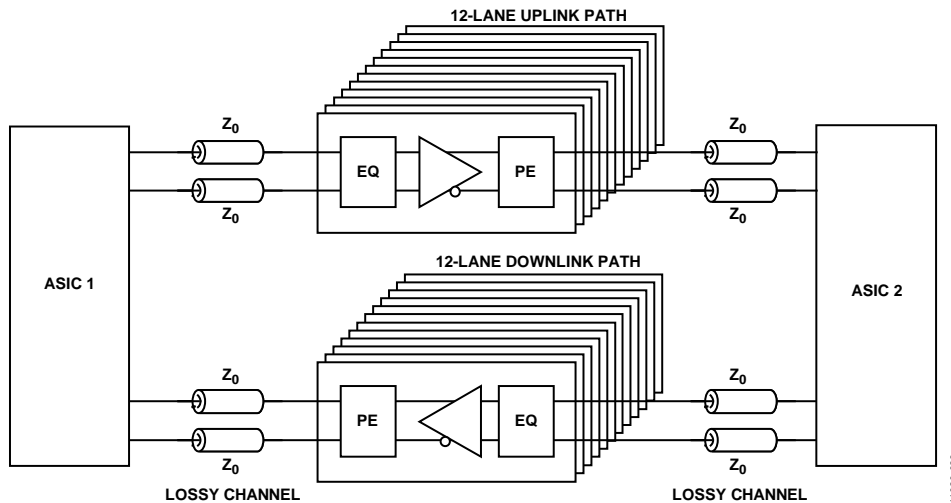


Figure 72. Using the ADN4612 for Signal Conditioning

APPLICATIONS CIRCUIT

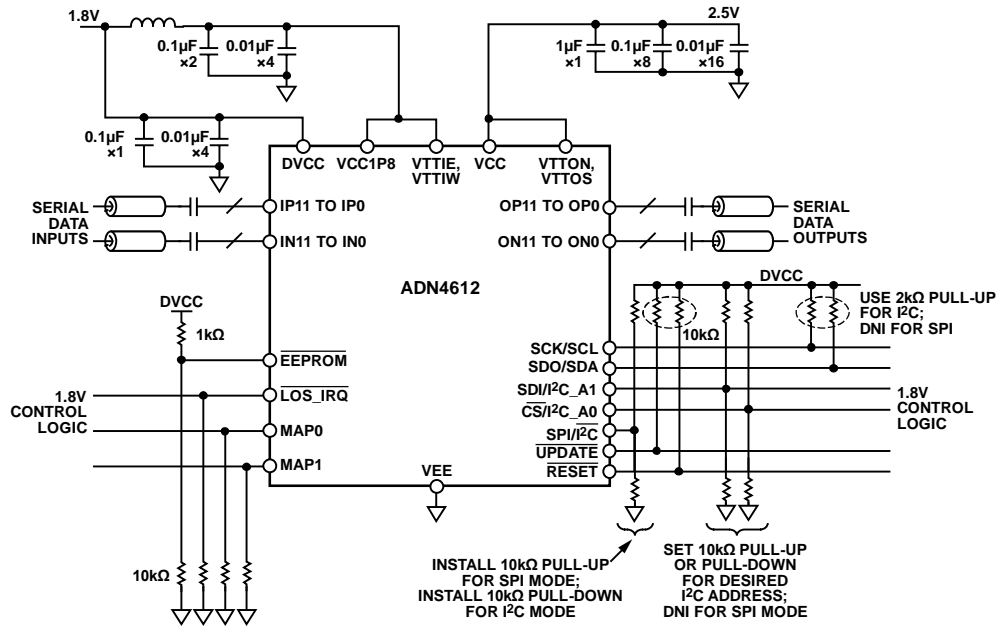


Figure 73. Applications Circuit

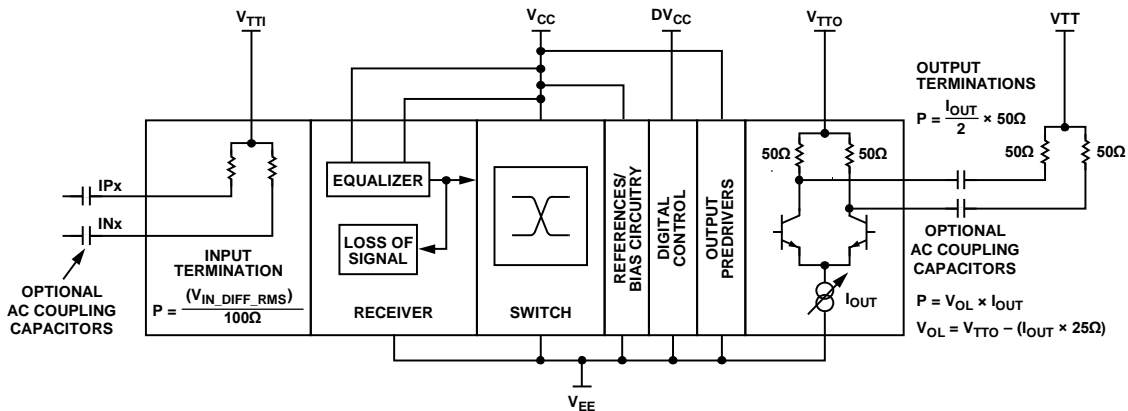


Figure 74. Power Distribution Block Diagram

POWER CONSUMPTION

Several sections of the ADN4612 draw varying power levels, depending on the supply voltages, the type of I/O coupling, and the status of the ADN4612 configuration. Figure 74 shows a block diagram of these sections.

The first section consists of the input termination resistors. The power dissipated in the termination resistors is due to the input differential swing and any common-mode current resulting from dc coupling the input.

In the next section (the receiver section), each input is powered only when it is enabled. If a receiver is disabled, it powers down. Thus, the total number of active inputs affects the total power consumption. Furthermore, the LOS detection circuits can be disabled independent of the receiver for even greater power savings.

The core of the device performs the crosspoint switching functions. It draws a fixed quiescent current of 2 mA when the ADN4612 is powered from VCC to VEE. The switch draws an additional 6 mA per lane when an input-to-output connection path is enabled. The switch core can be disabled on a per lane basis or, to save power, it can be disabled globally by programming the outputs to connect to an input value that is greater than eleven.

An output predriver section draws a current, IPRED, that is related to the programmed output current, IOUT. The IPRED current always flows from VCC to VEE. It is treated separately from the output IOUT current, which flows from VTT; VTT may not be the same voltage as VCC.

The final section is the outputs section. For an individual output, the programmed output current flows through two separate paths. One is the on-chip termination resistor, and the other is the transmission line and the destination termination resistor.

The nominal parallel impedance of these two paths is 25 Ω . The sum of these two currents flows through the switches and the current source of the ADN4612 output circuit and then out through V_{EE} . The power dissipated in the transmission line and the destination resistor is not dissipated in the ADN4612; however, it must be supplied from the power supply, and it is a factor in the overall system power. The current in the on-chip termination resistors and the output current source dissipate power in the ADN4612.

Outputs

The output current is set by a combination of the output level and preemphasis settings (see Table 26). For two logic switch states, this current flows through an on-chip termination resistor and a parallel path to the destination device and its termination resistor. The power in this parallel path is not dissipated by the ADN4612. With preemphasis enabled, some current always flows in both the P and N termination resistors. This preemphasis current gives rise to an output common-mode shift that varies with ac coupling or dc coupling, which can be calculated using the formulas listed in the Output Compliance section.

Perhaps the most direct method for calculating power dissipated in the output is to calculate the power that would be dissipated if all I_{TTO} were to flow on-die from V_{TTO} to V_{EE} , and then to subtract from this the power dissipated off-die in the destination device termination resistors and the channel. For this purpose, the destination device and channel can be modeled as 50 Ω load resistors, R_L , in parallel with the ADN4612 termination resistors.

Power Saving Considerations

Although the ADN4612 power consumption is very low when compared to similar devices, careful control of its operating conditions can yield still greater power savings.

Significant power reduction is realized by disabling unused transmitters; this can be done on a static basis, if the output is not used; or on a dynamic basis, if the output does not have a constant stream of traffic. On transmit disable, both the predriver and output switch currents are disabled. The LOS activated squelch disables only the output switch current, I_{TTO} . Superior power savings is achieved by using the Tx enable control registers (Register Address 0x02 and Register Address 0x03) and Rx enable control registers (Register Address 0x86 and Register Address 0x96) to turn off an unused lane rather than relying on the ADN4612 transmit squelch feature.

Because the majority of the power dissipated is in the output stage, the wide range of transmitter settings can be used to optimize the power consumption. First, the output current and output preemphasis settings can be programmed to the smallest amount required to maintain bit error rate (BER) performance. If an output is driving a short trace length and the downstream receiver device has good sensitivity, a lower output current can be used.

To lower the power dissipation, the voltage on V_{TTO} can be lowered. The amount that V_{TTO} can be lowered is dependent on the lowest of all the V_{OL} and V_{CC} outputs; this is determined by the output that is operating at the highest programmed output current.

Table 26 lists a subset of expected output (V_{OH} and V_{OL}) levels for various configurations of output swing, preemphasis V_{TTO} voltage, and I/O coupling configurations. Ensure that the minimum allowable V_{OL} limit provided in Table 1 is not exceeded.

Power Supply Sequencing

The general guidelines for power supply sequencing are as follows:

- $V_{CC} > DV_{CC}$
- $V_{CC} \geq V_{TTI}$
- $DV_{CC} = V_{CC1P8}$

In applications where alternate termination voltages at V_{TTI} and V_{TTO} are used, adhere to these sequence guidelines. However, in a typical ac-coupled application where $V_{CC} = V_{TTO} = 2.5$ V and $DV_{CC} = V_{CC1P8} = V_{TTI} = 1.8$ V, the recommended power-up sequence is 2.5 V first and 1.8 V second. During power down, power down 1.8 V first, and then power down 2.5 V.

Reset

On initial power-up, or at any point during operation, the ADN4612 registers can be restored to their default values by strobing the RESET pin low according to the control logic timing specification in Table 7. During normal operation, the RESET pin must be pulled up to DV_{CC} . A software reset is also available by writing 0x01 to the reset register at Register Address 0x00. This is a write only register.

PRINTED CIRCUIT BOARD (PCB) LAYOUT GUIDELINES

Route the high speed differential inputs and outputs with 100 Ω controlled impedance differential transmission lines. Reference the transmission lines, either microstrip or stripline, to a solid low impedance reference plane. An example of a PCB cross-section is shown in Figure 75. The trace width (W), differential spacing (S), height above reference plane (H), and dielectric constant of the PCB material determine the characteristic impedance. To minimize crosstalk, keep adjacent channels apart by a distance that is greater than three trace widths (3W).

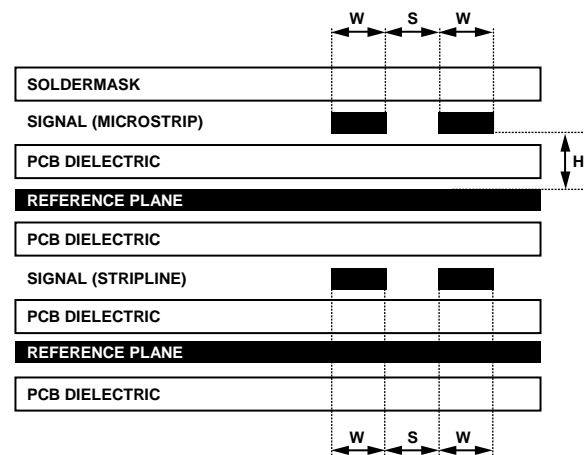


Figure 75. Example of a PCB Cross-Section

11020-278

Although minimizing the use of vias is recommended, vias may be required to route the transmission lines through multiple signal layers of the PCB. Make careful design considerations to minimize the transmission line impedance discontinuity created by the via structure. Blind or buried via design elements can be used to eliminate via stubs, which are created when the via structure continues past the connection point to the internal signal layer. The process of via back drilling is also recommended as a method of removing via stubs.

Thermal Pad Design

The LFCSP is designed with an exposed thermal pad to conduct heat away from the package and into the PCB. By incorporating thermal vias into the PCB thermal pad, heat is dissipated more effectively into the inner metal layers of the PCB. To ensure device performance at elevated temperatures, it is important to have a sufficient number of thermal vias incorporated into the design. An insufficient number of thermal vias results in a θ_{JA} value that is larger than specified in Table 2.

Additional PCB footprint and assembly guidelines are described in the [AN-772 Application Note, A Design and Manufacturing Guide for the Lead Frame Chip Scale Package \(LFCSP\)](#).

Use a via array of 4×4 or 5×5 , with a diameter of 0.3 mm to 0.33 mm, to set a pitch between 1.0 mm and 1.2 mm. See Figure 76 for a representation of these arrays.

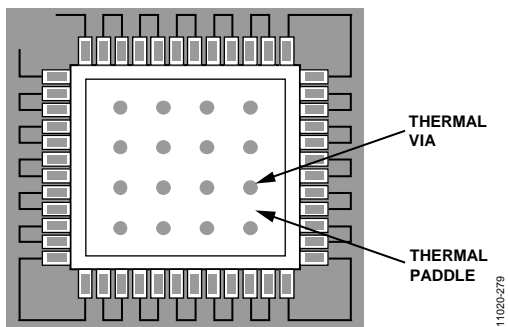


Figure 76. PCB Thermal Pad and Via

Stencil Design for the Thermal Pad

To effectively remove heat from the package and enhance electrical performance, the thermal pad must be soldered (bonded) to the PCB thermal pad, preferably with minimum voids. However, eliminating voids may not be possible because of the presence of thermal vias and the large size of the thermal pad for larger size packages. In addition, outgassing during the reflow process may cause defects (splatter, solder balling) if the solder paste coverage is too big. Use smaller, multiple openings in the stencil rather than one big opening for printing solder paste on the thermal pad region. This method typically results in 50% to 80% solder paste coverage. Figure 77 shows how to achieve these levels of coverage.

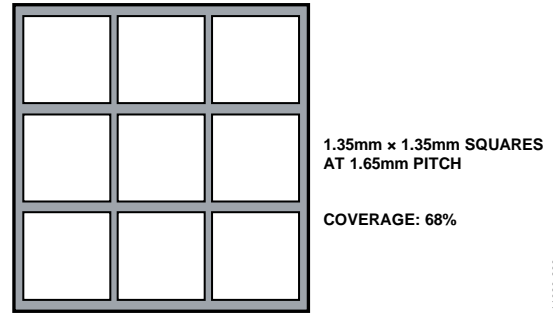


Figure 77. Typical Thermal Pad Stencil Design

Voids within solder joints under the exposed pad can have an adverse effect on high speed and RF applications, as well as on thermal performance. Because the LFCSP package incorporates a large center pad, controlling solder voiding within this region can be difficult. Voids within this ground plane can increase the current path of the circuit. The maximum size for a void must be less than the via pitch within the plane to ensure that any one via is not rendered ineffectual when any void increases the current path beyond the distance to the next available via.

Avoid large voids in the thermal pad area. To control voids in the thermal pad area, solder masking may be required for thermal vias to prevent solder wicking inside the via during reflow, thus displacing the solder away from the interface between the package thermal pad and the thermal pad land on the PCB. There are several methods employed for this purpose, such as via tenting (top or bottom side), using dry film solder mask, via plugging with liquid photoimageable (LPI) solder mask from the bottom side, or via encroaching (see Figure 78). When via tenting is used, ensure that the solder mask diameter is 100 microns larger than the via diameter.

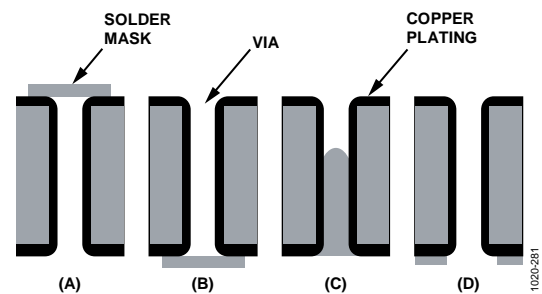


Figure 78. Solder Mask Options for Thermal Vias: (A) Via Tenting from the Top, (B) Via Tenting from the Bottom, (C) Via Plugging from the Bottom, and (D) Via Encroaching from the Bottom

A stencil thickness of 0.125 mm is recommended for 0.4 mm and 0.5 mm pitch parts. The stencil thickness can be increased to 0.15 mm to 0.2 mm for coarser pitch parts. A laser cut, stainless steel stencil is recommended, with electropolished trapezoidal walls to improve the paste release. Because not enough space is available underneath the part after reflow, use a no clean, Type 3 paste for mounting the LFCSP. Inert atmosphere is also recommended during reflow.

REGISTER MAP

Table 32. Register Summary

| Reg (Hex) | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW | | | | | |
|-----------|--------------------|-------|---------------|-------------|---------------|-------------|---------------|-------------|---------------|-----------|-----------|-----------------------|-----------|----------|----------|------|----|
| 0x00 | Soft_Reset | [7:0] | UNUSED_00 | | | | | | | | | SOFT_RESET | 0x00 | W | | | |
| 0x02 | Tx_Enable_7to0 | [7:0] | TXEN7 | TXEN6 | TXEN5 | TXEN4 | TXEN3 | TXEN2 | TXEN1 | TXEN0 | 0x00 | RW | | | | | |
| 0x03 | Tx_Enable_11to8 | [7:0] | UNUSED_03 | | | | | | | | | TXEN_11 | TXEN_10 | TXEN_9 | TXEN_8 | 0x00 | RW |
| 0x04 | Tx_Ref_En | [7:0] | UNUSED_04 | | | TX11AND10EN | TX9AND8EN | TX7AND6EN | TX5AND4EN | TX3AND2EN | TX1AND0EN | 0x3F | RW | | | | |
| 0x05 | Tx_Squelch_Control | [7:0] | UNUSED_05 | | | | | | | | | GLOBAL_SQUELCH_ENABLE | 0x00 | RW | | | |
| 0x08 | Rx7to0_Sign | [7:0] | RX7_SIGN | RX6_SIGN | RX5_SIGN | RX4_SIGN | RX3_SIGN | RX2_SIGN | RX1_SIGN | RX0_SIGN | 0x00 | RW | | | | | |
| 0x09 | Rx11to8_Sign | [7:0] | UNUSED_09 | | | | | | | | | RX11_SIGN | RX10_SIGN | RX9_SIGN | RX8_SIGN | 0x00 | RW |
| 0x0A | Tx7to0_Sign | [7:0] | TX7_SIGN | TX6_SIGN | TX5_SIGN | TX4_SIGN | TX3_SIGN | TX2_SIGN | TX1_SIGN | TX0_SIGN | 0x00 | RW | | | | | |
| 0x0B | Tx11to8_Sign | [7:0] | UNUSED_0B | | | | | | | | | TX11_SIGN | TX10_SIGN | TX9_SIGN | TX8_SIGN | 0x00 | RW |
| 0x0F | XPT_Broadcast | [7:0] | UNUSED_0F | | | | | | | | | XPT_BROADCAST | | 0x00 | RW | | |
| 0x20 | Tx0DrvCtrl0 | [7:0] | TX0_D0_SIGN | TX0_D0_OLEV | | | TX0_PC_SIGN | TX0_PC_OLEV | | | 0x30 | RW | | | | | |
| 0x21 | Tx0DrvCtrl1 | [7:0] | TX0_D2_SIGN | TX0_D2_OLEV | | | TX0_D1_SIGN | TX0_D1_OLEV | | | 0x33 | RW | | | | | |
| 0x22 | Tx0DrvCtrl2 | [7:0] | TX0_D4_SIGN | TX0_D4_OLEV | | | TX0_D3_SIGN | TX0_D3_OLEV | | | 0x0B | RW | | | | | |
| 0x23 | Tx0DrvCtrl3 | [7:0] | TX0_D6_SIGN | TX0_D6_OLEV | | | TX0_D5_SIGN | TX0_D5_OLEV | | | 0x00 | RW | | | | | |
| 0x24 | Tx0DrvEn0 | [7:0] | TX0_D2_DRV_EN | | TX0_D1_DRV_EN | | TX0_D0_DRV_EN | | TX0_PC_DRV_EN | | | 0x3C | RW | | | | |
| 0x25 | Tx0DrvEn1 | [7:0] | TX0_D6_DRV_EN | | TX0_D5_DRV_EN | | TX0_D4_DRV_EN | | TX0_D3_DRV_EN | | | 0x00 | RW | | | | |
| 0x26 | Tx0DrvRes0 | [7:0] | TX0_D2_RES | | TX0_D1_RES | | TX0_D0_RES | | TX0_PC_RES | | | 0x00 | RW | | | | |
| 0x27 | Tx0DrvRes1 | [7:0] | TX0_D6_RES | | TX0_D5_RES | | TX0_D4_RES | | TX0_D3_RES | | | 0x54 | RW | | | | |
| 0x28 | Tx1DrvCtrl0 | [7:0] | TX1_D0_SIGN | TX1_D0_OLEV | | | TX1_PC_SIGN | TX1_PC_OLEV | | | 0x30 | RW | | | | | |
| 0x29 | Tx1DrvCtrl1 | [7:0] | TX1_D2_SIGN | TX1_D2_OLEV | | | TX1_D1_SIGN | TX1_D1_OLEV | | | 0x33 | RW | | | | | |
| 0x2A | Tx1DrvCtrl2 | [7:0] | TX1_D4_SIGN | TX1_D4_OLEV | | | TX1_D3_SIGN | TX1_D3_OLEV | | | 0x0B | RW | | | | | |
| 0x2B | Tx1DrvCtrl3 | [7:0] | TX1_D6_SIGN | TX1_D6_OLEV | | | TX1_D5_SIGN | TX1_D5_OLEV | | | 0x00 | RW | | | | | |
| 0x2C | Tx1DrvEn0 | [7:0] | TX1_D2_DRV_EN | | TX1_D1_DRV_EN | | TX1_D0_DRV_EN | | TX1_PC_DRV_EN | | | 0x3C | RW | | | | |
| 0x2D | Tx1DrvEn1 | [7:0] | TX1_D6_DRV_EN | | TX1_D5_DRV_EN | | TX1_D4_DRV_EN | | TX1_D3_DRV_EN | | | 0x00 | RW | | | | |
| 0x2E | Tx1DrvRes0 | [7:0] | TX1_D2_RES | | TX1_D1_RES | | TX1_D0_RES | | TX1_PC_RES | | | 0x00 | RW | | | | |
| 0x2F | Tx1DrvRes1 | [7:0] | TX1_D6_RES | | TX1_D5_RES | | TX1_D4_RES | | TX1_D3_RES | | | 0x54 | RW | | | | |
| 0x30 | Tx2DrvCtrl0 | [7:0] | TX2_D0_SIGN | TX2_D0_OLEV | | | TX2_PC_SIGN | TX2_PC_OLEV | | | 0x30 | RW | | | | | |
| 0x31 | Tx2DrvCtrl1 | [7:0] | TX2_D2_SIGN | TX2_D2_OLEV | | | TX2_D1_SIGN | TX2_D1_OLEV | | | 0x33 | RW | | | | | |
| 0x32 | Tx2DrvCtrl2 | [7:0] | TX2_D4_SIGN | TX2_D4_OLEV | | | TX2_D3_SIGN | TX2_D3_OLEV | | | 0x0B | RW | | | | | |
| 0x33 | Tx2DrvCtrl3 | [7:0] | TX2_D6_SIGN | TX2_D6_OLEV | | | TX2_D5_SIGN | TX2_D5_OLEV | | | 0x00 | RW | | | | | |
| 0x34 | Tx2DrvEn0 | [7:0] | TX2_D2_DRV_EN | | TX2_D1_DRV_EN | | TX2_D0_DRV_EN | | TX2_PC_DRV_EN | | | 0x3C | RW | | | | |
| 0x35 | Tx2DrvEn1 | [7:0] | TX2_D6_DRV_EN | | TX2_D5_DRV_EN | | TX2_D4_DRV_EN | | TX2_D3_DRV_EN | | | 0x00 | RW | | | | |
| 0x36 | Tx2DrvRes0 | [7:0] | TX2_D2_RES | | TX2_D1_RES | | TX2_D0_RES | | TX2_PC_RES | | | 0x00 | RW | | | | |
| 0x37 | Tx2DrvRes1 | [7:0] | TX2_D6_RES | | TX2_D5_RES | | TX2_D4_RES | | TX2_D3_RES | | | 0x54 | RW | | | | |
| 0x38 | Tx3DrvCtrl0 | [7:0] | TX3_D0_SIGN | TX3_D0_OLEV | | | TX3_PC_SIGN | TX3_PC_OLEV | | | 0x30 | RW | | | | | |
| 0x39 | Tx3DrvCtrl1 | [7:0] | TX3_D2_SIGN | TX3_D2_OLEV | | | TX3_D1_SIGN | TX3_D1_OLEV | | | 0x33 | RW | | | | | |
| 0x3A | Tx3DrvCtrl2 | [7:0] | TX3_D4_SIGN | TX3_D4_OLEV | | | TX3_D3_SIGN | TX3_D3_OLEV | | | 0x0B | RW | | | | | |
| 0x3B | Tx3DrvCtrl3 | [7:0] | TX3_D6_SIGN | TX3_D6_OLEV | | | TX3_D5_SIGN | TX3_D5_OLEV | | | 0x00 | RW | | | | | |
| 0x3C | Tx3DrvEn0 | [7:0] | TX3_D2_DRV_EN | | TX3_D1_DRV_EN | | TX3_D0_DRV_EN | | TX3_PC_DRV_EN | | | 0x3C | RW | | | | |
| 0x3D | Tx3DrvEn1 | [7:0] | TX3_D6_DRV_EN | | TX3_D5_DRV_EN | | TX3_D4_DRV_EN | | TX3_D3_DRV_EN | | | 0x00 | RW | | | | |
| 0x3E | Tx3DrvRes0 | [7:0] | TX3_D2_RES | | TX3_D1_RES | | TX3_D0_RES | | TX3_PC_RES | | | 0x00 | RW | | | | |
| 0x3F | Tx3DrvRes1 | [7:0] | TX3_D6_RES | | TX3_D5_RES | | TX3_D4_RES | | TX3_D3_RES | | | 0x54 | RW | | | | |
| 0x40 | Tx4DrvCtrl0 | [7:0] | TX4_D0_SIGN | TX4_D0_OLEV | | | TX4_PC_SIGN | TX4_PC_OLEV | | | 0x30 | RW | | | | | |
| 0x41 | Tx4DrvCtrl1 | [7:0] | TX4_D2_SIGN | TX4_D2_OLEV | | | TX4_D1_SIGN | TX4_D1_OLEV | | | 0x33 | RW | | | | | |
| 0x42 | Tx4DrvCtrl2 | [7:0] | TX4_D4_SIGN | TX4_D4_OLEV | | | TX4_D3_SIGN | TX4_D3_OLEV | | | 0x0B | RW | | | | | |
| 0x43 | Tx4DrvCtrl3 | [7:0] | TX4_D6_SIGN | TX4_D6_OLEV | | | TX4_D5_SIGN | TX4_D5_OLEV | | | 0x00 | RW | | | | | |
| 0x44 | Tx4DrvEn0 | [7:0] | TX4_D2_DRV_EN | | TX4_D1_DRV_EN | | TX4_D0_DRV_EN | | TX4_PC_DRV_EN | | | 0x3C | RW | | | | |
| 0x45 | Tx4DrvEn1 | [7:0] | TX4_D6_DRV_EN | | TX4_D5_DRV_EN | | TX4_D4_DRV_EN | | TX4_D3_DRV_EN | | | 0x00 | RW | | | | |
| 0x46 | Tx4DrvRes0 | [7:0] | TX4_D2_RES | | TX4_D1_RES | | TX4_D0_RES | | TX4_PC_RES | | | 0x00 | RW | | | | |
| 0x47 | Tx4DrvRes1 | [7:0] | TX4_D6_RES | | TX4_D5_RES | | TX4_D4_RES | | TX4_D3_RES | | | 0x54 | RW | | | | |
| 0x48 | Tx5DrvCtrl0 | [7:0] | TX5_D0_SIGN | TX5_D0_OLEV | | | TX5_PC_SIGN | TX5_PC_OLEV | | | 0x30 | RW | | | | | |
| 0x49 | Tx5DrvCtrl1 | [7:0] | TX5_D2_SIGN | TX5_D2_OLEV | | | TX5_D1_SIGN | TX5_D1_OLEV | | | 0x33 | RW | | | | | |
| 0x4A | Tx5DrvCtrl2 | [7:0] | TX5_D4_SIGN | TX5_D4_OLEV | | | TX5_D3_SIGN | TX5_D3_OLEV | | | 0x0B | RW | | | | | |
| 0x4B | Tx5DrvCtrl3 | [7:0] | TX5_D6_SIGN | TX5_D6_OLEV | | | TX5_D4_OLEV | TX5_D5_OLEV | | | 0x00 | RW | | | | | |
| 0x4C | Tx5DrvEn0 | [7:0] | TX5_D2_DRV_EN | | TX5_D1_DRV_EN | | TX5_D0_DRV_EN | | TX5_PC_DRV_EN | | | 0x3C | RW | | | | |
| 0x4D | Tx5DrvEn1 | [7:0] | TX5_D6_DRV_EN | | TX5_D5_DRV_EN | | TX5_D4_DRV_EN | | TX5_D3_DRV_EN | | | 0x00 | RW | | | | |
| 0x4E | Tx5DrvRes0 | [7:0] | TX5_D2_RES | | TX5_D1_RES | | TX5_D0_RES | | TX5_PC_RES | | | 0x00 | RW | | | | |
| 0x4F | Tx5DrvRes1 | [7:0] | TX5_D6_RES | | TX5_D5_RES | | TX5_D4_RES | | TX5_D3_RES | | | 0x54 | RW | | | | |

| Reg (Hex) | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW | |
|-----------|-------------------|-------|----------------|----------------|----------------|----------|----------------|----------|----------------|----------|-------|----|---|
| 0x50 | Tx6DrvCtrl0 | [7:0] | TX6_D0_SIGN | | TX6_D0_OLEV | | TX6_PC_SIGN | | TX6_PC_OLEV | | 0x30 | RW | |
| 0x51 | Tx6DrvCtrl1 | [7:0] | TX6_D2_SIGN | | TX6_D2_OLEV | | TX6_D1_SIGN | | TX6_D1_OLEV | | 0x33 | RW | |
| 0x52 | Tx6DrvCtrl2 | [7:0] | TX6_D4_SIGN | | TX6_D4_OLEV | | TX6_D3_SIGN | | TX6_D3_OLEV | | 0x0B | RW | |
| 0x53 | Tx6DrvCtrl3 | [7:0] | TX6_D6_SIGN | | TX6_D6_OLEV | | TX6_D5_SIGN | | TX6_D5_OLEV | | 0x00 | RW | |
| 0x54 | Tx6DrvEn0 | [7:0] | TX6_D2_DRV_EN | | TX6_D1_DRV_EN | | TX6_D0_DRV_EN | | TX6_PC_DRV_EN | | 0x3C | RW | |
| 0x55 | Tx6DrvEn1 | [7:0] | TX6_D6_DRV_EN | | TX6_D5_DRV_EN | | TX6_D4_DRV_EN | | TX6_D3_DRV_EN | | 0x00 | RW | |
| 0x56 | Tx6DrvRes0 | [7:0] | TX6_D2_RES | | TX6_D1_RES | | TX6_D0_RES | | TX6_PC_RES | | 0x00 | RW | |
| 0x57 | Tx6DrvRes1 | [7:0] | TX6_D6_RES | | TX6_D5_RES | | TX6_D4_RES | | TX6_D3_RES | | 0x54 | RW | |
| 0x58 | Tx7DrvCtrl0 | [7:0] | TX7_D0_SIGN | | TX7_D0_OLEV | | TX7_PC_SIGN | | TX7_PC_OLEV | | 0x30 | RW | |
| 0x59 | Tx7DrvCtrl1 | [7:0] | TX7_D2_SIGN | | TX7_D2_OLEV | | TX7_D1_SIGN | | TX7_D1_OLEV | | 0x33 | RW | |
| 0x5A | Tx7DrvCtrl2 | [7:0] | TX7_D4_SIGN | | TX7_D4_OLEV | | TX7_D3_SIGN | | TX7_D3_OLEV | | 0x0B | RW | |
| 0x5B | Tx7DrvCtrl3 | [7:0] | TX7_D6_SIGN | | TX7_D6_OLEV | | TX7_D5_SIGN | | TX7_D5_OLEV | | 0x00 | RW | |
| 0x5C | Tx7DrvEn0 | [7:0] | TX7_D2_DRV_EN | | TX7_D1_DRV_EN | | TX7_D0_DRV_EN | | TX7_PC_DRV_EN | | 0x3C | RW | |
| 0x5D | Tx7DrvEn1 | [7:0] | TX7_D6_DRV_EN | | TX7_D5_DRV_EN | | TX7_D4_DRV_EN | | TX7_D3_DRV_EN | | 0x00 | RW | |
| 0x5E | Tx7DrvRes0 | [7:0] | TX7_D2_RES | | TX7_D1_RES | | TX7_D0_RES | | TX7_PC_RES | | 0x00 | RW | |
| 0x5F | Tx7DrvRes1 | [7:0] | TX7_D6_RES | | TX7_D5_RES | | TX7_D4_RES | | TX7_D3_RES | | 0x54 | RW | |
| 0x60 | Tx8DrvCtrl0 | [7:0] | TX8_D0_SIGN | | TX8_D0_OLEV | | TX8_PC_SIGN | | TX8_PC_OLEV | | 0x30 | RW | |
| 0x61 | Tx8DrvCtrl1 | [7:0] | TX8_D2_SIGN | | TX8_D2_OLEV | | TX8_D1_SIGN | | TX8_D1_OLEV | | 0x33 | RW | |
| 0x62 | Tx8DrvCtrl2 | [7:0] | TX8_D4_SIGN | | TX8_D4_OLEV | | TX8_D3_SIGN | | TX8_D3_OLEV | | 0x0B | RW | |
| 0x63 | Tx8DrvCtrl3 | [7:0] | TX8_D6_SIGN | | TX8_D6_OLEV | | TX8_D5_SIGN | | TX8_D5_OLEV | | 0x00 | RW | |
| 0x64 | Tx8DrvEn0 | [7:0] | TX8_D2_DRV_EN | | TX8_D1_DRV_EN | | TX8_D0_DRV_EN | | TX8_PC_DRV_EN | | 0x3C | RW | |
| 0x65 | Tx8DrvEn1 | [7:0] | TX8_D6_DRV_EN | | TX8_D5_DRV_EN | | TX8_D4_DRV_EN | | TX8_D3_DRV_EN | | 0x00 | RW | |
| 0x66 | Tx8DrvRes0 | [7:0] | TX8_D2_RES | | TX8_D1_RES | | TX8_D0_RES | | TX8_PC_RES | | 0x00 | RW | |
| 0x67 | Tx8DrvRes1 | [7:0] | TX8_D6_RES | | TX8_D5_RES | | TX8_D4_RES | | TX8_D3_RES | | 0x54 | RW | |
| 0x68 | Tx9DrvCtrl0 | [7:0] | TX9_D0_SIGN | | TX9_D0_OLEV | | TX9_PC_SIGN | | TX9_PC_OLEV | | 0x30 | RW | |
| 0x69 | Tx9DrvCtrl1 | [7:0] | TX9_D2_SIGN | | TX9_D2_OLEV | | TX9_D1_SIGN | | TX9_D1_OLEV | | 0x33 | RW | |
| 0x6A | Tx9DrvCtrl2 | [7:0] | TX9_D4_SIGN | | TX9_D4_OLEV | | TX9_D3_SIGN | | TX9_D3_OLEV | | 0x0B | RW | |
| 0x6B | Tx9DrvCtrl3 | [7:0] | TX9_D6_SIGN | | TX9_D6_OLEV | | TX9_D5_SIGN | | TX9_D5_OLEV | | 0x00 | RW | |
| 0x6C | Tx9DrvEn0 | [7:0] | TX9_D2_DRV_EN | | TX9_D1_DRV_EN | | TX9_D0_DRV_EN | | TX9_PC_DRV_EN | | 0x3C | RW | |
| 0x6D | Tx9DrvEn1 | [7:0] | TX9_D6_DRV_EN | | TX9_D5_DRV_EN | | TX9_D4_DRV_EN | | TX9_D3_DRV_EN | | 0x00 | RW | |
| 0x6E | Tx9DrvRes0 | [7:0] | TX9_D2_RES | | TX9_D1_RES | | TX9_D0_RES | | TX9_PC_RES | | 0x00 | RW | |
| 0x6F | Tx9DrvRes1 | [7:0] | TX9_D6_RES | | TX9_D5_RES | | TX9_D4_RES | | TX9_D3_RES | | 0x54 | RW | |
| 0x70 | Tx10DrvCtrl0 | [7:0] | TX10_D0_SIGN | | TX10_D0_OLEV | | TX10_PC_SIGN | | TX10_PC_OLEV | | 0x30 | RW | |
| 0x71 | Tx10DrvCtrl1 | [7:0] | TX10_D2_SIGN | | TX10_D2_OLEV | | TX10_D1_SIGN | | TX10_D1_OLEV | | 0x33 | RW | |
| 0x72 | Tx10DrvCtrl2 | [7:0] | TX10_D4_SIGN | | TX10_D4_OLEV | | TX10_D3_SIGN | | TX10_D3_OLEV | | 0x0B | RW | |
| 0x73 | Tx10DrvCtrl3 | [7:0] | TX10_D6_SIGN | | TX10_D6_OLEV | | TX10_D5_SIGN | | TX10_D5_OLEV | | 0x00 | RW | |
| 0x74 | Tx10DrvEn0 | [7:0] | TX10_D2_DRV_EN | | TX10_D1_DRV_EN | | TX10_D0_DRV_EN | | TX10_PC_DRV_EN | | 0x3C | RW | |
| 0x75 | Tx10DrvEn1 | [7:0] | TX10_D6_DRV_EN | | TX10_D5_DRV_EN | | TX10_D4_DRV_EN | | TX10_D3_DRV_EN | | 0x00 | RW | |
| 0x76 | Tx10DrvRes0 | [7:0] | TX10_D2_RES | | TX10_D1_RES | | TX10_D0_RES | | TX10_PC_RES | | 0x00 | RW | |
| 0x77 | Tx10DrvRes1 | [7:0] | TX10_D6_RES | | TX10_D5_RES | | TX10_D4_RES | | TX10_D3_RES | | 0x54 | RW | |
| 0x78 | Tx11DrvCtrl0 | [7:0] | TX11_D0_SIGN | | TX11_D0_OLEV | | TX11_PC_SIGN | | TX11_PC_OLEV | | 0x30 | RW | |
| 0x79 | Tx11DrvCtrl1 | [7:0] | TX11_D2_SIGN | | TX11_D2_OLEV | | TX11_D1_SIGN | | TX11_D1_OLEV | | 0x33 | RW | |
| 0x7A | Tx11DrvCtrl2 | [7:0] | TX11_D4_SIGN | | TX11_D4_OLEV | | TX11_D3_SIGN | | TX11_D3_OLEV | | 0x0B | RW | |
| 0x7B | Tx11DrvCtrl3 | [7:0] | TX11_D6_SIGN | | TX11_D6_OLEV | | TX11_D5_SIGN | | TX11_D5_OLEV | | 0x00 | RW | |
| 0x7C | Tx11DrvEn0 | [7:0] | TX11_D2_DRV_EN | | TX11_D1_DRV_EN | | TX11_D0_DRV_EN | | TX11_PC_DRV_EN | | 0x3C | RW | |
| 0x7D | Tx11DrvEn1 | [7:0] | TX11_D6_DRV_EN | | TX11_D5_DRV_EN | | TX11_D4_DRV_EN | | TX11_D3_DRV_EN | | 0x00 | RW | |
| 0x7E | Tx11DrvRes0 | [7:0] | TX11_D2_RES | | TX11_D1_RES | | TX11_D0_RES | | TX11_PC_RES | | 0x00 | RW | |
| 0x7F | Tx11DrvRes1 | [7:0] | TX11_D6_RES | | TX11_D5_RES | | TX11_D4_RES | | TX11_D3_RES | | 0x54 | RW | |
| 0x80 | Rx0EqCtrl | [7:0] | RX0_EQP | | | | RX0_EQA | | | | 0x85 | RW | |
| 0x81 | Rx1EqCtrl | [7:0] | RX1_EQP | | | | RX1_EQA | | | | 0x85 | RW | |
| 0x82 | Rx2EqCtrl | [7:0] | RX2_EQP | | | | RX2_EQA | | | | 0x85 | RW | |
| 0x83 | Rx3EqCtrl | [7:0] | RX3_EQP | | | | RX3_EQA | | | | 0x85 | RW | |
| 0x84 | Rx4EqCtrl | [7:0] | RX4_EQP | | | | RX4_EQA | | | | 0x85 | RW | |
| 0x85 | Rx5EqCtrl | [7:0] | RX5_EQP | | | | RX5_EQA | | | | 0x85 | RW | |
| 0x86 | Rx5to0En | [7:0] | UNUSED_86 | | RX5EN | RX4EN | RX3EN | RX2EN | RX1EN | RX0EN | 0x00 | RW | |
| 0x87 | Rx5to0EqEn | [7:0] | UNUSED_87 | | RX5EQEN | RX4EQEN | RX3EQEN | RX2EQEN | RX1EQEN | RX0EQEN | 0x00 | RW | |
| 0x88 | Rx5to0LOSEn | [7:0] | UNUSED_88 | RX5TO0LOSREFEN | RX5LOSEN | RX4LOSEN | RX3LOSEN | RX2LOSEN | RX1LOSEN | RX0LOSEN | 0x40 | RW | |
| 0x89 | Rx1to0LOSTimeCtrl | [7:0] | RX1_LOS_TIME | | | | RX0_LOS_TIME | | | | 0x99 | RW | |
| 0x8A | Rx3to2LOSTimeCtrl | [7:0] | RX3_LOS_TIME | | | | RX2_LOS_TIME | | | | 0x99 | RW | |
| 0x8B | Rx5to4LOSTimeCtrl | [7:0] | RX5_LOS_TIME | | | | RX4_LOS_TIME | | | | 0x99 | RW | |
| 0x8C | Rx5to0LOSSSta | [7:0] | UNUSED_8C | RESERVED | LOS5TO0STA | | | | 0x00 | | | | R |
| 0x8D | Rx5to0LOSSStkySta | [7:0] | UNUSED_8D | RESERVED | LOS5TO0STKYSTA | | | | 0x00 | | | | R |
| 0x8E | Rx5to0LOSlvlCtrl | [7:0] | LOS_DEASSERT | | | | LOS_ASSERT | | | | 0x62 | RW | |

| Reg (Hex) | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW | | |
|-----------|--------------------------|-------|------------------|-----------------|-----------------|--------------|---------------------|-------------|------------------|-------------|------------------|----------------|------|----|
| 0x8F | Rx5to0LOSIRQEn | [7:0] | UNUSED_8F | | | RX5LOSIRQEN | RX4LOSIRQEN | RX3LOSIRQEN | RX2LOSIRQEN | RX1LOSIRQEN | RX0LOSIRQEN | 0x00 | RW | |
| 0x90 | Rx6EqCtrl | [7:0] | RX6_EQP | | | | | | RX6_EQA | | | | 0x85 | RW |
| 0x91 | Rx7EqCtrl | [7:0] | RX7_EQP | | | | | | RX7_EQA | | | | 0x85 | RW |
| 0x92 | Rx8EqCtrl | [7:0] | RX8_EQP | | | | | | RX8_EQA | | | | 0x85 | RW |
| 0x93 | Rx9EqCtrl | [7:0] | RX9_EQP | | | | | | RX9_EQA | | | | 0x85 | RW |
| 0x94 | Rx10EqCtrl | [7:0] | RX10_EQP | | | | | | RX10_EQA | | | | 0x85 | RW |
| 0x95 | Rx11EqCtrl | [7:0] | RX11_EQP | | | | | | RX11_EQA | | | | 0x85 | RW |
| 0x96 | Rx11to6En | [7:0] | UNUSED_96 | | | RX11EN | RX10EN | RX9EN | RX8EN | RX7EN | RX6EN | 0x00 | RW | |
| 0x97 | Rx11to6EqEn | [7:0] | UNUSED_97 | | | RX11EQEN | RX10EQEN | RX9EQEN | RX8EQEN | RX7EQEN | RX6EQEN | 0x00 | RW | |
| 0x98 | Rx11to6LOSEn | [7:0] | UNUSED_98 | RX11TO6LOSREFEN | RX11LOSEN | RX10LOSEN | RX9LOSEN | RX8LOSEN | RX7LOSEN | RX6LOSEN | 0x40 | RW | | |
| 0x99 | Rx7to6LOSTimeCtrl | [7:0] | RX7_LOS_TIME | | | | | | RX6_LOS_TIME | | | | 0x99 | RW |
| 0x9A | Rx9to8LOSTimeCtrl | [7:0] | RX9_LOS_TIME | | | | | | RX8_LOS_TIME | | | | 0x99 | RW |
| 0x9B | Rx11to10LOSTimeCtrl | [7:0] | RX11_LOS_TIME | | | | | | RX10_LOS_TIME | | | | 0x99 | RW |
| 0x9C | Rx11to6LOSSta | [7:0] | UNUSED_9C | RESERVED | LOS11TO6STA | | | | | | 0x00 | RW | | |
| 0x9D | Rx11to6LOSStkySta | [7:0] | UNUSED_9D | RESERVED | LOS11TO6STKYSTA | | | | | | 0x00 | RW | | |
| 0x9E | Rx11to6LOSlvlCtrl | [7:0] | LOS_DEASSERT | | | | | | LOS_ASSERT | | | | 0x62 | RW |
| 0x9F | Rx11to6LOSIRQEn | [7:0] | UNUSED_8F | | | RX11LOSIRQEN | RX10LOSIRQEN | RX9LOSIRQEN | RX8LOSIRQEN | RX7LOSIRQEN | RX6LOSIRQEN | 0x00 | RW | |
| 0xA0 | Rx5to0OffsetCal | [7:0] | UNUSED_A0 | | | RX5OCAL | RX4OCAL | RX3OCAL | RX2OCAL | RX1OCAL | RX0OCAL | 0x00 | RW | |
| 0xA8 | Rx11to6OffsetCal | [7:0] | UNUSED_A8 | | | RX11OCAL | RX10OCAL | RX9OCAL | RX8OCAL | RX7OCAL | RX6OCAL | 0x00 | RW | |
| 0xB0 | XPT_MapA_Out_1_0 | [7:0] | XPT_MAPA_OUT1 | | | | | | XPT_MAPA_OUT0 | | | | 0x10 | RW |
| 0xB1 | XPT_MapA_Out_3_2 | [7:0] | XPT_MAPA_OUT3 | | | | | | XPT_MAPA_OUT2 | | | | 0x32 | RW |
| 0xB2 | XPT_MapA_Out_5_4 | [7:0] | XPT_MAPA_OUT5 | | | | | | XPT_MAPA_OUT4 | | | | 0x54 | RW |
| 0xB3 | XPT_MapA_Out_7_6 | [7:0] | XPT_MAPA_OUT7 | | | | | | XPT_MAPA_OUT6 | | | | 0x76 | RW |
| 0xB4 | XPT_MapA_Out_9_8 | [7:0] | XPT_MAPA_OUT9 | | | | | | XPT_MAPA_OUT8 | | | | 0x98 | RW |
| 0xB5 | XPT_MapA_Out_11_10 | [7:0] | XPT_MAPA_OUT11 | | | | | | XPT_MAPA_OUT10 | | | | 0xBA | RW |
| 0xB8 | XPT_MapB_Out_1_0 | [7:0] | XPT_MAPB_OUT1 | | | | | | XPT_MAPB_OUT0 | | | | 0x23 | RW |
| 0xB9 | XPT_MapB_Out_3_2 | [7:0] | XPT_MAPB_OUT3 | | | | | | XPT_MAPB_OUT2 | | | | 0x23 | RW |
| 0xBA | XPT_MapB_Out_5_4 | [7:0] | XPT_MAPB_OUT5 | | | | | | XPT_MAPB_OUT4 | | | | 0x01 | RW |
| 0xBB | XPT_MapB_Out_7_6 | [7:0] | XPT_MAPB_OUT7 | | | | | | XPT_MAPB_OUT6 | | | | 0x01 | RW |
| 0xBC | XPT_MapB_Out_9_8 | [7:0] | XPT_MAPB_OUT9 | | | | | | XPT_MAPB_OUT8 | | | | 0xAB | RW |
| 0xBD | XPT_MapB_Out_11_10 | [7:0] | XPT_MAPB_OUT11 | | | | | | XPT_MAPB_OUT10 | | | | 0x54 | RW |
| 0xC0 | XPT_MapC_Out_1_0 | [7:0] | XPT_MAPC_OUT1 | | | | | | XPT_MAPC_OUT0 | | | | 0x23 | RW |
| 0xC1 | XPT_MapC_Out_3_2 | [7:0] | XPT_MAPC_OUT3 | | | | | | XPT_MAPC_OUT2 | | | | 0x23 | RW |
| 0xC2 | XPT_MapC_Out_5_4 | [7:0] | XPT_MAPC_OUT5 | | | | | | XPT_MAPC_OUT4 | | | | 0x01 | RW |
| 0xC3 | XPT_MapC_Out_7_6 | [7:0] | XPT_MAPC_OUT7 | | | | | | XPT_MAPC_OUT6 | | | | 0x01 | RW |
| 0xC4 | XPT_MapC_Out_9_8 | [7:0] | XPT_MAPC_OUT9 | | | | | | XPT_MAPC_OUT8 | | | | 0x89 | RW |
| 0xC5 | XPT_MapC_Out_11_10 | [7:0] | XPT_MAPC_OUT11 | | | | | | XPT_MAPC_OUT10 | | | | 0x67 | RW |
| 0xC8 | XPT_MapD_Out_1_0 | [7:0] | XPT_MAPD_OUT1 | | | | | | XPT_MAPD_OUT0 | | | | 0x76 | RW |
| 0xC9 | XPT_MapD_Out_3_2 | [7:0] | XPT_MAPD_OUT3 | | | | | | XPT_MAPD_OUT2 | | | | 0x45 | RW |
| 0xCA | XPT_MapD_Out_5_4 | [7:0] | XPT_MAPD_OUT5 | | | | | | XPT_MAPD_OUT4 | | | | 0xBA | RW |
| 0xCB | XPT_MapD_Out_7_6 | [7:0] | XPT_MAPD_OUT7 | | | | | | XPT_MAPD_OUT6 | | | | 0x98 | RW |
| 0xCC | XPT_MapD_Out_9_8 | [7:0] | XPT_MAPD_OUT9 | | | | | | XPT_MAPD_OUT8 | | | | 0xAB | RW |
| 0xCD | XPT_MapD_Out_11_10 | [7:0] | XPT_MAPD_OUT11 | | | | | | XPT_MAPD_OUT10 | | | | 0x54 | RW |
| 0xD0 | XPT_Map_Status_1_0 | [7:0] | XPT_MAP_STATUS1 | | | | | | XPT_MAP_STATUS0 | | | | | R |
| 0xD1 | XPT_Map_Status_3_2 | [7:0] | XPT_MAP_STATUS3 | | | | | | XPT_MAP_STATUS2 | | | | | R |
| 0xD2 | XPT_Map_Status_5_4 | [7:0] | XPT_MAP_STATUS5 | | | | | | XPT_MAP_STATUS4 | | | | | R |
| 0xD3 | XPT_Map_Status_7_6 | [7:0] | XPT_MAP_STATUS7 | | | | | | XPT_MAP_STATUS6 | | | | | R |
| 0xD4 | XPT_Map_Status_9_8 | [7:0] | XPT_MAP_STATUS9 | | | | | | XPT_MAP_STATUS8 | | | | | R |
| 0xD5 | XPT_Map_Status_11_10 | [7:0] | XPT_MAP_STATUS11 | | | | | | XPT_MAP_STATUS10 | | | | | R |
| 0xDD | Boot_from_EEPROM_Control | [7:0] | UNUSED_DD | | | | | | | | | IGNORE_EEPROMB | 0x00 | RW |
| 0xDE | XPT_Table_Map | [7:0] | UNUSED_DE_1 | | | | XPT_TABLE_SELECT_EN | UNUSED_DE_0 | | | XPT_TABLE_SELECT | 0x00 | RW | |
| 0xDF | XPT_Update | [7:0] | UNUSED_DF | | | | | | | | | UPDATE_XPT | 0x00 | W |
| 0xEE | EEPROMChecksum | [7:0] | BOOTCHK[7:0] | | | | | | | | | | 0x00 | RW |
| 0xEF | EEPROMStatus | [7:0] | UNUSED_EF | | | | | | CHKSUM_PASS | CHKSUM_FAIL | EEPROM_DONE | | R | |
| 0xFE | Revid | [7:0] | REVID | | | | | | | | | | 0x00 | R |
| 0xFF | ChipID | [7:0] | CHIPID | | | | | | | | | | 0x12 | R |

REGISTER DESCRIPTIONS

SOFTWARE RESET REGISTER

Address: 0x00, Reset: 0x00, Name: Soft_Reset

Software reset register. Write a Logic 1 to reset the device registers to the default state. This register is write only.

Table 33. Bit Descriptions for Soft_Reset

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------|-----------------------|-------|--------|
| [7:1] | UNUSED_00 | | Unused register bits. | 0x0 | W |
| 0 | SOFT_RESET | | Software reset. | 0x0 | W |

Tx ENABLE CONTROL REGISTERS

Tx 7 to Tx 0 Enable Control Register

Address: 0x02, Reset: 0x00, Name: Tx_Enable_7to0

Tx 7 to Tx 0 enable control register. Write a Logic 1 to enable the transmitter output. Write a Logic 0 to disable the transmitter output.

Table 34. Bit Descriptions for Tx_Enable_7to0

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|---|-------|--------|
| 7 | TXEN7 | | Enable for Tx 7. | 0x0 | RW |
| 6 | TXEN6 | | Enable for Tx 6. | 0x0 | RW |
| 5 | TXEN5 | | Enable for Tx 5. | 0x0 | RW |
| 4 | TXEN4 | | Enable for Tx 4. | 0x0 | RW |
| 3 | TXEN3 | | Enable for Tx 3. | 0x0 | RW |
| 2 | TXEN2 | | Enable for Tx 2. | 0x0 | RW |
| 1 | TXEN1 | | Enable for Tx 1. | 0x0 | RW |
| 0 | TXEN0 | 0 1 | Enable for Tx 0. Disabled Enabled | 0x0 | RW |

Tx 11 to Tx 8 Enable Control Register

Address: 0x03, Reset: 0x00, Name: Tx_Enable_11to8

Tx 11 to Tx 8 enable control register. Write a Logic 1 to enable the transmitter output. Write a Logic 0 to disable the transmitter output.

Table 35. Bit Descriptions for Tx_Enable_11to8

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|---|-------|--------|
| [7:4] | UNUSED_03 | | Unused register bits. | 0x0 | RW |
| 3 | TXEN11 | | Enable for Tx 11. | 0x0 | RW |
| 2 | TXEN10 | | Enable for Tx 10. | 0x0 | RW |
| 1 | TXEN9 | | Enable for Tx 9. | 0x0 | RW |
| 0 | TXEN8 | 0 1 | Enable for Tx 8. Disabled Enabled | 0x0 | RW |

TX REFERENCE ENABLE REGISTER

Address: 0x04, Reset: 0x3F, Name: Tx_Ref_En

Tx reference enable register. Disable the unused Tx pair reference circuits to achieve further power savings.

Table 36. Bit Descriptions for Tx_Ref_En

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------|--|-------|--------|
| [7:6] | UNUSED_04 | | Unused register bits. | 0x0 | RW |
| 5 | TX11AND10EN | | Tx 11 and Tx 10 reference enable. | 0x1 | RW |
| 4 | TX9AND8EN | | Tx 9 and Tx 8 reference enable. | 0x1 | RW |
| 3 | TX7AND6EN | | Tx 7 and Tx 6 reference enable. | 0x1 | RW |
| 2 | TX5AND4EN | | Tx 5 and Tx 4 reference enable. | 0x1 | RW |
| 1 | TX3AND2EN | | Tx 3 and Tx 2 reference enable. | 0x1 | RW |
| 0 | TX1AND0EN | 0 1 | Tx 1 and Tx 0 reference enable. Disabled Enabled | 0x1 | RW |

SQUELCH CONTROL REGISTER

Address: 0x05, Reset: 0x00, Name: Tx_Squelch_Control

Squelch control register. Enable and configure squelch mode on LOS event.

Table 37. Bit Descriptions for Tx_Squelch_Control

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------------------|----------|--|-------|--------|
| [7:1] | UNUSED_05 | | Unused register bits. | 0x0 | RW |
| 0 | GLOBAL_SQUELCH_ENABLE | 0 1 | Enables squelch on LOS event. Disabled Enabled | 0x0 | RW |

Rx AND Tx SWAP SIGN REGISTERS**Swap Sign of Rx 7 to Rx 0 Inputs Register**

Address: 0x08, Reset: 0x00, Name: Rx7to0_Sign

Swap sign of Rx 7 to Rx 0 inputs register. Write a Logic 1 to invert P/N lanes. Write a Logic 0 to noninvert P/N lanes.

Table 38. Bit Descriptions for Rx7to0_Sign

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|---|-------|--------|
| 7 | RX7_SIGN | | Swap sign of Rx 7. | 0x0 | RW |
| 6 | RX6_SIGN | | Swap sign of Rx 6. | 0x0 | RW |
| 5 | RX5_SIGN | | Swap sign of Rx 5. | 0x0 | RW |
| 4 | RX4_SIGN | | Swap sign of Rx 4. | 0x0 | RW |
| 3 | RX3_SIGN | | Swap sign of Rx 3. | 0x0 | RW |
| 2 | RX2_SIGN | | Swap sign of Rx 2. | 0x0 | RW |
| 1 | RX1_SIGN | | Swap sign of Rx 1. | 0x0 | RW |
| 0 | RX0_SIGN | 0 1 | Swap sign of Rx 0. Noninverting Inverting | 0x0 | RW |

Swap Sign of Rx 11 to Rx 8 Inputs Register

Address: 0x09, Reset: 0x00, Name: Rx11to8_Sign

Swap sign of Rx 11 to Rx 8 inputs register. Write a Logic 1 to invert P/N lanes. Write a Logic 0 to noninvert P/N lanes.

Table 39. Bit Descriptions for Rx11to8_Sign

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|---|-------|--------|
| [7:4] | UNUSED_09 | | Unused register bits. | 0x0 | RW |
| 3 | RX11_SIGN | | Swap sign of Rx 11. | 0x0 | RW |
| 2 | RX10_SIGN | | Swap sign of Rx 10. | 0x0 | RW |
| 1 | RX9_SIGN | | Swap sign of Rx 9. | 0x0 | RW |
| 0 | RX8_SIGN | 0 1 | Swap sign of Rx 8. Noninverting Inverting | 0x0 | RW |

Swap Sign of Tx 7 to Tx 0 Outputs Register

Address: 0x0A, Reset: 0x00, Name: Tx7to0_Sign

Swap sign of Tx 7 to Tx 0 outputs register. Write a Logic 1 to invert P/N lanes. Write a Logic 0 to noninvert P/N lanes.

Table 40. Bit Descriptions for Tx7to0_Sign

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|---|-------|--------|
| 7 | TX7_SIGN | | Swap sign of Tx 7. | 0x0 | RW |
| 6 | TX6_SIGN | | Swap sign of Tx 6. | 0x0 | RW |
| 5 | TX5_SIGN | | Swap sign of Tx 5. | 0x0 | RW |
| 4 | TX4_SIGN | | Swap sign of Tx 4. | 0x0 | RW |
| 3 | TX3_SIGN | | Swap sign of Tx 3. | 0x0 | RW |
| 2 | TX2_SIGN | | Swap sign of Tx 2. | 0x0 | RW |
| 1 | TX1_SIGN | | Swap sign of Tx 1. | 0x0 | RW |
| 0 | TX0_SIGN | 0 1 | Swap sign of Tx 0. Noninverting Inverting | 0x0 | RW |

Swap Sign of Tx 11 to Tx 8 Outputs Register

Address: 0x0B, Reset: 0x00, Name: Tx11to8_Sign

Swap sign of Tx 11 to Tx 8 inputs register. Write a Logic 1 to invert P/N lanes. Write a Logic 0 to noninvert P/N lanes.

Table 41. Bit Descriptions for Tx11to8_Sign

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|---|-------|--------|
| [7:4] | UNUSED_0B | | Unused register bits. | 0x0 | RW |
| 3 | TX11_SIGN | | Swap sign of Tx 11. | 0x0 | RW |
| 2 | TX10_SIGN | | Swap sign of Tx 10. | 0x0 | RW |
| 1 | TX9_SIGN | | Swap sign of Tx 9. | 0x0 | RW |
| 0 | TX8_SIGN | 0 1 | Swap sign of Tx 8. Noninverting Inverting | 0x0 | RW |

XPT BROADCAST LANE NUMBER REGISTER

Address: 0x0F, Reset: 0x00, Name: XPT_Broadcast

XPT broadcast register. Connect a single input to all outputs.

Table 42. Bit Descriptions for XPT_Broadcast

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|---------------------------------|-------|--------|
| [7:4] | UNUSED_OF | | Unused register bits. | 0x0 | RW |
| [3:0] | XPT_BROADCAST | | XPT broadcast channel bits. | 0x0 | RW |
| | | 0000 | Connect Input 0 to All Outputs | | |
| | | 0001 | Connect Input 1 to All Outputs | | |
| | | 0010 | Connect Input 2 to All Outputs | | |
| | | 0011 | Connect Input 3 to All Outputs | | |
| | | 0100 | Connect Input 4 to All Outputs | | |
| | | 0101 | Connect Input 5 to All Outputs | | |
| | | 0110 | Connect Input 6 to All Outputs | | |
| | | 0111 | Connect Input 7 to All Outputs | | |
| | | 1000 | Connect Input 8 to All Outputs | | |
| | | 1001 | Connect Input 9 to All Outputs | | |
| | | 1010 | Connect Input 10 to All Outputs | | |
| | | 1011 | Connect Input 11 to All Outputs | | |

Tx 0 DRIVER CONTROL REGISTERS***Tx 0 Driver Control 0 Register***

Address: 0x20, Reset: 0x30, Name: Tx0DrvCtrl0

Tx 0 Driver Control 0 register. Configure precursor tap (PC) and main tap (D0) output level and sign.

Table 43. Bit Descriptions for Tx0DrvCtrl0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------|------------------------------|-------|--------|
| 7 | TX0_D0_SIGN | | Tx 0 D0 output level sign. | 0x0 | RW |
| [6:4] | TX0_D0_OLEV | | Tx 0 D0 output level. | 0x3 | RW |
| 3 | TX0_PC_SIGN | | Tx 0 PC output level sign. | 0x0 | RW |
| | | 0 | Positive (+) Tap Coefficient | | |
| | | 1 | Negative (-) Tap Coefficient | | |
| [2:0] | TX0_PC_OLEV | | Tx 0 PC output level. | 0x0 | RW |
| | | 0x0 | 2 mA | | |
| | | 0x1 | 4 mA | | |
| | | 0x2 | 6 mA | | |
| | | 0x3 | 8 mA | | |
| | | 0x4 | 10 mA | | |
| | | 0x5 | 12 mA | | |
| | | 0x6 | 14 mA | | |
| | | 0x7 | 16 mA | | |

Tx 0 Driver Control 1 Register

Address: 0x21, Reset: 0x33, Name: Tx0DrvCtrl1

Tx 0 Driver Control 1 register. Configure main tap (D1) and main tap (D2) output level and sign.

Table 44. Bit Descriptions for Tx0DrvCtrl1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|--|---|-------|--------|
| 7 | TX0_D2_SIGN | | Tx 0 D2 output level sign. | 0x0 | RW |
| [6:4] | TX0_D2_OLEV | | Tx 0 D2 output level. | 0x3 | RW |
| 3 | TX0_D1_SIGN | 0 | Positive (+) Tap Coefficient | 0x0 | RW |
| | | 1 | Negative (-) Tap Coefficient | | |
| [2:0] | TX0_D1_OLEV | 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7 | Tx 0 D1 output level. 2 mA 4 mA 6 mA 8 mA 10 mA 12 mA 14 mA 16 mA | 0x3 | RW |

Tx 0 Driver Control 2 Register

Address: 0x22, Reset: 0x0B, Name: Tx0DrvCtrl2

Tx 0 Driver Control 2 register. Configure post tap (D3) and post tap (D4) output level and sign.

Table 45. Bit Descriptions for Tx0DrvCtrl2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|--|---|-------|--------|
| 7 | TX0_D4_SIGN | | Tx 0 D4 output level sign. | 0x0 | RW |
| [6:4] | TX0_D4_OLEV | | Tx 0 D4 output level bit. | 0x0 | RW |
| 3 | TX0_D3_SIGN | 0 | Positive (+) Tap Coefficient | 0x1 | RW |
| | | 1 | Negative (-) Tap Coefficient | | |
| [2:0] | TX0_D3_OLEV | 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7 | Tx 0 D3 output level bit. 2 mA 4 mA 6 mA 8 mA 10 mA 12 mA 14 mA 16 mA | 0x3 | RW |

Tx 0 Driver Control 3 Register

Address: 0x23, Reset: 0x00, Name: Tx0DrvCtrl3

Tx 0 Driver Control 3 register. Configure post tap (D5) and post tap (D6) output level and sign.

Table 46. Bit Descriptions for Tx0DrvCtrl3

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------|------------------------------|-------|--------|
| 7 | TX0_D6_SIGN | | Tx 0 D6 output level sign. | 0x0 | RW |
| [6:4] | TX0_D6_OLEV | | Tx 0 D6 output level bit. | 0x0 | RW |
| 3 | TX0_D5_SIGN | 0 | Positive (+) Tap Coefficient | 0x0 | RW |
| | | 1 | Negative (-) Tap Coefficient | | |
| [2:0] | TX0_D5_OLEV | | Tx 0 D5 output level bit. | 0x0 | RW |
| | | 0x0 | 2 mA | | |
| | | 0x1 | 4 mA | | |
| | | 0x2 | 6 mA | | |
| | | 0x3 | 8 mA | | |
| | | 0x4 | 10 mA | | |
| | | 0x5 | 12 mA | | |
| | | 0x6 | 14 mA | | |
| 0x7 | 16 mA | | | | |

Tx 0 DRIVER ENABLE REGISTERS**Tx 0 Driver Enable 0 Register**

Address: 0x24, Reset: 0x3C, Name: Tx0DrvEn0

Tx 0 Driver Enable 0 register. Enable/disable driver for PC, D0, D1, and D2 taps. Write 0x3 to enable tap. Write 0x0 to disable tap.

Table 47. Bit Descriptions for Tx0DrvEn0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|------------------------|-------|--------|
| [7:6] | TX0_D2_DRV_EN | | Tx 0 D2 driver enable. | 0x0 | RW |
| [5:4] | TX0_D1_DRV_EN | | Tx 0 D1 driver enable. | 0x3 | RW |
| [3:2] | TX0_D0_DRV_EN | | Tx 0 D0 driver enable. | 0x3 | RW |
| [1:0] | TX0_PC_DRV_EN | | Tx 0 PC driver enable. | 0x0 | RW |
| | | 00 | Disabled | | |
| | | 01 | Not Used | | |
| | | 10 | Not Used | | |
| | | 11 | Enabled | | |

Tx 0 Driver Enable 1 Register

Address: 0x25, Reset: 0x00, Name: Tx0DrvEn1

Tx 0 Driver Enable 1 register. Enable/disable driver for D3, D4, D5, and D6 taps. Write 0x3 to enable tap. Write 0x0 to disable tap.

Table 48. Bit Descriptions for Tx0DrvEn1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|------------------------|-------|--------|
| [7:6] | TX0_D6_DRV_EN | | Tx 0 D6 driver enable. | 0x0 | RW |
| [5:4] | TX0_D5_DRV_EN | | Tx 0 D5 driver enable. | 0x0 | RW |
| [3:2] | TX0_D4_DRV_EN | | Tx 0 D4 driver enable. | 0x0 | RW |
| [1:0] | TX0_D3_DRV_EN | | Tx 0 D3 driver enable. | 0x0 | RW |
| | | 00 | Disabled | | |
| | | 01 | Not Used | | |
| | | 10 | Not Used | | |
| | | 11 | Enabled | | |

Tx 0 DRIVER RESOLUTION REGISTERS***Tx 0 Driver Resolution 0 Register***

Address: 0x26, Reset: 0x00, Name: Tx0DrvRes0

Tx 0 Driver Resolution 0 register. Resolution bit scales the Tx tap output level.

Table 49. Bit Descriptions for Tx0DrvRes0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------|-------------------------------------|-------|--------|
| [7:6] | TX0_D2_RES | | Tx 0 D2 output resolution bits. | 0x0 | RW |
| [5:4] | TX0_D1_RES | | Tx 0 D1 output resolution bits. | 0x0 | RW |
| [3:2] | TX0_D0_RES | | Tx 0 D0 output resolution bits | 0x0 | RW |
| [1:0] | TX0_PC_RES | | Tx 0 PC output resolution bits. | 0x0 | RW |
| | | 00 | 1 (Divides Tap Output Level by 1) | | |
| | | 01 | 1/2 (Divides Tap Output Level by 2) | | |
| | | 10 | 1/4 (Divides Tap Output Level by 4) | | |
| | | 11 | 1/8 (Divides Tap Output Level by 8) | | |

Tx 0 Driver Resolution 1 Register

Address: 0x27, Reset: 0x54, Name: Tx0DrvRes1

Tx 0 Driver Resolution 1 register. Resolution bit scales the Tx tap output level.

Table 50. Bit Descriptions for Tx0DrvRes1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------|-------------------------------------|-------|--------|
| [7:6] | TX0_D6_RES | | Tx 0 D6 output resolution bits. | 0x1 | RW |
| [5:4] | TX0_D5_RES | | Tx 0 D5 output resolution bits. | 0x1 | RW |
| [3:2] | TX0_D4_RES | | Tx 0 D4 output resolution bits. | 0x1 | RW |
| [1:0] | TX0_D3_RES | | Tx 0 D3 output resolution bits. | 0x0 | RW |
| | | 00 | 1 (Divides Tap Output Level by 1) | | |
| | | 01 | 1/2 (Divides Tap Output Level by 2) | | |
| | | 10 | 1/4 (Divides Tap Output Level by 4) | | |
| | | 11 | 1/8 (Divides Tap Output Level by 8) | | |

Tx 1 DRIVER CONTROL REGISTERS***Tx 1 Driver Control 0 Register***

Address: 0x28, Reset: 0x30, Name: Tx1DrvCtrl0

Refer to the Tx 0 Driver Control 0 Register section.

Tx 1 Driver Control 1 Register

Address: 0x29, Reset: 0x33, Name: Tx1DrvCtrl1

Refer to the Tx 0 Driver Control 1 Register section.

Tx 1 Driver Control 2 Register

Address: 0x2A, Reset: 0x0B, Name: Tx1DrvCtrl2

Refer to the Tx 0 Driver Control 2 Register section.

Tx 1 Driver Control 3 Register

Address: 0x2B, Reset: 0x00, Name: Tx1DrvCtrl3

Refer to the Tx 0 Driver Control 3 Register section.

Tx 1 DRIVER ENABLE REGISTERS***Tx 1 Driver Enable 0 Register***

Address: 0x2C, Reset: 0x3C, Name: Tx1DrvEn0

Refer to the Tx 0 Driver Enable 0 Register section.

Tx 1 Driver Enable 1 Register

Address: 0x2D, Reset: 0x00, Name: Tx1DrvEn1

Refer to the Tx 0 Driver Enable 1 Register section.

Tx 1 DRIVER RESOLUTION REGISTERS***Tx 1 Driver Resolution 0 Register***

Address: 0x2E, Reset: 0x00, Name: Tx1DrvRes0

Refer to the Tx 0 Driver Resolution 0 Register section.

Tx 1 Driver Resolution 1 Register

Address: 0x2F, Reset: 0x54, Name: Tx1DrvRes1

Refer to the Tx 0 Driver Resolution 1 Register section.

Tx 2 DRIVER CONTROL REGISTERS***Tx 2 Driver Control 0 Register***

Address: 0x30, Reset: 0x30, Name: Tx2DrvCtrl0

Refer to the Tx 0 Driver Control 0 Register section.

Tx 2 Driver Control 1 Register

Address: 0x31, Reset: 0x33, Name: Tx2DrvCtrl1

Refer to the Tx 0 Driver Control 1 Register section.

Tx 2 Driver Control 2 Register

Address: 0x32, Reset: 0x0B, Name: Tx2DrvCtrl2

Refer to the Tx 0 Driver Control 2 Register section.

Tx 2 Driver Control 3 Register

Address: 0x33, Reset: 0x00, Name: Tx2DrvCtrl3

Refer to the Tx 0 Driver Control 3 Register section.

Tx 2 DRIVER ENABLE REGISTERS***Tx 2 Driver Enable 0 Register***

Address: 0x34, Reset: 0x3C, Name: Tx2DrvEn0

Refer to the Tx 0 Driver Enable 0 Register section.

Tx 2 Driver Enable 1 Register

Address: 0x35, Reset: 0x00, Name: Tx2DrvEn1

Refer to the Tx 0 Driver Enable 1 Register section.

Tx 2 DRIVER RESOLUTION REGISTERS***Tx 2 Driver Resolution 0 Register***

Address: 0x36, Reset: 0x00, Name: Tx2DrvRes0

Refer to the Tx 0 Driver Resolution 0 Register section.

Tx 2 Driver Resolution 1 Register

Address: 0x37, Reset: 0x54, Name: Tx2DrvRes1

Refer to the Tx 0 Driver Resolution 1 Register section.

Tx 3 DRIVER CONTROL REGISTERS***Tx 3 Driver Control 0 Register***

Address: 0x38, Reset: 0x30, Name: Tx3DrvCtrl0

Refer to the Tx 0 Driver Control 0 Register section.

Tx 3 Driver Control 1 Register

Address: 0x39, Reset: 0x33, Name: Tx3DrvCtrl1

Refer to the Tx 0 Driver Control 1 Register section.

Tx 3 Driver Control 2 Register

Address: 0x3A, Reset: 0x0B, Name: Tx3DrvCtrl2

Refer to the Tx 0 Driver Control 2 Register section.

Tx 3 Driver Control 3 Register

Address: 0x3B, Reset: 0x00, Name: Tx3DrvCtrl3

Refer to the Tx 0 Driver Control 3 Register section.

Tx 3 DRIVER ENABLE REGISTERS***Tx 3 Driver Enable 0 Register***

Address: 0x3C, Reset: 0x3C, Name: Tx3DrvEn0

Refer to the Tx 0 Driver Enable 0 Register section.

Tx 3 Driver Enable 1 Register

Address: 0x3D, Reset: 0x00, Name: Tx3DrvEn1

Refer to the Tx 0 Driver Enable 1 Register section.

Tx 3 DRIVER RESOLUTION REGISTERS***Tx 3 Driver Resolution 0 Register***

Address: 0x3E, Reset: 0x00, Name: Tx3DrvRes0

Refer to the Tx 0 Driver Resolution 0 Register section.

Tx 3 Driver Resolution 1 Register

Address: 0x3F, Reset: 0x54, Name: Tx3DrvRes1

Refer to the Tx 0 Driver Resolution 1 Register section.

Tx 4 DRIVER CONTROL REGISTERS***Tx 4 Driver Control 0 Register***

Address: 0x40, Reset: 0x30, Name: Tx4DrvCtrl0

Refer to the Tx 0 Driver Control 0 Register section.

Tx 4 Driver Control 1 Register

Address: 0x41, Reset: 0x33, Name: Tx4DrvCtrl1

Refer to the Tx 0 Driver Control 1 Register section.

Tx 4 Driver Control 2 Register

Address: 0x42, Reset: 0x0B, Name: Tx4DrvCtrl2

Refer to the Tx 0 Driver Control 2 Register section.

Tx 4 Driver Control 3 Register

Address: 0x43, Reset: 0x00, Name: Tx4DrvCtrl3

Refer to the Tx 0 Driver Control 3 Register section.

Tx 4 DRIVER ENABLE REGISTERS***Tx 4 Driver Enable 0 Register***

Address: 0x44, Reset: 0x3C, Name: Tx4DrvEn0

Refer to the Tx 0 Driver Enable 0 Register section.

Tx 4 Driver Enable 1 Register

Address: 0x45, Reset: 0x00, Name: Tx4DrvEn1

Refer to the Tx 0 Driver Enable 1 Register section.

Tx 4 DRIVER RESOLUTION REGISTERS***Tx 4 Driver Resolution 0 Register***

Address: 0x46, Reset: 0x00, Name: Tx4DrvRes0

Refer to the Tx 0 Driver Resolution 0 Register section.

Tx 4 Driver Resolution 1 Register

Address: 0x47, Reset: 0x54, Name: Tx4DrvRes1

Refer to the Tx 0 Driver Resolution 1 Register section.

Tx 5 DRIVER CONTROL REGISTERS***Tx 5 Driver Control 0 Register***

Address: 0x48, Reset: 0x30, Name: Tx5DrvCtrl0

Refer to the Tx 0 Driver Control 0 Register section.

Tx 5 Driver Control 1 Register

Address: 0x49, Reset: 0x33, Name: Tx5DrvCtrl1

Refer to the Tx 0 Driver Control 1 Register section.

Tx 5 Driver Control 2 Register

Address: 0x4A, Reset: 0x0B, Name: Tx5DrvCtrl2

Refer to the Tx 0 Driver Control 2 Register section.

Tx 5 Driver Control 3 Register

Address: 0x4B, Reset: 0x00, Name: Tx5DrvCtrl3

Refer to Tx 0 Driver Control 3 Register section.

Tx 5 DRIVER ENABLE REGISTERS***Tx 5 Driver Enable 0 Register***

Address: 0x4C, Reset: 0x3C, Name: Tx5DrvEn0

Refer to Tx 0 Driver Enable 0 Register section.

Tx 5 Driver Enable 1 Register

Address: 0x4D, Reset: 0x00, Name: Tx5DrvEn1

Refer to Tx 0 Driver Enable 1 Register section.

Tx 5 DRIVER RESOLUTION REGISTERS***Tx 5 Driver Resolution 0 Register***

Address: 0x4E, Reset: 0x00, Name: Tx5DrvRes0

Refer to Tx 0 Driver Resolution 0 Register section.

Tx 5 Driver Resolution 1 Register

Address: 0x4F, Reset: 0x54, Name: Tx5DrvRes1

Refer to Tx 0 Driver Resolution 1 Register section.

Tx 6 DRIVER CONTROL REGISTERS***Tx 6 Driver Control 0 Register***

Address: 0x50, Reset: 0x30, Name: Tx6DrvCtrl0

Refer to Tx 0 Driver Control 0 Register section.

Tx 6 Driver Control 1 Register

Address: 0x51, Reset: 0x33, Name: Tx6DrvCtrl1

Refer to Tx 0 Driver Control 1 Register section.

Tx 6 Driver Control 2 Register

Address: 0x52, Reset: 0x0B, Name: Tx6DrvCtrl2

Refer to Tx 0 Driver Control 2 Register section.

Tx 6 Driver Control 3 Register

Address: 0x53, Reset: 0x00, Name: Tx6DrvCtrl3

Refer to Tx 0 Driver Control 3 Register section.

Tx 6 DRIVER ENABLE REGISTERS***Tx 6 Driver Enable 0 Register***

Address: 0x54, Reset: 0x3C, Name: Tx6DrvEn0

Refer to Tx 0 Driver Enable 0 Register section.

Tx 6 Driver Enable 1 Register

Address: 0x55, Reset: 0x00, Name: Tx6DrvEn1

Refer to Tx 0 Driver Enable 1 Register section.

Tx 6 DRIVER RESOLUTION REGISTERS***Tx 6 Driver Resolution 0 Register***

Address: 0x56, Reset: 0x00, Name: Tx6DrvRes0

Refer to Tx 0 Driver Resolution 0 Register section.

Tx 6 Driver Resolution 1 Register

Address: 0x57, Reset: 0x54, Name: Tx6DrvRes1

Refer to Tx 0 Driver Resolution 1 Register section.

Tx 7 DRIVER CONTROL REGISTERS***Tx 7 Driver Control 0 Register***

Address: 0x58, Reset: 0x30, Name: Tx7DrvCtrl0

Refer to Tx 0 Driver Control 0 Register section.

Tx 7 Driver Control 1 Register

Address: 0x59, Reset: 0x33, Name: Tx7DrvCtrl1

Refer to Tx 0 Driver Control 1 Register section.

Tx 7 Driver Control 2 Register

Address: 0x5A, Reset: 0x0B, Name: Tx7DrvCtrl2

Refer to Tx 0 Driver Control 2 Register section.

Tx 7 Driver Control 3 Register

Address: 0x5B, Reset: 0x00, Name: Tx7DrvCtrl3

Refer to Tx 0 Driver Control 3 Register section.

Tx 7 DRIVER ENABLE REGISTERS***Tx 7 Driver Enable 0 Register***

Address: 0x5C, Reset: 0x3C, Name: Tx7DrvEn0

Refer to Tx 0 Driver Enable 0 Register section.

Tx 7 Driver Enable 1 Register

Address: 0x5D, Reset: 0x00, Name: Tx7DrvEn1

Refer to Tx 0 Driver Enable 1 Register section.

Tx 7 DRIVER RESOLUTION REGISTERS***Tx 7 Driver Resolution 0 Register***

Address: 0x5E, Reset: 0x00, Name: Tx7DrvRes0

Refer to Tx 0 Driver Resolution 0 Register section.

Tx 7 Driver Resolution 1 Register

Address: 0x5F, Reset: 0x54, Name: Tx7DrvRes1

Refer to Tx 0 Driver Resolution 1 Register section.

Tx 8 DRIVER CONTROL REGISTERS***Tx 8 Driver Control 0 Register***

Address: 0x60, Reset: 0x30, Name: Tx8DrvCtrl0

Refer to Tx 0 Driver Control 0 Register section.

Tx 8 Driver Control 1 Register

Address: 0x61, Reset: 0x33, Name: Tx8DrvCtrl1

Refer to Tx 0 Driver Control 1 Register section.

Tx 8 Driver Control 2 Register

Address: 0x62, Reset: 0x0B, Name: Tx8DrvCtrl2

Refer to Tx 0 Driver Control 2 Register section.

Tx 8 Driver Control 3 Register

Address: 0x63, Reset: 0x00, Name: Tx8DrvCtrl3

Refer to Tx 0 Driver Control 3 Register section.

Tx 8 DRIVER ENABLE REGISTERS***Tx 8 Driver Enable 0 Register***

Address: 0x64, Reset: 0x3C, Name: Tx8DrvEn0

Refer to Tx 0 Driver Enable 0 Register section.

Tx 8 Driver Enable 1 Register

Address: 0x65, Reset: 0x00, Name: Tx8DrvEn1

Refer to Tx 0 Driver Enable 1 Register section.

Tx 8 DRIVER RESOLUTION REGISTERS***Tx 8 Driver Resolution 0 Register***

Address: 0x66, Reset: 0x00, Name: Tx8DrvRes0

Refer to Tx 0 Driver Resolution 0 Register section.

Tx 8 Driver Resolution 1 Register

Address: 0x67, Reset: 0x54, Name: Tx8DrvRes1

Refer to Tx 0 Driver Resolution 1 Register section.

Tx 9 DRIVER CONTROL REGISTERS***Tx 9 Driver Control 0 Register***

Address: 0x68, Reset: 0x30, Name: Tx9DrvCtrl0

Refer to Tx 0 Driver Control 0 Register section.

Tx 9 Driver Control 1 Register

Address: 0x69, Reset: 0x33, Name: Tx9DrvCtrl1

Refer to Tx 0 Driver Control 1 Register section.

Tx 9 Driver Control 2 Register

Address: 0x6A, Reset: 0x0B, Name: Tx9DrvCtrl2

Refer to Tx 0 Driver Control 2 Register section.

Tx 9 Driver Control 3 Register

Address: 0x6B, Reset: 0x00, Name: Tx9DrvCtrl3

Refer to Tx 0 Driver Control 3 Register section.

Tx 9 DRIVER ENABLE REGISTERS***Tx 9 Driver Enable 0 Register***

Address: 0x6C, Reset: 0x3C, Name: Tx9DrvEn0

Refer to Tx 0 Driver Enable 0 Register section.

Tx 9 Driver Enable 1 Register

Address: 0x6D, Reset: 0x00, Name: Tx9DrvEn1

Refer to Tx 0 Driver Enable 1 Register section.

Tx 9 DRIVER RESOLUTION REGISTERS***Tx 9 Driver Resolution 0 Register***

Address: 0x6E, Reset: 0x00, Name: Tx9DrvRes0

Refer to Tx 0 Driver Resolution 0 Register section.

Tx 9 Driver Resolution 1 Register

Address: 0x6F, Reset: 0x54, Name: Tx9DrvRes1

Refer to Tx 0 Driver Resolution 1 Register section.

Tx 10 DRIVER CONTROL REGISTERS***Tx 10 Driver Control 0 Register***

Address: 0x70, Reset: 0x30, Name: Tx10DrvCtrl0

Refer to Tx 0 Driver Control 0 Register section.

Tx 10 Driver Control 1 Register

Address: 0x71, Reset: 0x33, Name: Tx10DrvCtrl1

Refer to Tx 0 Driver Control 1 Register section.

Tx 10 Driver Control 2 Register

Address: 0x72, Reset: 0x0B, Name: Tx10DrvCtrl2

Refer to Tx 0 Driver Control 2 Register section.

Tx 10 Driver Control 3 Register

Address: 0x73, Reset: 0x00, Name: Tx10DrvCtrl3

Refer to Tx 0 Driver Control 3 Register section.

Tx 10 DRIVER ENABLE REGISTERS***Tx 10 Driver Enable 0 Register***

Address: 0x74, Reset: 0x3C, Name: Tx10DrvEn0

Refer to Tx 0 Driver Enable 0 Register section.

Tx 10 Driver Enable 1 Register

Address: 0x75, Reset: 0x00, Name: Tx10DrvEn1

Refer to Tx 0 Driver Enable 1 Register section.

Tx 10 DRIVER RESOLUTION REGISTERS***Tx 10 Driver Resolution 0 Register***

Address: 0x76, Reset: 0x00, Name: Tx10DrvRes0

Refer to Tx 0 Driver Resolution 0 Register section.

Tx 10 Driver Resolution 1 Register

Address: 0x77, Reset: 0x54, Name: Tx10DrvRes1

Refer to Tx 0 Driver Resolution 1 Register section.

Tx 11 DRIVER CONTROL REGISTERS***Tx 11 Driver Control 0 Register***

Address: 0x78, Reset: 0x30, Name: Tx11DrvCtrl0

Refer to Tx 0 Driver Control 0 Register section.

Tx 11 Driver Control 1 Register

Address: 0x79, Reset: 0x33, Name: Tx11DrvCtrl1

Refer to Tx 0 Driver Control 1 Register section.

Tx 11 Driver Control 2 Register

Address: 0x7A, Reset: 0x0B, Name: Tx11DrvCtrl2

Refer to Tx 0 Driver Control 2 Register section.

Tx 11 Driver Control 3 Register

Address: 0x7B, Reset: 0x00, Name: Tx11DrvCtrl3

Refer to Tx 0 Driver Control 3 Register section.

Tx 11 DRIVER ENABLE REGISTERS***Tx 11 Driver Enable 0 Register***

Address: 0x7C, Reset: 0x3C, Name: Tx11DrvEn0

Refer to Tx 0 Driver Enable 0 Register section.

Tx 11 Driver Enable 1 Register

Address: 0x7D, Reset: 0x00, Name: Tx11DrvEn1

Refer to Tx 0 Driver Enable 1 Register section.

Tx 11 DRIVER RESOLUTION REGISTERS***Tx 11 Driver Resolution 0 Register***

Address: 0x7E, Reset: 0x00, Name: Tx11DrvRes0

Refer to Tx 0 Driver Resolution 0 Register section.

Tx 11 Driver Resolution 1 Register

Address: 0x7F, Reset: 0x54, Name: Tx11DrvRes1

Refer to Tx 0 Driver Resolution 1 Register section.

Rx 0 TO Rx 5 ACTIVE AND PASSIVE EQUALIZATION CONTROL REGISTERS***Rx 0 Active and Passive Equalization Control Register 0 Register***

Address: 0x80, Reset: 0x85, Name: Rx0EqCtrl

Rx 0 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 51. Bit Descriptions for Rx0EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|---|---|-------|--------|
| [7:4] | RX0_EQP | 0x0 0x4 0x6 0x8 0xB 0xD | Rx 0 passive equalization. 0 dB 2.5 dB 4 dB 6 dB 9.5 dB 12 dB | 0x8 | RW |
| [3:0] | RX0_EQA | 0x0 0x3 0x5 0x7 0x9 0xB 0xD | Rx 0 active equalization. 1 dB 2.5 dB 3.5 dB 4.5 dB 5.5 dB 7.5 dB 9 dB | 0x5 | RW |

Rx 1 Active and Passive Equalization Control Register 0 Register

Address: 0x81, Reset: 0x85, Name: Rx1EqCtrl

Rx 1 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 52. Bit Descriptions for Rx1EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX1_EQP | | Rx 1 passive equalization. | 0x8 | RW |
| [3:0] | RX1_EQA | | Rx 1 active equalization. | 0x5 | RW |

Rx 2 Active and Passive Equalization Control Register 0 Register

Address: 0x82, Reset: 0x85, Name: Rx2EqCtrl

Rx 2 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 53. Bit Descriptions for Rx2EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX2_EQP | | Rx 2 passive equalization. | 0x8 | RW |
| [3:0] | RX2_EQA | | Rx 2 active equalization. | 0x5 | RW |

Rx 3 Active and Passive Equalization Control Register 0 Register

Address: 0x83, Reset: 0x85, Name: Rx3EqCtrl

Rx 3 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 54. Bit Descriptions for Rx3EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX3_EQP | | Rx 3 passive equalization. | 0x8 | RW |
| [3:0] | RX3_EQA | | Rx 3 active equalization. | 0x5 | RW |

Rx 4 Active and Passive Equalization Control Register 0 Register

Address: 0x84, Reset: 0x85, Name: Rx4EqCtrl

Rx 4 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 55. Bit Descriptions for Rx4EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX4_EQP | | Rx 4 passive equalization. | 0x8 | RW |
| [3:0] | RX4_EQA | | Rx 4 active equalization. | 0x5 | RW |

Rx 5 Active and Passive Equalization Control Register 0 Register

Address: 0x85, Reset: 0x85, Name: Rx5EqCtrl

Rx 5 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 56. Bit Descriptions for Rx5EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX5_EQP | | Rx 5 passive equalization. | 0x8 | RW |
| [3:0] | RX5_EQA | | Rx 5 active equalization. | 0x5 | RW |

Rx 5 TO Rx 0 ENABLE CONTROL REGISTER

Address: 0x86, Reset: 0x00, Name: Rx5to0En

Rx 5 to Rx 0 enable control register. Write a Logic 1 to enable the receiver input. Write a Logic 0 to disable the receiver input.

Table 57. Bit Descriptions for Rx5to0En

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|-------------------------------------|-------|--------|
| [7:6] | UNUSED_86 | | Unused register bits. | 0x0 | RW |
| 5 | RX5EN | | Rx 5 enable. | 0x0 | RW |
| 4 | RX4EN | | Rx 4 enable. | 0x0 | RW |
| 3 | RX3EN | | Rx 3 enable. | 0x0 | RW |
| 2 | RX2EN | | Rx 2 enable. | 0x0 | RW |
| 1 | RX1EN | | Rx 1 enable. | 0x0 | RW |
| 0 | RX0EN | 0 1 | Rx 0 enable. Disabled Enabled | 0x0 | RW |

Rx 5 TO Rx 0 EQUALIZER ENABLE CONTROL REGISTER

Address: 0x87, Reset: 0x00, Name: Rx5to0EqEn

Rx 5 to Rx 0 receiver equalizer enable register. Write a Logic 1 to enable the receiver equalizer. Write a Logic 0 to bypass the receiver equalizer.

Table 58. Bit Descriptions for Rx5to0EqEn

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|---|-------|--------|
| [7:6] | UNUSED_87 | | Unused register bits. | 0x0 | RW |
| 5 | RX5EQEN | | Rx 5 EQ enable. | 0x0 | RW |
| 4 | RX4EQEN | | Rx 4 EQ enable. | 0x0 | RW |
| 3 | RX3EQEN | | Rx 3 EQ enable. | 0x0 | RW |
| 2 | RX2EQEN | | Rx 2 EQ enable. | 0x0 | RW |
| 1 | RX1EQEN | | Rx 1 EQ enable. | 0x0 | RW |
| 0 | RX0EQEN | 0 1 | Rx 0 EQ enable. Disabled (Bypassed) Enabled | 0x0 | RW |

Rx 5 TO Rx 0 LOS ENABLE CONTROL REGISTER

Address: 0x88, Reset: 0x40, Name: Rx5to0LOSEn

Rx 5 to Rx 0 loss of signal (LOS) detector enable register. Write a Logic 1 to enable the receiver LOS detector. Write a Logic 0 to disable the receiver LOS detector.

Table 59. Bit Descriptions for Rx5to0LOSEn

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------------|----------|---|-------|--------|
| 7 | UNUSED_88 | | Unused register bit. | 0x0 | RW |
| 6 | RX5TO0LOSREFEN | | Rx 5 to Rx 0 LOS reference enable. | 0x1 | RW |
| 5 | RX5LOSEN | | Rx 5 LOS enable. | 0x0 | RW |
| 4 | RX4LOSEN | | Rx 4 LOS enable. | 0x0 | RW |
| 3 | RX3LOSEN | | Rx 3 LOS enable. | 0x0 | RW |
| 2 | RX2LOSEN | | Rx 2 LOS enable. | 0x0 | RW |
| 1 | RX1LOSEN | | Rx 1 LOS enable. | 0x0 | RW |
| 0 | RX0LOSEN | 0 1 | Rx 0 LOS enable. Disabled Enabled | 0x0 | RW |

Rx 5 TO Rx 0 LOS TIME CONTROL REGISTERS***Rx 1 to Rx 0 LOS Time Control Register***

Address: 0x89, Reset: 0x99, Name: Rx1to0LOSTimeCtrl

Rx 1 and Rx 0 loss of signal (LOS) event time control register. Controls the time delay of transmitter squelch when an LOS event is detected.

Table 60. Bit Descriptions for Rx1to0LOSTimeCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|----------------|-------|--------|
| [7:4] | RX1_LOS_TIME | | Rx 1 LOS time | 0x9 | RW |
| [3:0] | RX0_LOS_TIME | | Rx 0 LOS time. | 0x9 | RW |
| | | 0000 | 2.5 ns | | |
| | | 0001 | 5.0 ns | | |
| | | 0010 | 10.0 ns | | |
| | | 0011 | 20.0 ns | | |
| | | 0100 | 40.0 ns | | |
| | | 0101 | 80.0 ns | | |
| | | 0110 | 160.0 ns | | |
| | | 0111 | 320.0 ns | | |
| | | 1000 | 460.0 ns | | |
| | | 1001 | 1280.0 ns | | |
| | | 1010 | 2560.0 ns | | |
| | | 1011 | 5120.0 ns | | |
| | | 1100 | 10,240.0 ns | | |
| | | 1101 | 20,480.0 ns | | |
| | | 1110 | 40,960.0 ns | | |
| | | 1111 | 81,920.0 ns | | |

Rx 3 to Rx 2 LOS Time Control Register

Address: 0x8A, Reset: 0x99, Name: Rx3to2LOSTimeCtrl

Rx 3 and Rx 2 loss of signal (LOS) event time control register. Controls the time delay of the transmitter squelch when an LOS event is detected.

Table 61. Bit Descriptions for Rx3to2LOSTimeCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|----------------|-------|--------|
| [7:4] | RX3_LOS_TIME | | Rx 3 LOS time. | 0x9 | RW |
| [3:0] | RX2_LOS_TIME | | Rx 2 LOS time. | 0x9 | RW |

Rx 5 to Rx 4 LOS Time Control Register

Address: 0x8B, Reset: 0x99, Name: Rx5to4LOSTimeCtrl

Rx 5 and Rx 4 loss of signal (LOS) event time control register. Controls the time delay of the transmitter squelch when an LOS event is detected.

Table 62. Bit Descriptions for Rx5to4LOSTimeCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|----------------|-------|--------|
| [7:4] | RX5_LOS_TIME | | Rx 5 LOS time. | 0x9 | RW |
| [3:0] | RX4_LOS_TIME | | Rx 4 LOS time. | 0x9 | RW |

Rx 5 TO Rx 0 LOS STATUS REGISTER

Address: 0x8C, Reset: 0x00, Name: Rx5to0LOSSta

Rx 5 to Rx 0 loss of signal (LOS) status register. Read register to determine if an active signal is detected on Rx 5 to Rx 0.

Table 63. Bit Descriptions for Rx5to0LOSSta

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------|---|-------|--------|
| 7 | UNUSED_8C | | Unused register bits. | 0x0 | RW |
| [5:0] | LOS5TO0STA | 0 1 | LOS status for Rx 5 to Rx 0. LOS Deasserted; Active Signal Detected LOS Asserted; Signal Not Detected | 0x0 | R |

Rx 5 TO Rx 0 LOS STICKY STATUS REGISTER

Address: 0x8D, Reset: 0x00, Name: Rx5to0LOSStkySta

Rx 5 to Rx 0 loss of signal (LOS) sticky status register. Read register to determine if an LOS event has been detected on Rx 5 to Rx 0.

Table 64. Bit Descriptions for Rx5to0LOSStkySta

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------------|----------|---|-------|--------|
| 7 | UNUSED_8D | | Unused register bits. | 0x0 | RW |
| [5:0] | LOS5TO0STKYSTA | 0 1 | LOS sticky status for Rx 5 to Rx 0. LOS Event Has Not Occurred LOS Event Has Occurred | 0x0 | R |

Rx 5 TO Rx 0 LOS ASSERT AND DEASSERT LEVEL CONTROL REGISTER

Address: 0x8E, Reset: 0x62, Name: Rx5to0LOSLvlCtrl

Loss of signal (LOS) detect programmable assert and deassert levels. Recommended setting: deassert = 6; assert = 2 (0x62).

Table 65. Bit Descriptions for Rx5to0LOSLvlCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|---|--|-------|--------|
| [7:4] | LOS_DEASSERT | | LOS deassert level. Loss of signal (LOS) deassert level. LOS status bit is deasserted when input signal level is above the deassert level. Range of LOS deassert levels is 0 mV to 300 mV in 25 mV increments. Voltage levels are differential peak-to-peak. Always set the deassert level higher than the assert level. | 0x6 | RW |
| [3:0] | LOS_ASSERT | 0x0 0x1 0x2 0x3 0x4 0x5 0x6 0x7 0x8 0x9 0xA 0xB 0xC | LOS assert level. Loss of signal (LOS) assert level. LOS status bit is asserted when input signal level is below the assert level. Range of LOS assert levels is 0 mV to 300 mV in 25 mV increments. Voltage levels are differential peak-to-peak. Always set the assert level lower than the deassert level. 0 mV 25 mV 50 mV 75 mV 100 mV 125 mV 150 mV 175 mV 200 mV 225 mV 250 mV 275 mV 300 mV | 0x2 | RW |

Rx 5 TO Rx 0 LOS IRQ ENABLE REGISTER**Address: 0x8F, Reset: 0x00, Name: Rx5to0LOSIRQEn**

Rx 5 to Rx 0 loss of signal (LOS) IRQ enable register. Write a Logic 1 to enable the update of the IRQ control pin status when an LOS event is detected on Rx 5 to Rx 0. The LOS IRQ control pin status is determined by the wire-ORed value of the Rx LOS event status of Rx 11 to Rx 0.

Table 66. Bit Descriptions for Rx5to0LOSIRQEn

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------|--|-------|--------|
| [7:6] | UNUSED_8F | | Unused register bits. | 0x0 | RW |
| 5 | RX5LOSIRQEN | | Rx5 LOS IRQ enable. | 0x0 | RW |
| 4 | RX4LOSIRQEN | | Rx4 LOS IRQ enable. | 0x0 | RW |
| 3 | RX3LOSIRQEN | | Rx3 LOS IRQ enable. | 0x0 | RW |
| 2 | RX2LOSIRQEN | | Rx2 LOS IRQ enable. | 0x0 | RW |
| 1 | RX1LOSIRQEN | | Rx1 LOS IRQ enable. | 0x0 | RW |
| 0 | RX0LOSIRQEN | 0 1 | Rx0 LOS IRQ enable. Disabled Enabled | 0x0 | RW |

Rx 6 TO Rx 11 ACTIVE AND PASSIVE EQUALIZATION CONTROL REGISTERS**Rx 6 Active and Passive Equalization Control Register 0 Register****Address: 0x90, Reset: 0x85, Name: Rx6EqCtrl**

Rx 6 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 67. Bit Descriptions for RX6EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX6_EQP | | Rx 6 passive equalization. | 0x8 | RW |
| [3:0] | RX6_EQA | | Rx 6 active equalization. | 0x5 | RW |

Rx 7 Active and Passive Equalization Control Register 0 Register**Address: 0x91, Reset: 0x85, Name: Rx7EqCtrl**

Rx 7 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 68. Bit Descriptions for RX7EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX7_EQP | | Rx 7 passive equalization. | 0x8 | RW |
| [3:0] | RX7_EQA | | Rx 7 active equalization. | 0x5 | RW |

Rx 8 Active and Passive Equalization Control Register 0 Register**Address: 0x92, Reset: 0x85, Name: Rx8EqCtrl**

Rx 8 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 69. Bit Descriptions for Rx8EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX8_EQP | | Rx 8 passive equalization. | 0x8 | RW |
| [3:0] | RX8_EQA | | Rx 8 active equalization. | 0x5 | RW |

Rx 9 Active and Passive Equalization Control Register 0 Register

Address: 0x93, Reset: 0x85, Name: Rx9EqCtrl

Rx 9 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 70. Bit Descriptions for Rx9EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------------|-------|--------|
| [7:4] | RX9_EQP | | Rx 9 passive equalization. | 0x8 | RW |
| [3:0] | RX9_EQA | | Rx 9 active equalization. | 0x5 | RW |

Rx 10 Active and Passive Equalization Control Register 0 Register

Address: 0x94, Reset: 0x85, Name: Rx10EqCtrl

Rx 10 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 71. Bit Descriptions for Rx10EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|-----------------------------|-------|--------|
| [7:4] | RX10_EQP | | Rx 10 passive equalization. | 0x8 | RW |
| [3:0] | RX10_EQA | | Rx 10 active equalization. | 0x5 | RW |

Rx 11 Active and Passive Equalization Control Register 0 Register

Address: 0x95, Reset: 0x85, Name: Rx11EqCtrl

Rx 11 equalization control register. Configures the high frequency boost of the active and passive equalizer stages. The total high frequency boost is the addition of the boost of the two stages.

Table 72. Bit Descriptions for Rx11EqCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|-----------------------------|-------|--------|
| [7:4] | RX11_EQP | | Rx 11 passive equalization. | 0x8 | RW |
| [3:0] | RX11_EQA | | Rx 11 active equalization. | 0x5 | RW |

Rx 11 TO Rx 6 ENABLE CONTROL REGISTER

Address: 0x96, Reset: 0x00, Name: Rx11to6En

Rx 11 to Rx 6 enable control register. Write a Logic 1 to enable receiver input. Write a Logic 0 to disable receiver input.

Table 73. Bit Descriptions for Rx11to6En

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|-------------------------------------|-------|--------|
| [7:6] | UNUSED_96 | | Unused register bits. | 0x0 | RW |
| 5 | RX11EN | | Rx 11 enable. | 0x0 | RW |
| 4 | RX10EN | | Rx 10 enable. | 0x0 | RW |
| 3 | RX9EN | | Rx 9 enable. | 0x0 | RW |
| 2 | RX8EN | | Rx 8 enable. | 0x0 | RW |
| 1 | RX7EN | | Rx 7 enable. | 0x0 | RW |
| 0 | RX6EN | 0 1 | Rx 6 enable. Disabled Enabled | 0x0 | RW |

Rx 11 TO Rx 6 EQUALIZER ENABLE CONTROL REGISTER

Address: 0x97, Reset: 0x00, Name: Rx11to6EqEn

Rx 11 to Rx 6 receiver equalizer enable. Write a Logic 1 to enable the receiver equalizer. Write a Logic 0 to bypass the receiver equalizer.

Table 74. Bit Descriptions for Rx11to6EqEn

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|---|-------|--------|
| [7:6] | UNUSED_97 | | Unused register bits. | 0x0 | RW |
| 5 | RX11EQEN | | Rx 11 EQ enable. | 0x0 | RW |
| 4 | RX10EQEN | | Rx 10 EQ enable. | 0x0 | RW |
| 3 | RX9EQEN | | Rx 9 EQ enable. | 0x0 | RW |
| 2 | RX8EQEN | | Rx 8 EQ enable. | 0x0 | RW |
| 1 | RX7EQEN | | Rx 7 EQ enable. | 0x0 | RW |
| 0 | RX6EQEN | 0 1 | Rx 6 EQ enable. Disabled (Bypassed) Enabled | 0x0 | RW |

Rx 11 TO Rx 6 LOS ENABLE CONTROL REGISTER

Address: 0x98, Reset: 0x40, Name: Rx11to6LOSEn

Rx 11 to Rx 6 receiver loss of signal (LOS) detector enable register. Write a Logic 1 to enable the receiver LOS detector. Write a Logic 0 to disable the receiver LOS detector.

Table 75. Bit Descriptions for Rx11to6LOSEn

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-----------------|----------|---|-------|--------|
| 7 | UNUSED_98 | | Unused register bit. | 0x0 | RW |
| 6 | RX11TO6LOSREFEN | | Rx 11 to Rx 6 LOS reference enable. | 0x1 | RW |
| 5 | RX11LOSEN | | Rx 11 LOS enable. | 0x0 | RW |
| 4 | RX10LOSEN | | Rx 10 LOS enable. | 0x0 | RW |
| 3 | RX9LOSEN | | Rx 9 LOS enable. | 0x0 | RW |
| 2 | RX8LOSEN | | Rx 8 LOS enable. | 0x0 | RW |
| 1 | RX7LOSEN | | Rx 7 LOS enable. | 0x0 | RW |
| 0 | RX6LOSEN | 0 1 | Rx 6 LOS enable. Disabled Enabled | 0x0 | RW |

Rx 11 TO Rx 6 LOS TIME CONTROL REGISTERS***Rx 7 to Rx 6 LOS Time Control Register***

Address: 0x99, Reset: 0x99, Name: Rx7to6LOSTimeCtrl

Rx 7 and Rx 6 loss of signal (LOS) event time control register. Controls the time delay of transmitter squelch when an LOS event is detected.

Table 76. Bit Descriptions for Rx7to6LOSTimeCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|----------------|-------|--------|
| [7:4] | RX7_LOS_TIME | | Rx 7 LOS time. | 0x9 | RW |
| [3:0] | RX6_LOS_TIME | | Rx 6 LOS time. | 0x9 | RW |
| | | 0000 | 2.5 ns | | |
| | | 0001 | 5.0 ns | | |
| | | 0010 | 10.0 ns | | |
| | | 0011 | 20.0 ns | | |
| | | 0100 | 40.0 ns | | |
| | | 0101 | 80.0 ns | | |
| | | 0110 | 160.0 ns | | |
| | | 0111 | 320.0 ns | | |
| | | 1000 | 460.0 ns | | |
| | | 1001 | 1280.0 ns | | |
| | | 1010 | 2560.0 ns | | |
| | | 1011 | 5120.0 ns | | |
| | | 1100 | 10,240.0 ns | | |
| | | 1101 | 20,480.0 ns | | |
| | | 1110 | 40,960.0 ns | | |
| | | 1111 | 81,920.0 ns | | |

Rx 9 to Rx 8 LOS Time Control Register

Address: 0x9A, Reset: 0x99, Name: Rx9to8LOSTimeCtrl

Rx 9 and Rx 8 loss of signal (LOS) event time control register. Controls the time delay of transmitter squelch when an LOS event is detected.

Table 77. Bit Descriptions for Rx9to8LOSTimeCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|----------------|-------|--------|
| [7:4] | RX9_LOS_TIME | | Rx 9 LOS time. | 0x9 | RW |
| [3:0] | RX8_LOS_TIME | | Rx 8 LOS time. | 0x9 | RW |

Rx 11 to Rx 10 LOS Time Control Register

Address: 0x9B, Reset: 0x99, Name: Rx11to10LOSTimeCtrl

Rx 11 and Rx 10 loss of signal (LOS) event time control register. Controls the time delay of transmitter squelch when an LOS event is detected.

Table 78. Bit Descriptions for Rx11to10LOSTimeCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------|-------|--------|
| [7:4] | RX11_LOS_TIME | | Rx 11 LOS time. | 0x9 | RW |
| [3:0] | RX10_LOS_TIME | | Rx 10 LOS time. | 0x9 | RW |

Rx 11 TO Rx 6 LOS STATUS REGISTER

Address: 0x9C, Reset: 0x00, Name: Rx11to6LOSSta

Rx 11 to Rx 6 loss of signal (LOS) status register. Read register to determine if an active signal is detected on Rx 11 to Rx 6.

Table 79. Bit Descriptions for Rx11to6LOSSta

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------|--|-------|--------|
| 7 | UNUSED_9C | | Unused register bit. | 0x0 | RW |
| [5:0] | LOS11TO6STA | | LOS status for Rx 11 to Rx 6. Loss of signal (LOS) status. LOS status bit is asserted when input signal level is below the assert level. LOS status bit is deasserted when input signal is above the deassert level. | 0x0 | R |
| | | 0 | LOS Deasserted; Active Signal Detected | | |
| | | 1 | LOS Asserted; Signal Not Detected | | |

Rx 11 TO Rx 6 LOS STICKY STATUS REGISTER

Address: 0x9D, Reset: 0x00, Name: Rx11to6LOSStkySta

Rx 11 to Rx 6 loss of signal (LOS) sticky status register. Read register to determine if an LOS event has been detected on Rx 11 to Rx 6.

Table 80. Bit Descriptions for Rx11to6LOSStkySta

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------------|----------|--------------------------------------|-------|--------|
| 7 | UNUSED_9D | | Unused register bits. | 0x0 | RW |
| [5:0] | LOS11TO6STKYSTA | | LOS sticky status for Rx 11 to Rx 6. | 0x0 | R |
| | | 0 | LOS Event Has Not Occurred | | |
| | | 1 | LOS Event Has Occurred | | |

Rx 11 TO Rx 6 LOS ASSERT AND DEASSERT LEVEL CONTROL REGISTER

Address: 0x9E, Reset: 0x62, Name: Rx11to6LOSLvlCtrl

Loss of signal (LOS) detect programmable assert and deassert levels. Recommended setting: deassert = 6, assert = 2 (0x62).

Table 81. Bit Descriptions for Rx11to6LOSLvlCtrl

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|--|-------|--------|
| [7:4] | LOS_DEASSERT | | LOS deassert level. Loss of signal (LOS) deassert level. LOS status bit is deasserted when input signal level is above the deassert level. Range of LOS deassert levels is 0 mV to 300 mV in 25 mV increments. Voltage levels are differential peak-to-peak. Always set the deassert level higher than the assert level. | 0x6 | RW |
| [3:0] | LOS_ASSERT | | LOS assert level. Loss of signal (LOS) assert level. LOS status bit is asserted when input signal level is below the assert level. Range of LOS assert levels is 0 mV to 300 mV in 25 mV increments. Voltage levels are differential peak-to-peak. Always set the assert level lower than the deassert level. | 0x2 | RW |
| | | 0x0 | 0 mV | | |
| | | 0x1 | 25 mV | | |
| | | 0x2 | 50 mV | | |
| | | 0x3 | 75 mV | | |
| | | 0x4 | 100 mV | | |
| | | 0x5 | 125 mV | | |
| | | 0x6 | 150 mV | | |
| | | 0x7 | 175 mV | | |
| | | 0x8 | 200 mV | | |
| | | 0x9 | 225 mV | | |
| | | 0xA | 250 mV | | |
| | | 0xB | 275 mV | | |
| | | 0xC | 300 mV | | |

Rx 11 TO Rx 6 LOS IRQ ENABLE REGISTER**Address: 0x9F, Reset: 0x00, Name: Rx11to6LOSIRQEn**

Rx 11 to Rx 6 loss of signal (LOS) IRQ enable register. Write a Logic 1 to enable the update of the IRQ control pin status when an LOS event is detected on Rx 11 to Rx 6. The LOS IRQ control pin status is determined by the wire-OR'd value of the receiver LOS event status of Rx 11 to Rx 6.

Table 82. Bit Descriptions for Rx11to6LOSIRQEn

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [7:6] | UNUSED_8F | | Unused register bits. | 0x0 | RW |
| 5 | RX11LOSIRQEN | | Rx 11 LOS IRQ enable. | 0x0 | RW |
| 4 | RX10LOSIRQEN | | Rx 10 LOS IRQ enable. | 0x0 | RW |
| 3 | RX9LOSIRQEN | | Rx 9 LOS IRQ enable. | 0x0 | RW |
| 2 | RX8LOSIRQEN | | Rx 8 LOS IRQ enable. | 0x0 | RW |
| 1 | RX7LOSIRQEN | | Rx 7 LOS IRQ enable. | 0x0 | RW |
| 0 | RX6LOSIRQEN | 0 1 | Rx 6 LOS IRQ enable. Disabled Enabled | 0x0 | RW |

Rx OFFSET CALIBRATION CONTROL REGISTERS**Rx 5 to Rx 0 Offset Calibration Control Register****Address: 0xA0, Reset: 0x00, Name: Rx5to0OffsetCal**

Rx 5 to Rx 0 offset calibration register. Write a Logic 1 to disable the duty cycle distortion (DCD) calibration circuit on Rx 5 to Rx 0. Write a Logic 0 to enable the duty cycle distortion (DCD) calibration circuit on Rx 5 to Rx 0.

Table 83. Bit Descriptions for Rx5to0OffsetCal

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|--|-------|--------|
| [7:6] | UNUSED_A0 | | Unused register bits. | 0x0 | RW |
| 5 | RX5OCAL | | Rx 5 offset calibration enable. | 0x0 | RW |
| 4 | RX4OCAL | | Rx 4 offset calibration enable. | 0x0 | RW |
| 3 | RX3OCAL | | Rx 3 offset calibration enable. | 0x0 | RW |
| 2 | RX2OCAL | | Rx 2 offset calibration enable. | 0x0 | RW |
| 1 | RX1OCAL | | Rx 1 offset calibration enable. | 0x0 | RW |
| 0 | RX0OCAL | 0 1 | Rx 0 offset calibration enable. Disabled Enabled | 0x0 | RW |

Rx 11 to Rx 6 Offset Calibration Control Register**Address: 0xA8, Reset: 0x00, Name: Rx11to6OffsetCal**

Rx 11 to Rx 6 offset calibration register. Write a Logic 1 to disable the duty cycle distortion (DCD) calibration circuit on Rx 11 to Rx 6. Write a Logic 0 to enable the duty cycle distortion (DCD) calibration circuit on Rx 11 to Rx 6.

Table 84. Bit Descriptions for Rx11to6OffsetCal

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------|--|-------|--------|
| [7:6] | UNUSED_A8 | | Unused register bits. | 0x0 | RW |
| 5 | RX11OCAL | | Rx 11 offset calibration enable. | 0x0 | RW |
| 4 | RX10OCAL | | Rx 10 offset calibration enable. | 0x0 | RW |
| 3 | RX9OCAL | | Rx 9 offset calibration enable. | 0x0 | RW |
| 2 | RX8OCAL | | Rx 8 offset calibration enable. | 0x0 | RW |
| 1 | RX7OCAL | | Rx 7 offset calibration enable. | 0x0 | RW |
| 0 | RX6OCAL | 0 1 | Rx 6 offset calibration enable. Disabled Enabled | 0x0 | RW |

XPT MAP A Tx LANE SELECT REGISTERS***XPT Map A Tx 0 and XPT Map A Tx 1 Lane Select Register***

Address: 0xB0, Reset: 0x10, Name: XPT_MapA_Out_1_0

XPT Map A Tx 1 and XPT Map A Tx 0 lane select register. Programs the input lane connection to the Tx 1 and Tx 0 lanes.

Table 85. Bit Descriptions for XPT_MapA_Out_1_0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPA_OUT1 | | XPT Map A Tx 1 lane select. | 0x1 | RW |
| [3:0] | XPT_MAPA_OUT0 | | XPT Map A Tx 0 lane select. | 0x0 | RW |
| | | 0000 | OUT[n] = Input 0 | | |
| | | 0001 | OUT[n] = Input 1 | | |
| | | 0010 | OUT[n] = Input 2 | | |
| | | 0011 | OUT[n] = Input 3 | | |
| | | 0100 | OUT[n] = Input 4 | | |
| | | 0101 | OUT[n] = Input 5 | | |
| | | 0110 | OUT[n] = Input 6 | | |
| | | 0111 | OUT[n] = Input 7 | | |
| | | 1000 | OUT[n] = Input 8 | | |
| | | 1001 | OUT[n] = Input 9 | | |
| | | 1010 | OUT[n] = Input 10 | | |
| | | 1011 | OUT[n] = Input 11 | | |

XPT Map A Tx 2 and XPT Map A Tx 3 Lane Select Register

Address: 0xB1, Reset: 0x32, Name: XPT_MapA_Out_3_2

XPT Map A Tx 3 and XPT Map A Tx 2 lane select register. Programs the input lane connection to the Tx 3 and Tx 2 lanes.

Table 86. Bit Descriptions for XPT_MapA_Out_3_2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPA_OUT3 | | XPT Map A Tx 3 lane select. | 0x3 | RW |
| [3:0] | XPT_MAPA_OUT2 | | XPT Map A Tx 2 lane select. | 0x2 | RW |

XPT Map A Tx 4 and XPT Map A Tx 5 Lane Select Register

Address: 0xB2, Reset: 0x54, Name: XPT_MapA_Out_5_4

XPT Map A Tx 5 and XPT Map A Tx 4 lane select register. Programs the input lane connection to the Tx 5 and Tx 4 lanes.

Table 87. Bit Descriptions for XPT_MapA_Out_5_4

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPA_OUT5 | | XPT Map A Tx 5 lane select. | 0x5 | RW |
| [3:0] | XPT_MAPA_OUT4 | | XPT Map A Tx 4 lane select. | 0x4 | RW |

XPT Map A Tx 6 and XPT Map A Tx 7 Lane Select Register

Address: 0xB3, Reset: 0x76, Name: XPT_MapA_Out_7_6

XPT Map A Tx 7 and XPT Map A Tx 6 lane select register. Programs the input lane connection to the Tx 7 and Tx 6 lanes.

Table 88. Bit Descriptions for XPT_MapA_Out_7_6

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPA_OUT7 | | XPT Map A Tx 7 lane select. | 0x7 | RW |
| [3:0] | XPT_MAPA_OUT6 | | XPT Map A Tx 6 lane select. | 0x6 | RW |

XPT Map A Tx 8 and XPT Map A Tx 9 Lane Select Register

Address: 0xB4, Reset: 0x98, Name: XPT_MapA_Out_9_8

XPT Map A Tx 9 and XPT Map A Tx 8 lane select register. Programs the input lane connection to the Tx 9 and Tx 8 lanes.

Table 89. Bit Descriptions for XPT_MapA_Out_9_8

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPA_OUT9 | | XPT Map A Tx 9 lane select. | 0x9 | RW |
| [3:0] | XPT_MAPA_OUT8 | | XPT Map A Tx 8 lane select. | 0x8 | RW |

XPT Map A Tx 10 and XPT Map A Tx 11 Lane Select Register

Address: 0xB5, Reset: 0xBA, Name: XPT_MapA_Out_11_10

XPT Map A Tx 11 and XPT Map A Tx 10 lane select register. Programs the input lane connection to the Tx 11 and Tx 10 lanes.

Table 90. Bit Descriptions for XPT_MapA_Out_11_10

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------------|----------|------------------------------|-------|--------|
| [7:4] | XPT_MAPA_OUT11 | | XPT Map A Tx 11 lane select. | 0xB | RW |
| [3:0] | XPT_MAPA_OUT10 | | XPT Map A Tx 10 lane select. | 0xA | RW |

XPT MAP B Tx LANE SELECT REGISTERS**XPT Map B Tx 0 and XPT Map B Tx 1 Lane Select Register**

Address: 0xB8, Reset: 0x23, Name: XPT_MapB_Out_1_0

XPT Map B Tx 1 and XPT Map B Tx 0 lane select register. Programs the input lane connection to the Tx 1 and Tx 0 lanes.

Table 91. Bit Descriptions for XPT_MapB_Out_1_0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPB_OUT1 | | XPT Map B Tx 1 lane select. | 0x2 | RW |
| [3:0] | XPT_MAPB_OUT0 | | XPT Map B Tx 0 lane select. | 0x3 | RW |

XPT Map B Tx 2 and XPT Map B Tx 3 Lane Select Register

Address: 0xB9, Reset: 0x23, Name: XPT_MapB_Out_3_2

XPT Map B Tx 3 and XPT Map B Tx 2 lane select register. Program input lane connection to Tx 3 and Tx 2 lanes.

Table 92. Bit Descriptions for XPT_MapB_Out_3_2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPB_OUT3 | | XPT Map B Tx 3 lane select. | 0x2 | RW |
| [3:0] | XPT_MAPB_OUT2 | | XPT Map B Tx 2 lane select. | 0x3 | RW |

XPT Map B Tx 4 and XPT Map B Tx 5 Lane Select Register

Address: 0xBA, Reset: 0x01, Name: XPT_MapB_Out_5_4

XPT Map B Tx 5 and XPT Map B Tx 4 lane select register. Programs the input lane connection to the Tx 5 and Tx 4 lanes.

Table 93. Bit Descriptions for XPT_MapB_Out_5_4

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPB_OUT5 | | XPT Map B Tx 5 lane select. | 0x0 | RW |
| [3:0] | XPT_MAPB_OUT4 | | XPT Map B Tx 4 lane select. | 0x1 | RW |

XPT Map B Tx 6 and XPT Map B Tx 7 Lane Select Register

Address: 0xBB, Reset: 0x01, Name: XPT_MapB_Out_7_6

XPT Map B Tx 7 and XPT Map B Tx 6 lane select register. Programs the input lane connection to the Tx 7 and Tx 6 lanes.

Table 94. Bit Descriptions for XPT_MapB_Out_7_6

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPB_OUT7 | | XPT Map B Tx 7 lane select. | 0x0 | RW |
| [3:0] | XPT_MAPB_OUT6 | | XPT Map B Tx 6 lane select. | 0x1 | RW |

XPT Map B Tx 8 and XPT Map B Tx 9 Lane Select Register

Address: 0xBC, Reset: 0xAB, Name: XPT_MapB_Out_9_8

XPT Map B Tx 9 and XPT Map B Tx 8 lane select register. Programs the input lane connection to the Tx 9 and Tx 8 lanes.

Table 95. Bit Descriptions for XPT_MapB_Out_9_8

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPB_OUT9 | | XPT Map B Tx 9 lane select. | 0xA | RW |
| [3:0] | XPT_MAPB_OUT8 | | XPT Map B Tx 8 lane select. | 0xB | RW |

XPT Map B Tx 10 and XPT Map B Tx 11 Lane Select Register

Address: 0xBD, Reset: 0x54, Name: XPT_MapB_Out_11_10

XPT Map B Tx 11 and XPT Map B Tx 10 lane select register. Programs the input lane connection to the Tx 11 and Tx 10 lanes.

Table 96. Bit Descriptions for XPT_MapB_Out_11_10

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------------|----------|------------------------------|-------|--------|
| [7:4] | XPT_MAPB_OUT11 | | XPT Map B Tx 11 lane select. | 0x5 | RW |
| [3:0] | XPT_MAPB_OUT10 | | XPT Map B Tx 10 lane select. | 0x4 | RW |

XPT MAP C Tx LANE SELECT REGISTERS**XPT Map C Tx 0 and XPT Map C Tx 1 Lane Select Register**

Address: 0xC0, Reset: 0x23, Name: XPT_MapC_Out_1_0

XPT Map C Tx 1 and XPT Map C Tx 0 lane select register. Programs the input lane connection to the Tx 1 and Tx 0 lanes.

Table 97. Bit Descriptions for XPT_MapC_Out_1_0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPC_OUT1 | | XPT Map C Tx 1 lane select. | 0x2 | RW |
| [3:0] | XPT_MAPC_OUT0 | | XPT Map C Tx 0 lane select. | 0x3 | RW |

XPT Map C Tx 2 and XPT Map C Tx 3 Lane Select Register

Address: 0xC1, Reset: 0x23, Name: XPT_MapC_Out_3_2

XPT Map C Tx 3 and XPT Map C Tx 2 lane select register. Programs the input lane connection to the Tx 3 and Tx 2 lanes.

Table 98. Bit Descriptions for XPT_MapC_Out_3_2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPC_OUT3 | | XPT Map C Tx 3 lane select. | 0x2 | RW |
| [3:0] | XPT_MAPC_OUT2 | | XPT Map C Tx 2 lane select. | 0x3 | RW |

XPT Map C Tx 4 and XPT Map C Tx 5 Lane Select Register

Address: 0xC2, Reset: 0x01, Name: XPT_MapC_Out_5_4

XPT Map C Tx 5 and XPT Map C Tx 4 lane select register. Programs the input lane connection to the Tx 5 and Tx 4 lanes.

Table 99. Bit Descriptions for XPT_MapC_Out_4_5

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPC_OUT5 | | XPT Map C Tx 5 lane select. | 0x0 | RW |
| [3:0] | XPT_MAPC_OUT4 | | XPT Map C Tx 4 lane select. | 0x1 | RW |

XPT Map C Tx 6 and XPT Map C Tx 7 Lane Select Register

Address: 0xC3, Reset: 0x01, Name: XPT_MapC_Out_7_6

XPT Map C Tx 7 and XPT Map C Tx 6 lane select register. Programs the input lane connection to the Tx 7 and Tx 6 lanes.

Table 100. Bit Descriptions for XPT_MapC_Out_7_6

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPC_OUT7 | | XPT Map C Tx 7 lane select. | 0x0 | RW |
| [3:0] | XPT_MAPC_OUT6 | | XPT Map C Tx 6 lane select. | 0x1 | RW |

XPT Map C Tx 8 and XPT Map C Tx 9 Lane Select Register

Address: 0xC4, Reset: 0x89, Name: XPT_MapC_Out_9_8

XPT Map C Tx 9 and XPT Map C Tx 8 lane select register. Programs the input lane connection to the Tx 9 and Tx 8 lanes.

Table 101. Bit Descriptions for XPT_MapC_Out_9_8

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPC_OUT9 | | XPT Map C Tx 9 lane select. | 0x8 | RW |
| [3:0] | XPT_MAPC_OUT8 | | XPT Map C Tx 8 lane select. | 0x9 | RW |

XPT Map C Tx 10 and XPT Map C Tx 11 Lane Select Register

Address: 0xC5, Reset: 0x67, Name: XPT_MapC_Out_11_10

XPT Map C Tx 11 and XPT Map C Tx 10 lane select register. Programs the input lane connection to the Tx 11 and Tx 10 lanes.

Table 102. Bit Descriptions for XPT_MapC_Out_11_10

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------------|----------|------------------------------|-------|--------|
| [7:4] | XPT_MAPC_OUT11 | | XPT Map C Tx 11 lane select. | 0x6 | RW |
| [3:0] | XPT_MAPC_OUT10 | | XPT Map C Tx 10 lane select. | 0x7 | RW |

XPT MAP D Tx LANE SELECT REGISTERS**XPT Map D Tx 0 and XPT Map D Tx 1 Lane Select Register**

Address: 0xC8, Reset: 0x76, Name: XPT_MapD_Out_1_0

XPT Map D Tx 1 and XPT Map D Tx 0 lane select register. Programs the input lane connection to the Tx 1 and Tx 0 lanes.

Table 103. Bit Descriptions for XPT_MapD_Out_1_0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPD_OUT1 | | XPT Map D Tx 1 lane select. | 0x7 | RW |
| [3:0] | XPT_MAPD_OUT0 | | XPT Map D Tx 0 lane select. | 0x6 | RW |

XPT Map D Tx 2 and XPT Map D Tx 3 Lane Select Register

Address: 0xC9, Reset: 0x45, Name: XPT_MapD_Out_3_2

XPT Map D Tx 3 and XPT Map D Tx 2 lane select register. Programs the input lane connection to the Tx 3 and Tx 2 lanes.

Table 104. Bit Descriptions for XPT_MapD_Out_3_2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPD_OUT3 | | XPT Map D Tx 3 lane select. | 0x4 | RW |
| [3:0] | XPT_MAPD_OUT2 | | XPT Map D Tx 2 lane select. | 0x5 | RW |

XPT Map D Tx 4 and XPT Map D Tx 5 Lane Select Register

Address: 0xCA, Reset: 0xBA, Name: XPT_MapD_Out_5_4

XPT Map D Tx 5 and XPT Map D Tx 4 lane select register. Programs the input lane connection to the Tx 5 and Tx 4 lanes.

Table 105. Bit Descriptions for XPT_MapD_Out_5_4

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPD_OUT5 | | XPT Map D Tx 5 lane select. | 0xB | RW |
| [3:0] | XPT_MAPD_OUT4 | | XPT Map D Tx 4 lane select. | 0xA | RW |

XPT Map D Tx 6 and XPT Map D Tx 7 Lane Select Register

Address: 0xCB, Reset: 0x98, Name: XPT_MapD_Out_7_6

XPT Map D Tx 7 and XPT Map D Tx 6 lane select register. Programs the input lane connection to the Tx 7 and Tx 6 lanes.

Table 106. Bit Descriptions for XPT_MapD_Out_7_6

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPD_OUT7 | | XPT Map D Tx 7 lane select. | 0x9 | RW |
| [3:0] | XPT_MAPD_OUT6 | | XPT Map D Tx 6 lane select. | 0x8 | RW |

XPT Map D Tx 8 and XPT Map D Tx 9 Lane Select Register

Address: 0xCC, Reset: 0xAB, Name: XPT_MapD_Out_9_8

XPT Map D Tx 9 and XPT Map D Tx 8 lane select register. Programs the input lane connection to the Tx 9 and Tx 8 lanes.

Table 107. Bit Descriptions for XPT_MapD_Out_9_8

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|-----------------------------|-------|--------|
| [7:4] | XPT_MAPD_OUT9 | | XPT MAP D TX 9 lane select. | 0xA | RW |
| [3:0] | XPT_MAPD_OUT8 | | XPT MAP D TX 8 lane select. | 0xB | RW |

XPT Map D Tx 10 and XPT Map D Tx 11 Lane Select Register

Address: 0xCD, Reset: 0x54, Name: XPT_MapD_Out_11_10

XPT Map D Tx 11 and XPT Map D Tx 10 lane select register. Programs the input lane connection to the Tx 11 and Tx 10 lanes.

Table 108. Bit Descriptions for XPT_MapD_Out_11_10

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------------|----------|------------------------------|-------|--------|
| [7:4] | XPT_MAPD_OUT11 | | XPT Map D Tx 11 lane select. | 0x5 | RW |
| [3:0] | XPT_MAPD_OUT10 | | XPT Map D Tx 10 lane select. | 0x4 | RW |

XPT MAP Tx LANE STATUS REGISTERS***XPT Map Tx 0 and XPT Map Tx 1 Lane Status Register***

Address: 0xD0, Reset: 0x (Undefined), Name: XPT_Map_Status_1_0

XPT Map Tx 1 and XPT Map Tx 0 lane status register. Reads the current state of the XPT connectivity for the Tx 1 and Tx 0 lanes.

Table 109. Bit Descriptions for XPT_Map_Status_1_0

| Bits | Bit Name | Settings | Description | Reset ¹ | Access |
|-------|-----------------|----------|---------------------------|--------------------|--------|
| [7:4] | XPT_MAP_STATUS1 | | XPT Map Tx 1 lane status. | 0xX | R |
| [3:0] | XPT_MAP_STATUS0 | | XPT Map Tx 0 lane status. | 0xX | R |

¹X = don't care.***XPT Map Tx 2 and XPT Map Tx 3 Lane Status Register***

Address: 0xD1, Reset: 0x (Undefined), Name: XPT_Map_Status_3_2

XPT Map Tx 3 and XPT Map Tx 2 lane status register. Reads the current state of the XPT connectivity for the Tx 3 and Tx 2 lanes.

Table 110. Bit Descriptions for XPT_Map_Status_3_2

| Bits | Bit Name | Settings | Description | Reset ¹ | Access |
|-------|-----------------|----------|---------------------------|--------------------|--------|
| [7:4] | XPT_MAP_STATUS3 | | XPT Map Tx 3 lane status. | 0xX | R |
| [3:0] | XPT_MAP_STATUS2 | | XPT Map Tx 2 lane status. | 0xX | R |

¹X = don't care.***XPT Map Tx 4 and XPT Map Tx 5 Lane Status Register***

Address: 0xD2, Reset: 0x (Undefined), Name: XPT_Map_Status_5_4

XPT Map Tx 5 and XPT Map Tx 4 lane status register. Reads the current state of the XPT connectivity for the Tx 5 and Tx 4 lanes.

Table 111. Bit Descriptions for XPT_Map_Status_5_4

| Bits | Bit Name | Settings | Description | Reset ¹ | Access |
|-------|-----------------|----------|---------------------------|--------------------|--------|
| [7:4] | XPT_MAP_STATUS5 | | XPT Map Tx 5 lane status. | 0xX | R |
| [3:0] | XPT_MAP_STATUS4 | | XPT Map Tx 4 lane status. | 0xX | R |

¹X = don't care.***XPT Map Tx 6 and XPT Map Tx 7 Lane Status Register***

Address: 0xD3, Reset: 0x (Undefined), Name: XPT_Map_Status_7_6

XPT Map Tx 7 and XPT Map Tx 6 lane status register. Reads the current state of the XPT connectivity for the Tx 7 and Tx 6 lanes.

Table 112. Bit Descriptions for XPT_Map_Status_7_6

| Bits | Bit Name | Settings | Description | Reset ¹ | Access |
|-------|-----------------|----------|---------------------------|--------------------|--------|
| [7:4] | XPT_MAP_STATUS7 | | XPT Map Tx 7 lane status. | 0xX | R |
| [3:0] | XPT_MAP_STATUS6 | | XPT Map Tx 6 lane status. | 0xX | R |

¹X = don't care.***XPT Map Tx 8 and XPT Map Tx 9 Lane Status Register***

Address: 0xD4, Reset: 0x (Undefined), Name: XPT_Map_Status_9_8

XPT Map Tx 9 and XPT Map Tx 8 lane status register. Reads the current state of the XPT connectivity for the Tx 9 and Tx 8 lanes.

Table 113. Bit Descriptions for XPT_Map_Status_9_8

| Bits | Bit Name | Settings | Description | Reset ¹ | Access |
|-------|-----------------|----------|---------------------------|--------------------|--------|
| [7:4] | XPT_MAP_STATUS9 | | XPT Map Tx 9 lane status. | 0xX | R |
| [3:0] | XPT_MAP_STATUS8 | | XPT Map Tx 8 lane status. | 0xX | R |

¹X = don't care.

XPT Map Tx 10 and XPT Map Tx 11 Lane Status Register

Address: 0xD5, Reset: 0x (Undefined), Name: XPT_Map_Status_11_10

XPT Map Tx 11 and XPT Map Tx 10 lane status register. Reads the current state of the XPT connectivity for the Tx 11 and Tx 10 lanes.

Table 114. Bit Descriptions for XPT_Map_Status_11_10

| Bits | Bit Name | Settings | Description | Reset ¹ | Access |
|-------|------------------|----------|----------------------------|--------------------|--------|
| [7:4] | XPT_MAP_STATUS11 | | XPT Map Tx 11 lane status. | 0xX | R |
| [3:0] | XPT_MAP_STATUS10 | | XPT Map Tx 10 lane status. | 0xX | R |

¹X = don't care.**BOOT FROM EEPROM CONTROL REGISTER**

Address: 0xDD, Reset: 0x00, Name: Boot_from_EEPROM_Control

Boot from EEPROM control register. Write a Logic 1 to disable the EEPROM control pin. Write a Logic 0 to enable the EEPROM control pin.

Table 115. Bit Descriptions for Boot_from_eeprom_control

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------|--|-------|--------|
| [7:1] | UNUSED_DD | | Unused register bits. | 0x0 | RW |
| 0 | IGNORE_EEPROM | 0 1 | EEPROM control pin. Enable Disable | | |

XPT TABLE SELECTION CONTROL REGISTER

Address: 0xDE, Reset: 0x00, Name: XPT_Table_Map

XPT table selection control register. Select active XPT table map.

Table 116. Bit Descriptions for XPT_Table_Map

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------------|----------------------|--|-------|--------|
| [7:5] | UNUSED_DE_1 | | Unused register bits. | 0x0 | RW |
| 4 | XPT_TABLE_SELECT_EN | 0 1 | XPT table select pins enable. Program XPT table map from MAP1 and MAP0 control pins Program XPT table map from software register | | |
| [3:2] | UNUSED_DE_0 | | Unused register bits. | 0x0 | RW |
| [1:0] | XPT_TABLE_SELECT | 00 01 10 11 | XPT table selection control. Map A Selected Map B Selected Map C Selected Map D Selected | 0x0 | RW |

UPDATE XPT TABLE REGISTER

Address: 0xDF, Reset: 0x00, Name: XPT_Update

Software update register. Write a Logic 1 to update the XPT input to output connections as defined in the XPT map registers. This register is write only.

Table 117. Bit Descriptions for XPT_Update

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------|-----------------------|-------|--------|
| [7:1] | UNUSED_DF | | Unused register bits. | 0x0 | RW |
| 0 | UPDATE_XPT | | Update XPT table. | 0x0 | W |

EEPROM CHECKSUM REGISTER

Address: 0xEE, Reset: 0x00, Name: EEPROMChecksum

EEPROM checksum register. Reads the computed checksum value after a load from the EEPROM cycle.

Table 118. Bit Descriptions for EEPROMChecksum

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|------------------------|-------|--------|
| [7:0] | BOOTCHK[7:0] | | EEPROM checksum value. | 0x0 | RW |

EEPROM STATUS REGISTER

Address: 0xEF, Reset: 0x00, Name: EEPROMStatus

EEPROM status register. Checks the load from the EEPROM pass, fail, or completion status.

Table 119. Bit Descriptions for EEPROMStatus

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------|--------------------------------------|-------|--------|
| [7:3] | UNUSED_EF | | Unused register bits. | 0x0 | RW |
| 2 | CHKSUM PASS | | CHKSUM pass status. | 0x0 | R |
| 1 | CHKSUM FAIL | | CHKSUM fail status. | 0x0 | R |
| 0 | EEPROM DONE | | EEPROM load completion check status. | 0x0 | R |

REVISION ID REGISTER

Address: 0xFE, Reset: 0x0B, Name: RevID

Table 120. Bit Descriptions for RevID

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|--------------|-------|--------|
| [7:0] | REVID | | Revision ID. | 0x0 | RW |

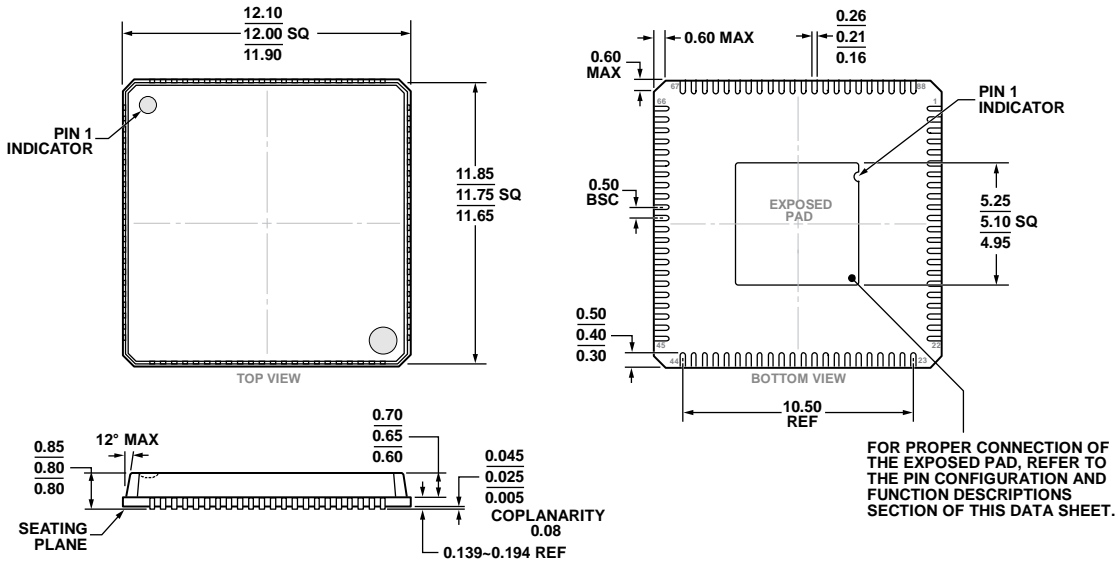
CHIP ID REGISTER

Address: 0xFF, Reset: 0x12, Name: ChipID

Table 121. Bit Descriptions for ChipID

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|-------------|-------|--------|
| [7:0] | CHIPID | | Chip ID. | 0x12 | RW |

PACKAGING AND ORDERING INFORMATION
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220

Figure 79. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
 12 mm × 12 mm Body, Very Thin Quad
 (CP-88-7)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| ADN4612ACPZ | -40°C to +85°C | 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-88-7 |
| ADN4612-EVALZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).