# Low Power Differential ADC Driver

Data Sheet

# ADA4932-1/ADA4932-2

## FEATURES

- High performance at low power
- High speed
  - −3 dB bandwidth of 560 MHz, G = 1
  - 0.1 dB gain flatness to 300 MHz
  - Slew rate: 2800 V/µs, 25% to 75%
  - Fast 0.1% settling time of 9 ns
- Low power: 9.6 mA per amplifier
- Low harmonic distortion
  - 100 dB SFDR at 10 MHz
  - 90 dB SFDR at 20 MHz
- Low input voltage noise: 3.6 nV/√Hz
- ±0.5 mV typical input offset voltage
- Externally adjustable gain
- Can be used with gains less than 1
- Differential-to-differential or single-ended-to-differential operation
- Adjustable output common-mode voltage
- Input common-mode range shifted down by 1 $V_{BE}$
- Wide supply range: +3 V to ±5 V
- Available in 16-lead and 24-lead LFCSP packages

## APPLICATIONS

- ADC drivers
- Single-ended-to-differential converters
- IF and baseband gain blocks
- Differential buffers
- Line drivers

## FUNCTIONAL BLOCK DIAGRAM

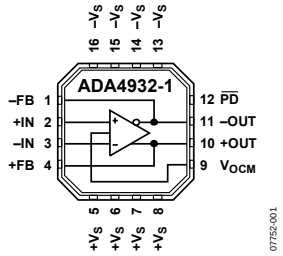


Figure 1. ADA4932-1

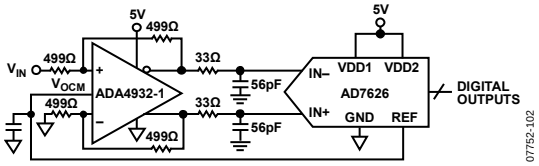


Figure 2. ADC Driver Test Circuit (Data Shown in Figure 3)

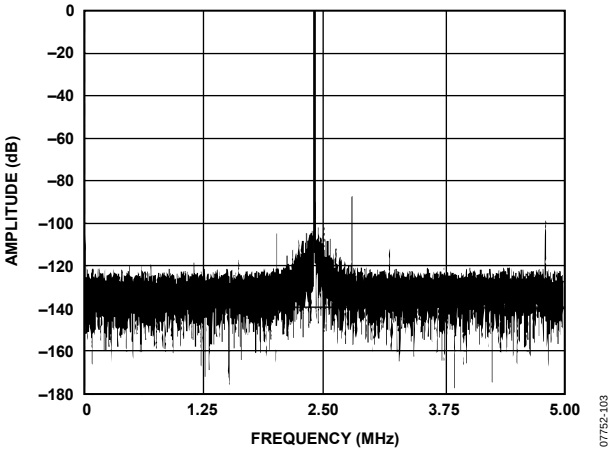


Figure 3. AD7626 Output, 64,000 Point, FFT Plot −1 dBFS Amplitude 2.40173 MHz Input Ton, 10.000 MSPS Sampling Rate

## GENERAL DESCRIPTION

The ADA4932 family is the next generation AD8132 with higher performance, and lower noise and power consumption. It is an ideal choice for driving high performance ADCs as a single-ended-to-differential or differential-to-differential amplifier. The output common-mode voltage is user adjustable by means of an internal common-mode feedback loop, allowing the ADA4932 family output to match the input of the ADC. The internal feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion products.

With the ADA4932 family, differential gain configurations are easily realized with a simple external four-resistor feedback network that determines the closed-loop gain of the amplifier.

The ADA4932 family is fabricated using the Analog Devices, Inc., proprietary silicon-germanium (SiGe) complementary bipolar process, enabling it to achieve low levels of distortion and noise at low power consumption. The low offset and excellent dynamic performance of the ADA4932 family make it well suited for a wide variety of data acquisition and signal processing applications.

The ADA4932-1 is available in a 16-lead LFCSP and the ADA4932-2 is available in a 24-lead LFCSP. The pinout has been optimized to facilitate PCB layout and minimize distortion. The ADA4932 family is specified to operate over the −40°C to +105°C temperature range; both operate on supplies between +3 V and ±5 V.

Rev. D
Document Feedback


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**10/08—Revision 0: Initial Version**

# SPECIFICATIONS

## ±5 V OPERATION

$T_A$ = 25°C, $+V_S$ = 5 V, $-V_S$ = −5 V, $V_{OCM}$ = 0 V, $R_F$ = 499 Ω, $R_G$ = 499 Ω, $R_T$ = 53.6 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 55 for signal definitions.

### *±$D_{IN}$ to $V_{OUT, dm}$ Performance*

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, dm}$ = 0.1 V p-p | | 560 | | MHz |
| | $V_{OUT, dm}$ = 0.1 V p-p, $R_F = R_G$ = 205 Ω | | 1000 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT, dm}$ = 2.0 V p-p | | 360 | | MHz |
| | $V_{OUT, dm}$ = 2.0 V p-p, $R_F = R_G$ = 205 Ω | | 360 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT, dm}$ = 2.0 V p-p, ADA4932-1, $R_L$ = 200 Ω | | 300 | | MHz |
| | $V_{OUT, dm}$ = 2.0 V p-p, ADA4932-2, $R_L$ = 200 Ω | | 100 | | MHz |
| Slew Rate | $V_{OUT, dm}$ = 2 V p-p, 25% to 75% | | 2800 | | V/µs |
| Settling Time to 0.1% | $V_{OUT, dm}$ = 2 V step | | 9 | | ns |
| Overdrive Recovery Time | $V_{IN}$ = 0 V to 5 V ramp, G = 2 | | 20 | | ns |
| NOISE/HARMONIC PERFORMANCE | See Figure 54 for distortion test circuit | | | | |
| Second Harmonic | $V_{OUT, dm}$ = 2 V p-p, 1 MHz | | −110 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 10 MHz | | −100 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 20 MHz | | −90 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 50 MHz | | −72 | | dBc |
| Third Harmonic | $V_{OUT, dm}$ = 2 V p-p, 1 MHz | | −130 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 10 MHz | | −120 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 20 MHz | | −105 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 50 MHz | | −80 | | dBc |
| IMD | $f_1$ = 30 MHz, $f_2$ = 30.1 MHz, $V_{OUT, dm}$ = 2 V p-p | | −91 | | dBc |
| Voltage Noise (RTI) | f = 1 MHz | | 3.6 | | nV/√Hz |
| Input Current Noise | f = 1 MHz | | 1.0 | | pA/√Hz |
| Crosstalk | f = 10 MHz, ADA4932-2 | | −100 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Offset Voltage | $V_{+DIN} = V_{-DIN} = V_{OCM}$ = 0 V | −2.2 | ±0.5 | +2.2 | mV |
| | $T_{MIN}$ to $T_{MAX}$ variation | | −3.7 | | µV/°C |
| Input Bias Current | | −5.2 | −2.5 | −0.1 | µA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | −9.5 | | nA/°C |
| Input Offset Current | | −0.2 | ±0.025 | +0.2 | µA |
| Input Resistance | Differential | | 11 | | MΩ |
| | Common mode | | 16 | | MΩ |
| Input Capacitance | | | 0.5 | | pF |
| Input Common-Mode Voltage Range | | | $-V_S$ + 0.2 to $+V_S$ − 1.8 | | V |
| CMRR | $\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V | | −100 | −87 | dB |
| Open-Loop Gain | | 64 | 66 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Maximum $\Delta V_{OUT}$, single-ended output, $R_F = R_G$ = 10 kΩ, $R_L$ = 1 kΩ | $-V_S$ + 1.4 to $+V_S$ − 1.4 | $-V_S$ + 1.2 to $+V_S$ − 1.2 | | V |
| Linear Output Current | 200 kHz, $R_{L, dm}$ = 10 Ω, SFDR = 68 dB | | 80 | | mA rms |
| Output Balance Error | $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$, $\Delta V_{OUT, dm}$ = 2 V p-p, 1 MHz, see Figure 53 for output balance test circuit | | −64 | −60 | dB |

### *$V_{OCM}$ to $V_{OUT, cm}$ Performance*

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OCM}$ DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, cm}$ = 100 mV p-p | | 270 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT, cm}$ = 2 V p-p | | 105 | | MHz |
| Slew Rate | $V_{IN}$ = 1.5 V to 3.5 V, 25% to 75% | | 410 | | V/µs |
| Input Voltage Noise (RTI) | f = 1 MHz | | 9.6 | | nV/√Hz |
| $V_{OCM}$ INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range | | | $-V_S$ + 1.2 to $+V_S$ − 1.2 | | V |
| Input Resistance | | 22 | 25 | 29 | kΩ |
| Input Offset Voltage | $V_{+DIN} = V_{-DIN}$ = 0 V | −5.1 | ±1 | +5.1 | mV |
| $V_{OCM}$ CMRR | $\Delta V_{OUT, dm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | | −100 | −86 | dB |
| Gain | $\Delta V_{OUT, cm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | 0.995 | 0.998 | 1.000 | V/V |

### *General Performance*

**Table 3.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Operating Range | | 3.0 | | 11 | V |
| Quiescent Current per Amplifier | | 9.0 | 9.6 | 10.1 | mA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | 35 | | µA/°C |
| | Powered down | | 0.9 | 1.0 | mA |
| Power Supply Rejection Ratio | $\Delta V_{OUT, dm}/\Delta V_S$, $\Delta V_S$ = 1 V p-p | | −96 | −84 | dB |
| POWER-DOWN ($\overline{PD}$) | | | | | |
| $\overline{PD}$ Input Voltage | Powered down | | ≤($+V_S$ − 2.5) | | V |
| | Enabled | | ≥($+V_S$ − 1.8) | | V |
| Turn-Off Time | | | 1100 | | ns |
| Turn-On Time | | | 16 | | ns |
| $\overline{PD}$ Pin Bias Current per Amplifier | | | | | |
| Enabled | $\overline{PD}$ = 5 V | −10 | +0.7 | +10 | µA |
| Disabled | $\overline{PD}$ = 0 V | −240 | −195 | −140 | µA |
| OPERATING TEMPERATURE RANGE | | −40 | | +105 | °C |

## 5 V OPERATION

$T_A$ = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{OCM}$ = 2.5 V, $R_F$ = 499 Ω, $R_G$ = 499 Ω, $R_T$ = 53.6 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted. Refer to Figure 55 for signal definitions.

### *±$D_{IN}$ to $V_{OUT, dm}$ Performance*

**Table 4.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, dm}$ = 0.1 V p-p | | 560 | | MHz |
| | $V_{OUT, dm}$ = 0.1 V p-p, $R_F = R_G$ = 205 Ω | | 990 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT, dm}$ = 2.0 V p-p | | 315 | | MHz |
| | $V_{OUT, dm}$ = 2.0 V p-p, $R_F = R_G$ = 205 Ω | | 320 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT, dm}$ = 2.0 V p-p, ADA4932-1, $R_L$ = 200 Ω | | 120 | | MHz |
| | $V_{OUT, dm}$ = 2.0 V p-p, ADA4932-2, $R_L$ = 200 Ω | | 200 | | MHz |
| Slew Rate | $V_{OUT, dm}$ = 2 V p-p, 25% to 75% | | 2200 | | V/µs |
| Settling Time to 0.1% | $V_{OUT, dm}$ = 2 V step | | 10 | | ns |
| Overdrive Recovery Time | $V_{IN}$ = 0 V to 2.5 V ramp, G = 2 | | 20 | | ns |
| NOISE/HARMONIC PERFORMANCE | See Figure 54 for distortion test circuit | | | | |
| Second Harmonic | $V_{OUT, dm}$ = 2 V p-p, 1 MHz | | −110 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 10 MHz | | −100 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 20 MHz | | −90 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 50 MHz | | −72 | | dBc |
| Third Harmonic | $V_{OUT, dm}$ = 2 V p-p, 1 MHz | | −120 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 10 MHz | | −100 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 20 MHz | | −87 | | dBc |
| | $V_{OUT, dm}$ = 2 V p-p, 50 MHz | | −70 | | dBc |
| IMD | $f_1$ = 30 MHz, $f_2$ = 30.1 MHz, $V_{OUT, dm}$ = 2 V p-p | | −91 | | dBc |
| Voltage Noise (RTI) | f = 1 MHz | | 3.6 | | nV/√Hz |
| Input Current Noise | f = 1 MHz | | 1.0 | | pA/√Hz |
| Crosstalk | f = 10 MHz, ADA4932-2 | | −100 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Offset Voltage | $V_{+DIN} = V_{-DIN} = V_{OCM}$ = 2.5 V | −2.2 | ±0.5 | +2.2 | mV |
| | $T_{MIN}$ to $T_{MAX}$ variation | | −3.7 | | µV/°C |
| Input Bias Current | | −5.3 | −3.0 | −0.23 | µA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | −9.5 | | nA/°C |
| Input Offset Current | | −0.25 | ±0.025 | +0.25 | µA |
| Input Resistance | Differential | | 11 | | MΩ |
| | Common mode | | 16 | | MΩ |
| Input Capacitance | | | 0.5 | | pF |
| Input Common-Mode Voltage Range | | | $-V_S$ + 0.2 to $+V_S$ − 1.8 | | V |
| CMRR | $\Delta V_{OUT, dm}/\Delta V_{IN, cm}$, $\Delta V_{IN, cm}$ = ±1 V | | −100 | −87 | dB |
| Open-Loop Gain | | 64 | 66 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Maximum $\Delta V_{OUT}$, single-ended output, $R_F = R_G$ = 10 kΩ, $R_L$ = 1 kΩ | $-V_S$ + 1.15 to $+V_S$ − 1.15 | $-V_S$ + 1.02 to $+V_S$ − 1.02 | | V |
| Linear Output Current | 200 kHz, $R_{L, dm}$ = 10 Ω, SFDR = 67 dB | | 53 | | mA rms |
| Output Balance Error | $\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$, $\Delta V_{OUT, dm}$ = 1 V p-p, 1 MHz, see Figure 53 for output balance test circuit | | −64 | −60 | dB |

### *$V_{OCM}$ to $V_{OUT, cm}$ Performance*

**Table 5.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OCM}$ DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT, cm}$ = 100 mV p-p | | 260 | | MHz |
| −3 dB Large Signal Bandwidth | $V_{OUT, cm}$ = 2 V p-p | | 90 | | MHz |
| Slew Rate | $V_{IN}$ = 1.5 V to 3.5 V, 25% to 75% | | 360 | | V/µs |
| Input Voltage Noise (RTI) | f = 1 MHz | | 9.6 | | nV/√Hz |
| $V_{OCM}$ INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range | | | $-V_S$ + 1.2 to $+V_S$ − 1.2 | | V |
| Input Resistance | | 22 | 25 | 29 | kΩ |
| Input Offset Voltage | $V_{+DIN} = V_{-DIN}$ = 2.5 V | −6.5 | −3.0 | +6.5 | mV |
| $V_{OCM}$ CMRR | $\Delta V_{OUT, dm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | | −100 | −86 | dB |
| Gain | $\Delta V_{OUT, cm}/\Delta V_{OCM}$, $\Delta V_{OCM}$ = ±1 V | 0.995 | 0.998 | 1.000 | V/V |

### *General Performance*

**Table 6.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| Operating Range | | 3.0 | | 11 | V |
| Quiescent Current per Amplifier | | 8.2 | 8.8 | 9.5 | mA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | 35 | | µA/°C |
| | Powered down | | 0.7 | 0.8 | mA |
| Power Supply Rejection Ratio | $\Delta V_{OUT, dm}/\Delta V_S$, $\Delta V_S$ = 1 V p-p | | −96 | −84 | dB |
| POWER-DOWN ($\overline{PD}$) | | | | | |
| $\overline{PD}$ Input Voltage | Powered down | | ≤($+V_S$ − 2.5) | | V |
| | Enabled | | ≥($+V_S$ − 1.8) | | V |
| Turn-Off Time | | | 1100 | | ns |
| Turn-On Time | | | 16 | | ns |
| $\overline{PD}$ Pin Bias Current per Amplifier | | | | | |
| Enabled | $\overline{PD}$ = 5 V | −10 | +0.7 | +10 | µA |
| Disabled | $\overline{PD}$ = 0 V | −100 | −70 | −40 | µA |
| OPERATING TEMPERATURE RANGE | | −40 | | +105 | °C |

# ABSOLUTE MAXIMUM RATINGS

**Table 7.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 11 V |
| Power Dissipation | See Figure 4 |
| Input Current, +IN, −IN, $\overline{PD}$ | ±5 mA |
| Storage Temperature Range | −65°C to +125°C |
| Operating Temperature Range | |
| ADA4932-1 | −40°C to +105°C |
| ADA4932-2 | −40°C to +105°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD 51-7.

**Table 8. Thermal Resistance**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| ADA4932-1, 16-Lead LFCSP (Exposed Pad) | 91 | °C/W |
| ADA4932-2, 24-Lead LFCSP (Exposed Pad) | 65 | °C/W |

## MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4932 family package is limited by the associated rise in junction temperature ($T_J$) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4932 family. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package ($P_D$) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins ($V_S$) times the quiescent current ($I_S$). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing $\theta_{JA}$. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through holes, ground, and power planes reduces $\theta_{JA}$.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the single 16-lead LFCSP (91°C/W) and the dual 24-lead LFCSP (65°C/W) on a JEDEC standard 4-layer board with the exposed pad soldered to a PCB pad that is connected to a solid plane.

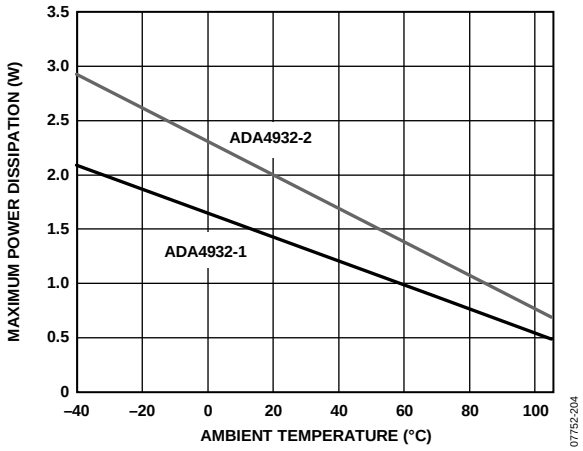
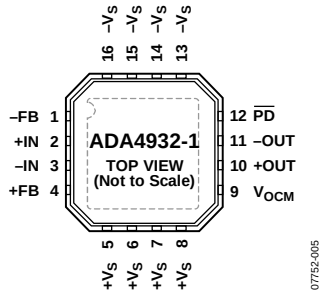



*Figure 4. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board*

## ESD CAUTION

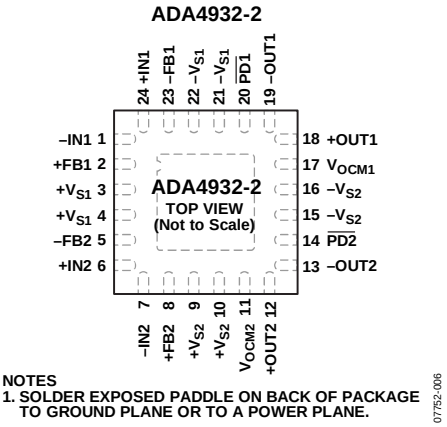
**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS




NOTES
1. SOLDER EXPOSED PADDLE ON BACK OF PACKAGE TO GROUND PLANE OR TO A POWER PLANE.

*Figure 5. ADA4932-1 Pin Configuration*




NOTES
1. SOLDER EXPOSED PADDLE ON BACK OF PACKAGE TO GROUND PLANE OR TO A POWER PLANE.

*Figure 6. ADA4932-2 Pin Configuration*

**Table 9. ADA4932-1 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | –FB | Negative Output for Feedback Component Connection. |
| 2 | +IN | Positive Input Summing Node. |
| 3 | –IN | Negative Input Summing Node. |
| 4 | +FB | Positive Output for Feedback Component Connection. |
| 5 to 8 | $+V_S$ | Positive Supply Voltage. |
| 9 | $V_{OCM}$ | Output Common-Mode Voltage. |
| 10 | +OUT | Positive Output for Load Connection. |
| 11 | –OUT | Negative Output for Load Connection. |
| 12 | $\overline{PD}$ | Power-Down Pin. |
| 13 to 16 | $-V_S$ | Negative Supply Voltage. |
| 17 (EPAD) | Exposed Paddle (EPAD) | Solder the exposed paddle on the back of the package to a ground plane or to a power plane. |

**Table 10. ADA4932-2 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | –IN1 | Negative Input Summing Node 1. |
| 2 | +FB1 | Positive Output Feedback 1. |
| 3, 4 | $+V_{S1}$ | Positive Supply Voltage 1. |
| 5 | –FB2 | Negative Output Feedback 2. |
| 6 | +IN2 | Positive Input Summing Node 2. |
| 7 | –IN2 | Negative Input Summing Node 2. |
| 8 | +FB2 | Positive Output Feedback 2. |
| 9, 10 | $+V_{S2}$ | Positive Supply Voltage 2. |
| 11 | $V_{OCM2}$ | Output Common-Mode Voltage 2. |
| 12 | +OUT2 | Positive Output 2. |
| 13 | –OUT2 | Negative Output 2. |
| 14 | $\overline{PD2}$ | Power-Down Pin 2. |
| 15, 16 | $-V_{S2}$ | Negative Supply Voltage 2. |
| 17 | $V_{OCM1}$ | Output Common-Mode Voltage 1. |
| 18 | +OUT1 | Positive Output 1. |
| 19 | –OUT1 | Negative Output 1. |
| 20 | $\overline{PD1}$ | Power-Down Pin 1. |
| 21, 22 | $-V_{S1}$ | Negative Supply Voltage 1. |
| 23 | –FB1 | Negative Output Feedback 1. |
| 24 | +IN1 | Positive Input Summing Node 1. |
| 25 (EPAD) | Exposed Paddle (EPAD) | Solder the exposed paddle on the back of the package to a ground plane or to a power plane. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $+V_S$ = 5 V, $-V_S$ = −5 V, $V_{OCM}$ = 0 V, $R_G$ = 499 Ω, $R_F$ = 499 Ω, $R_T$ = 53.6 Ω (when used), $R_{L, dm}$ = 1 kΩ, unless otherwise noted. Refer to Figure 52 for test setup. Refer to Figure 55 for signal definitions.

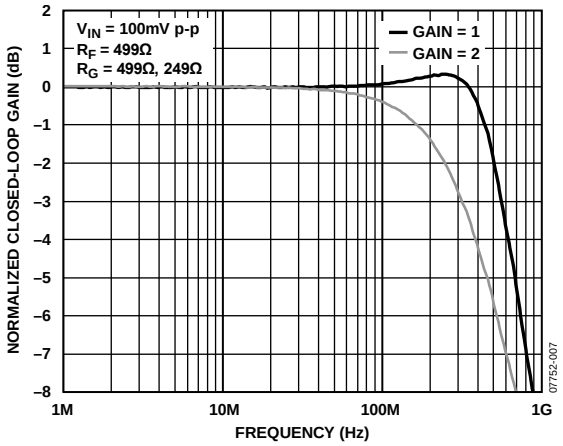



Figure 7. Small Signal Frequency Response for Various Gains

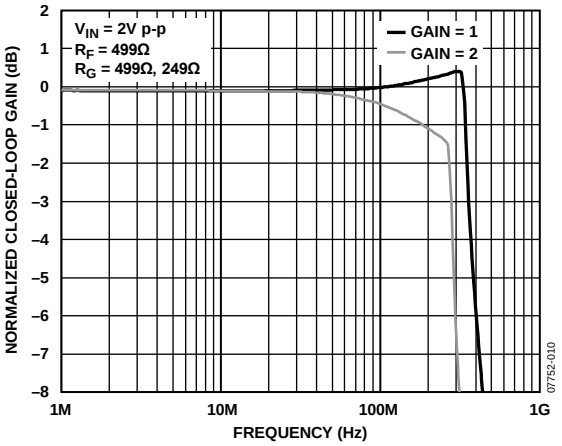



Figure 10. Large Signal Frequency Response for Various Gains

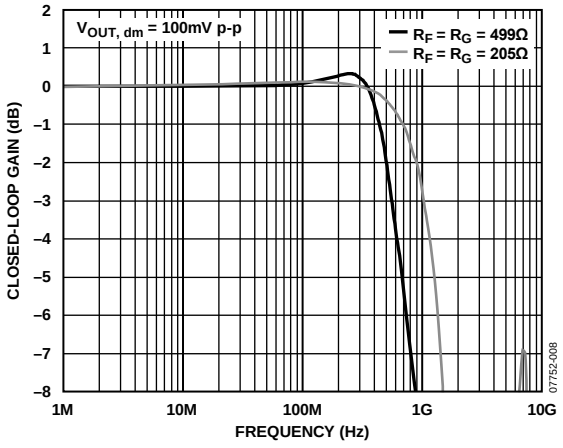



Figure 8. Small Signal Frequency Response for Various $R_F$ and $R_G$

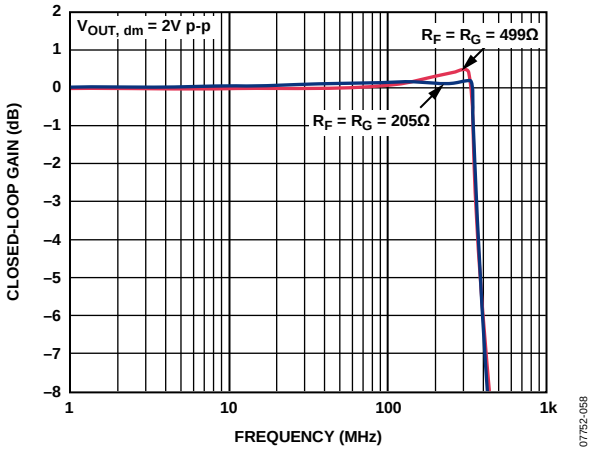



Figure 11. Large Signal Frequency Response for Various $R_F$ and $R_G$

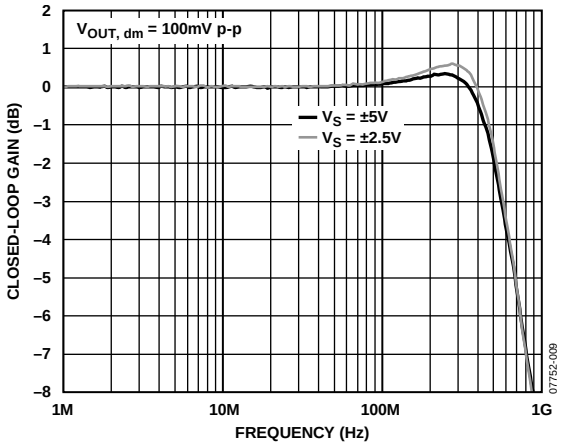



Figure 9. Small Signal Frequency Response for Various Supplies

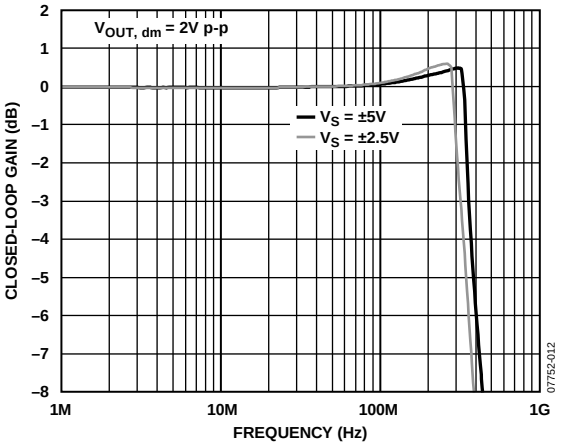



Figure 12. Large Signal Frequency Response for Various Supplies

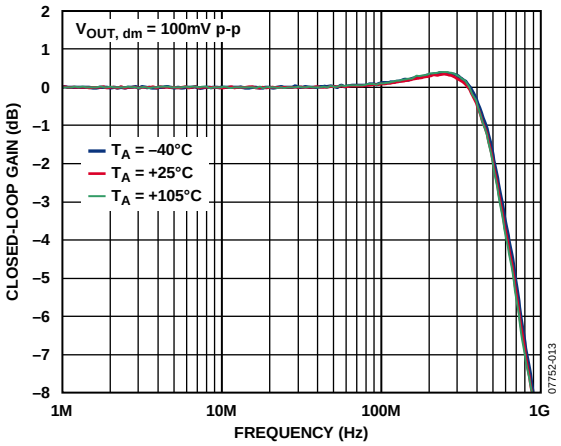



Figure 13. Small Signal Frequency Response for Various Temperatures

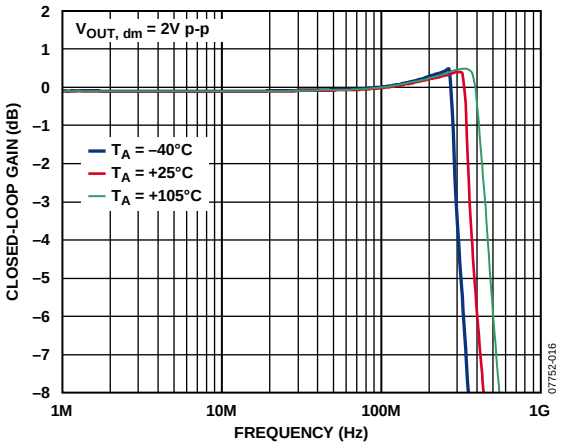



Figure 16. Large Signal Frequency Response for Various Temperatures

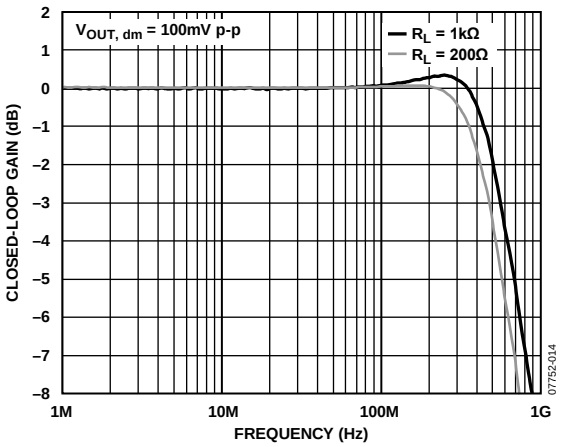



Figure 14. Small Signal Frequency Response at Various Loads

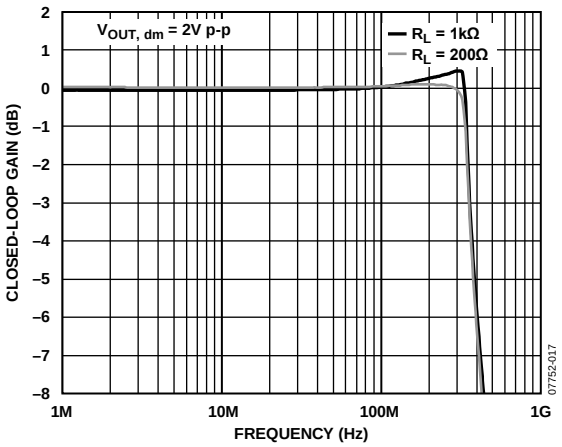



Figure 17. Large Signal Frequency Response at Various Loads

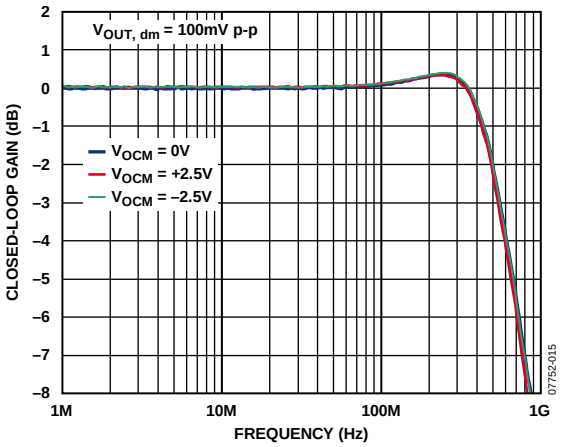



Figure 15. Small Signal Frequency Response for Various $V_{OCM}$ Levels

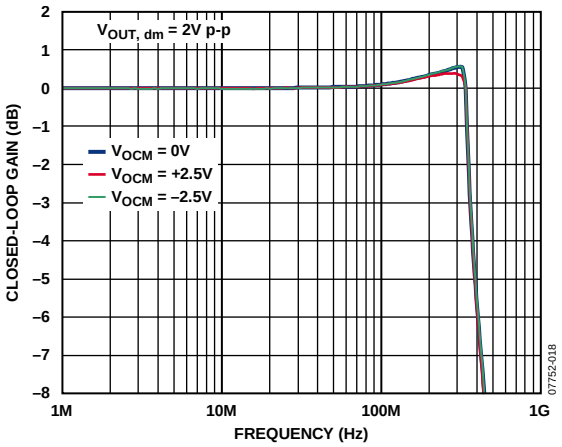



Figure 18. Large Signal Frequency Response for Various $V_{OCM}$ Levels

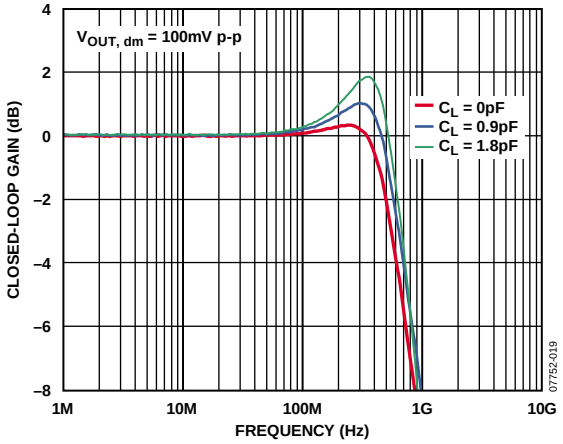



Figure 19. Small Signal Frequency Response at Various Capacitive Loads

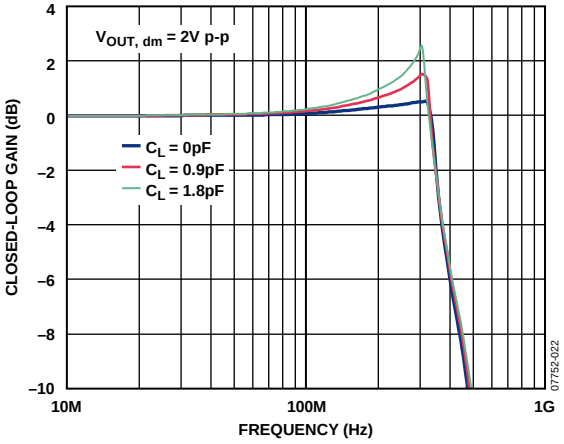



Figure 22. Large Signal Frequency Response at Various Capacitive Loads

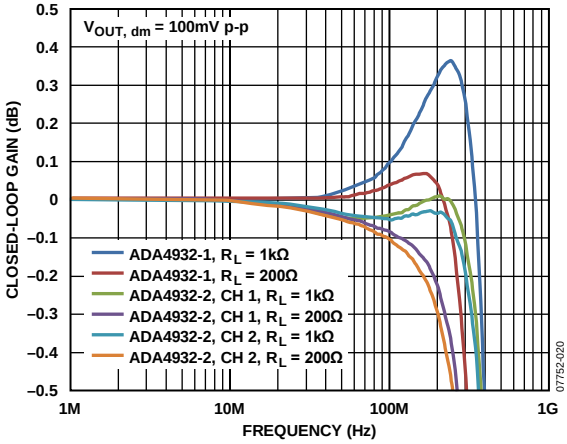



Figure 20. 0.1 dB Flatness Small Signal Frequency Response for Various Loads

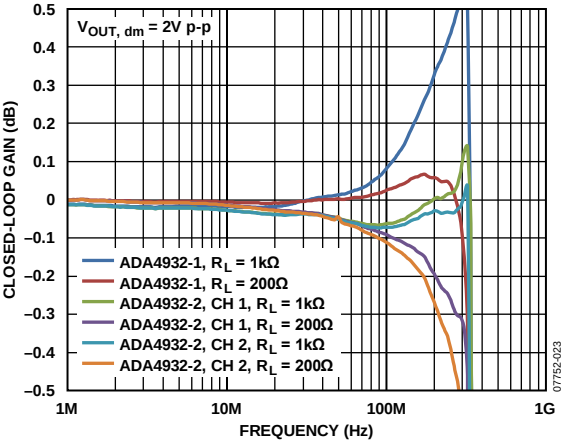



Figure 23. 0.1 dB Flatness Large Signal Frequency Response for Various Loads

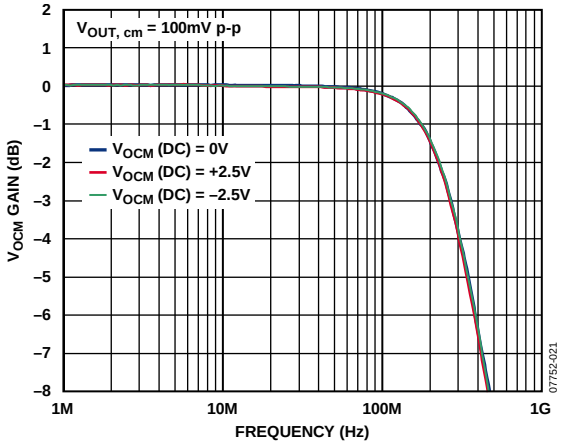



Figure 21. $V_{OCM}$ Small Signal Frequency Response at Various DC Levels

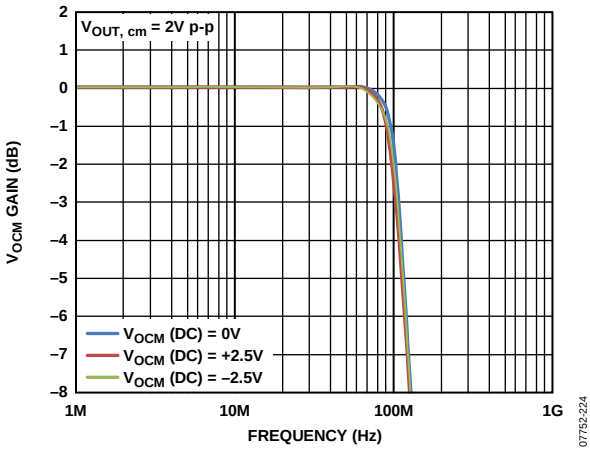



Figure 24. $V_{OCM}$ Large Signal Frequency Response at Various DC Levels

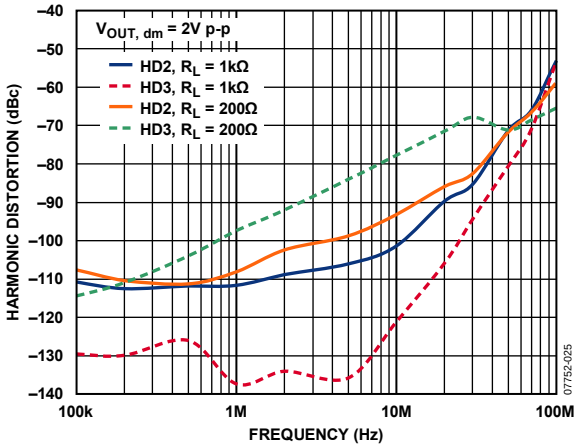



Figure 25. Harmonic Distortion vs. Frequency at Various Loads

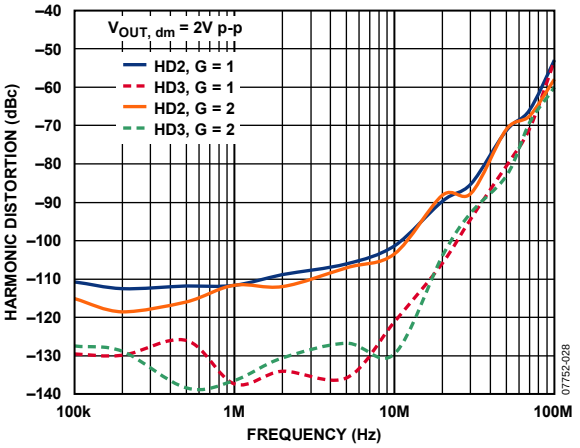



Figure 28. Harmonic Distortion vs. Frequency at Various Gains

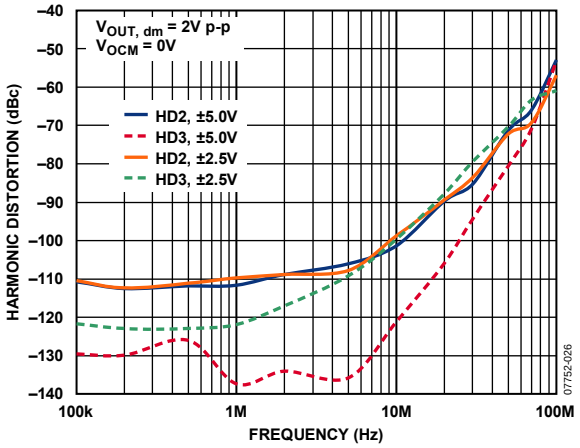



Figure 26. Harmonic Distortion vs. Frequency at Various Supplies

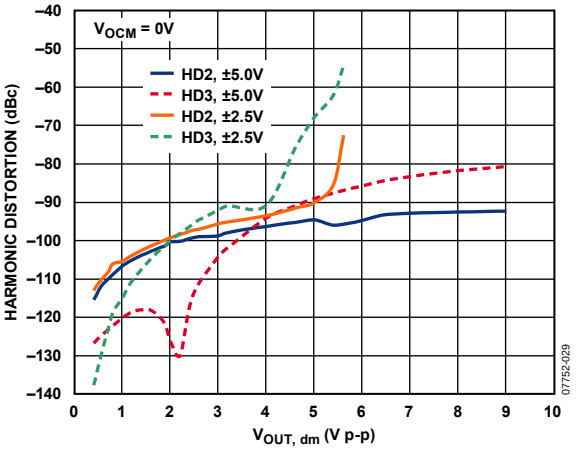



Figure 29. Harmonic Distortion vs. $V_{OUT, dm}$ and Supply Voltage, f = 10 MHz

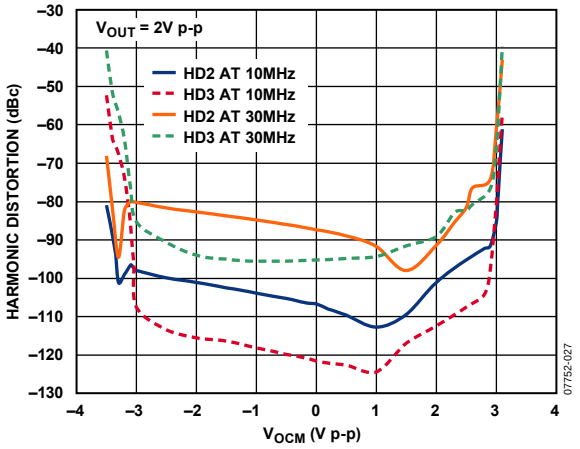



Figure 27. Harmonic Distortion vs. $V_{OCM}$ at Various Frequencies, ±5 V Supplies

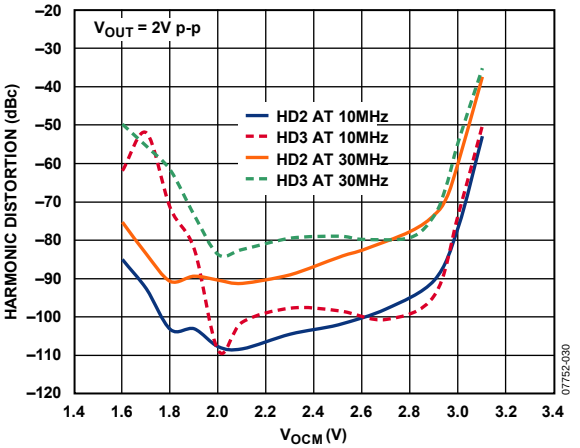



Figure 30. Harmonic Distortion vs. $V_{OCM}$ at Various Frequencies, +5 V Supply

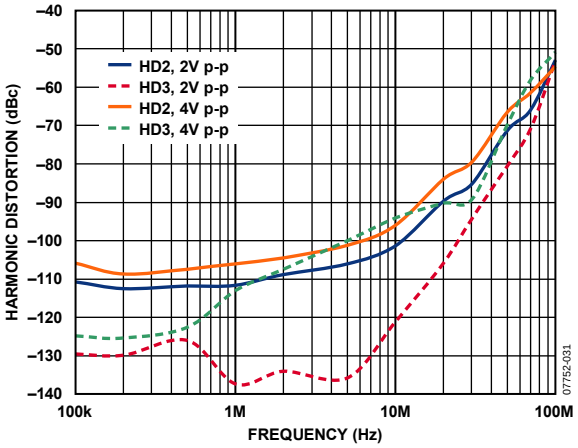



Figure 31. Harmonic Distortion vs. Frequency at Various $V_{OUT, dm}$

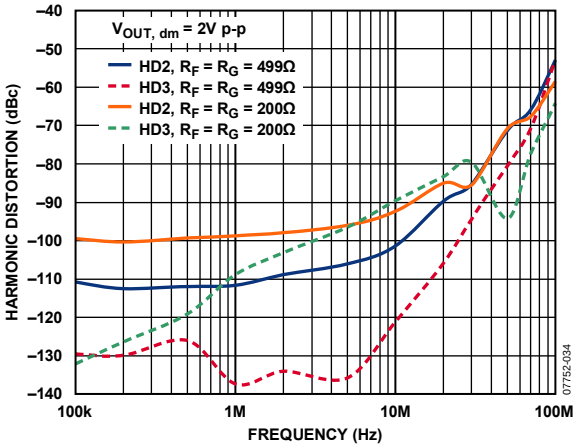



Figure 34. Harmonic Distortion vs. Frequency at Various $R_F$ and $R_G$

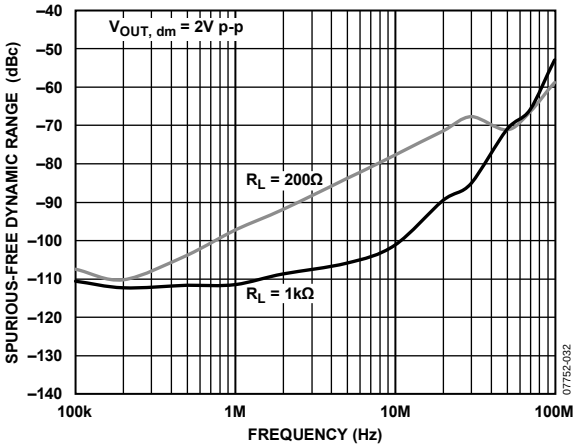



Figure 32. Spurious-Free Dynamic Range vs. Frequency at Various Loads

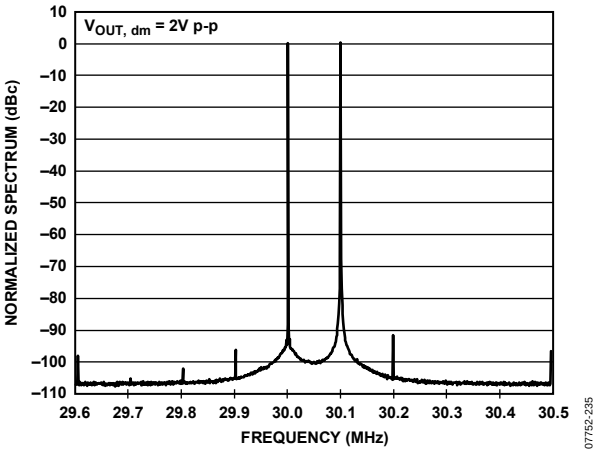



Figure 35. 30 MHz Intermodulation Distortion

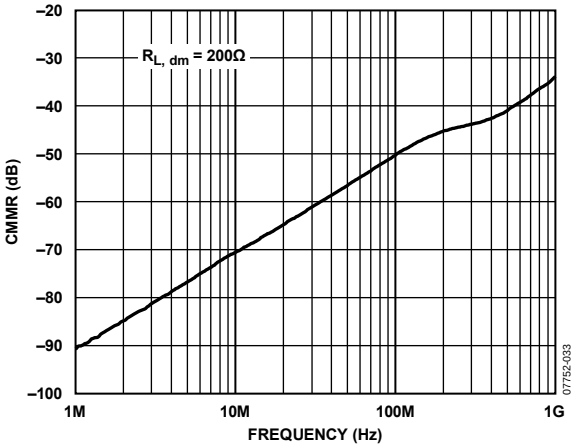



Figure 33. CMRR vs. Frequency

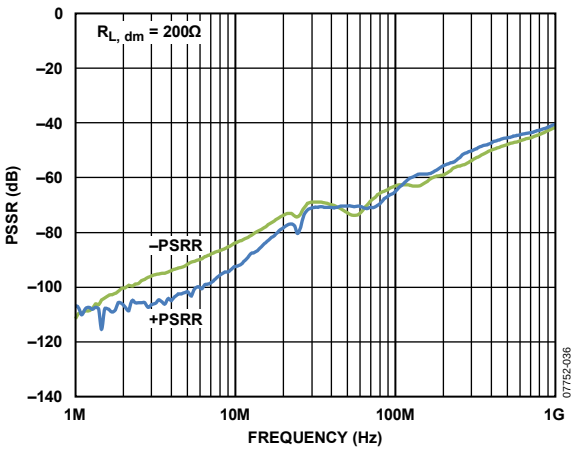



Figure 36. PSRR vs. Frequency

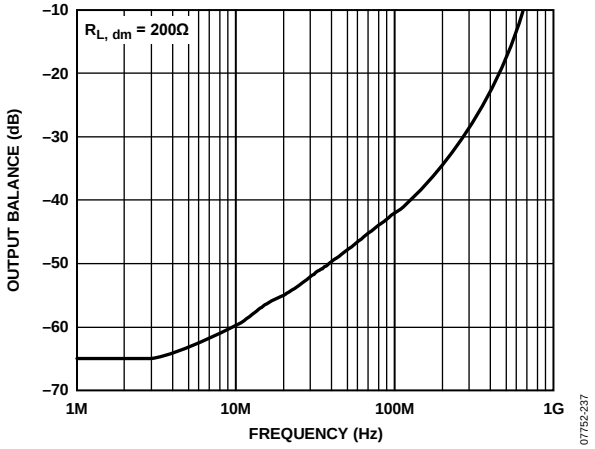



Figure 37. Output Balance vs. Frequency

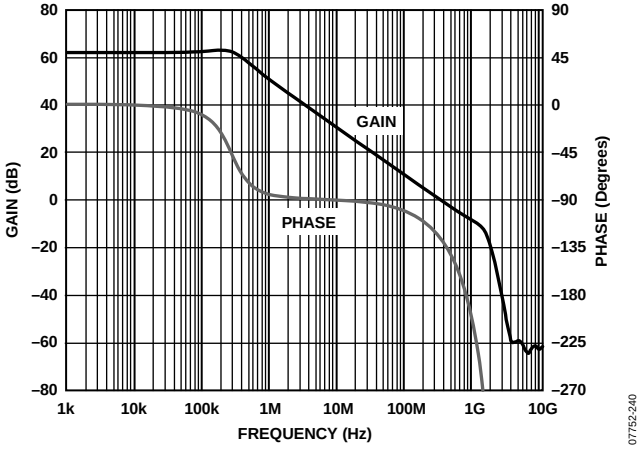



Figure 40. Open-Loop Gain and Phase vs. Frequency

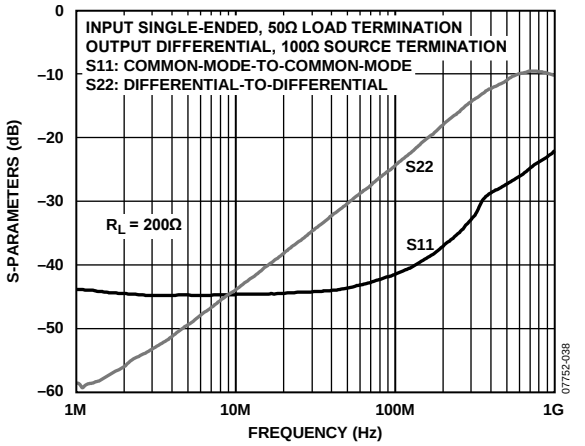



Figure 38. Return Loss ($S_{11}$, $S_{22}$) vs. Frequency

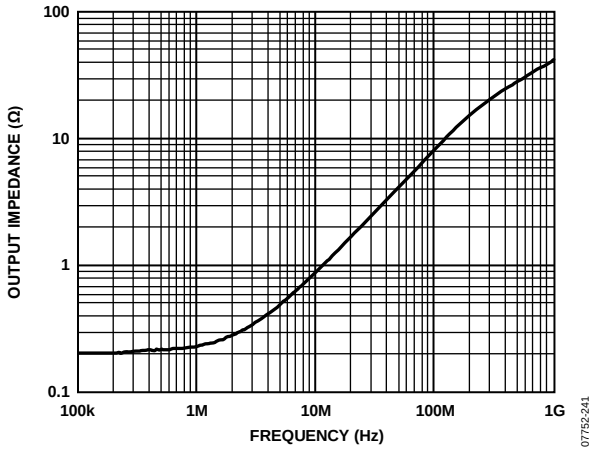



Figure 41. Closed-Loop Output Impedance Magnitude vs. Frequency, G = 1

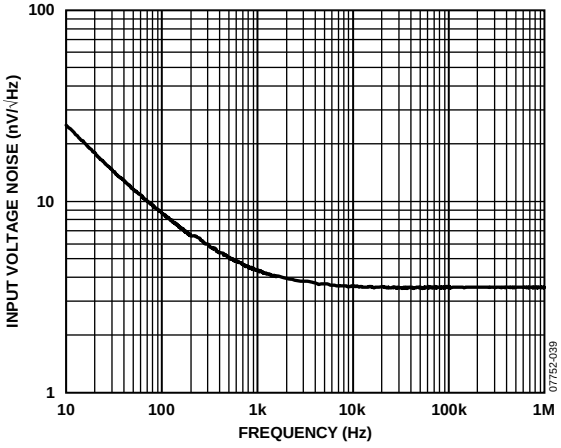



Figure 39. Voltage Noise Spectral Density, Referred to Input

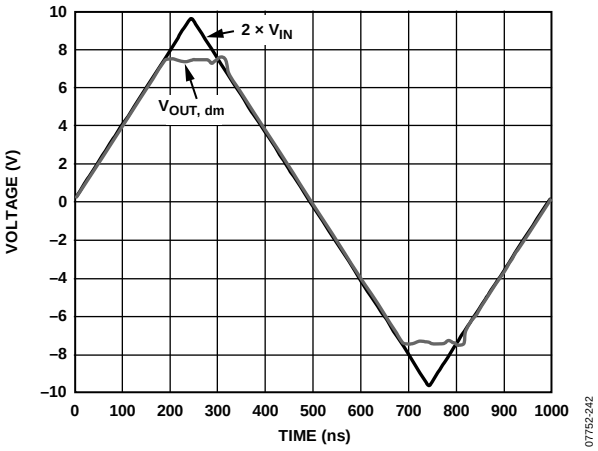



Figure 42.Overdrive Recovery, G = 2

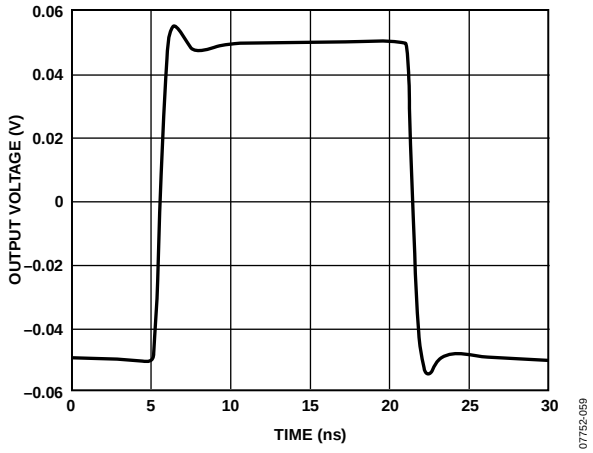



Figure 43. Small Signal Pulse Response

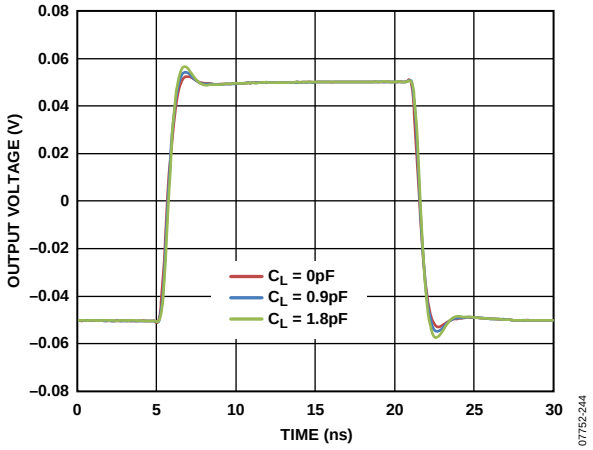



Figure 44. Small Signal Pulse Response for Various Capacitive Loads

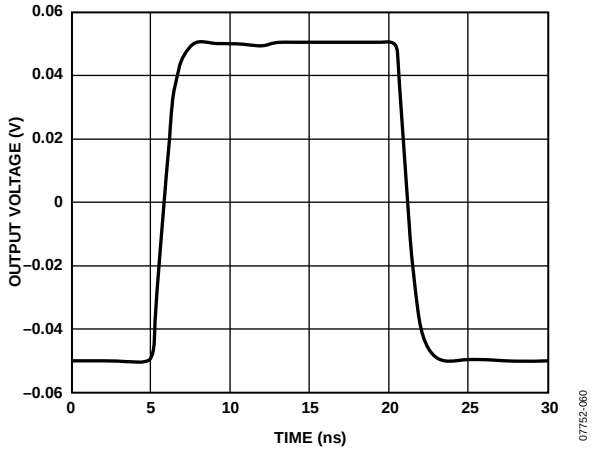



Figure 45. $V_{OCM}$ Small Signal Pulse Response

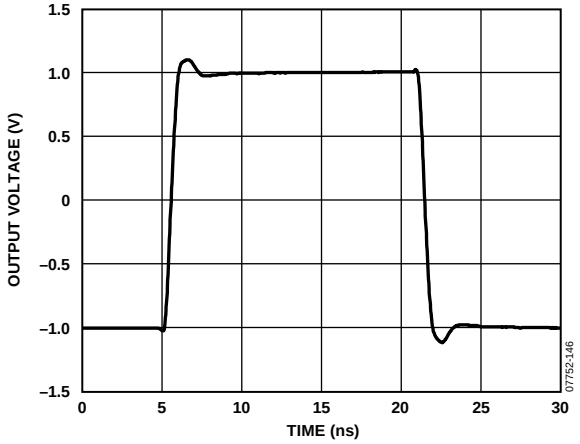



Figure 46. Large Signal Pulse Response

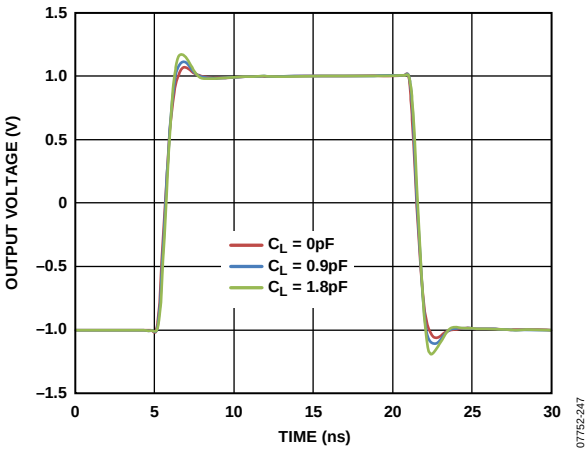



Figure 47. Large Signal Pulse Response for Various Capacitive Loads

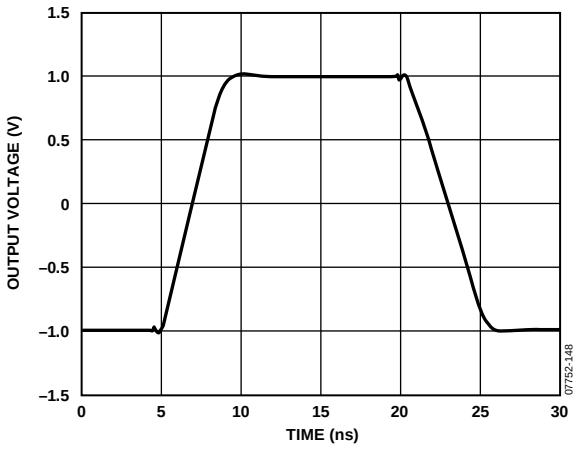



Figure 48. $V_{OCM}$ Large Signal Pulse Response

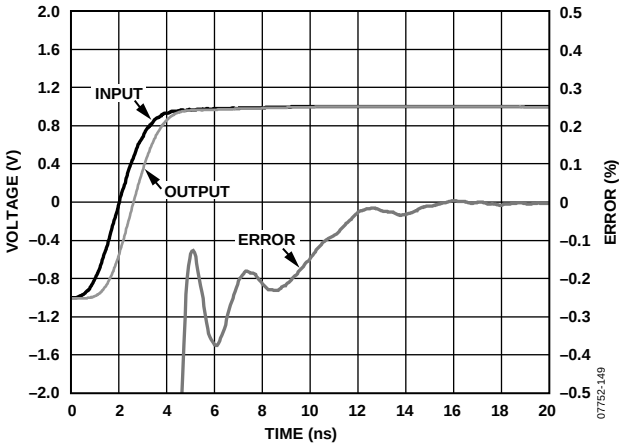



Figure 49. Settling Time

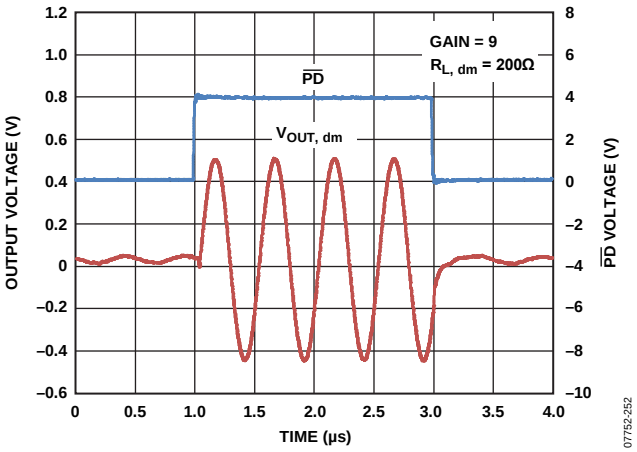



Figure 51. $\overline{PD}$ Response Time

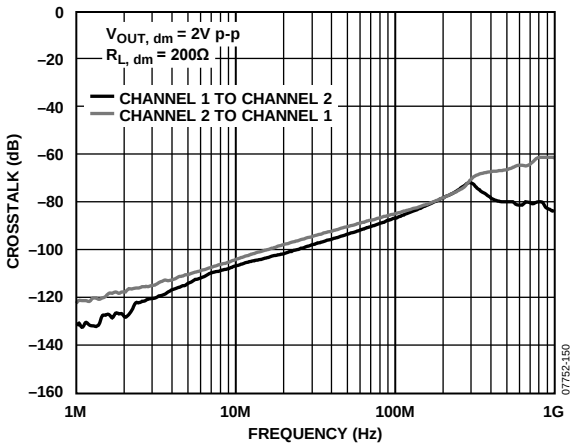



Figure 50. Crosstalk vs. Frequency, ADA4932-2

# TEST CIRCUITS

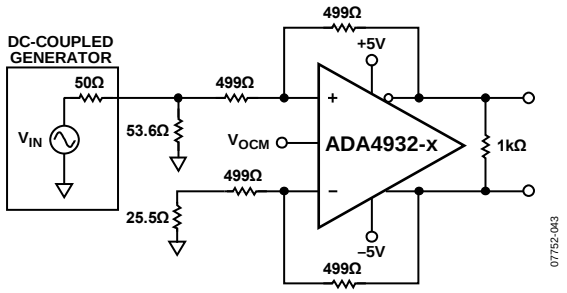



*Figure 52. Equivalent Basic Test Circuit, G = 1*

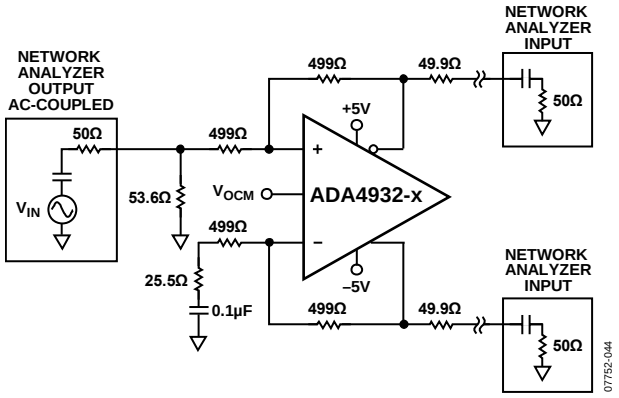



*Figure 53. Test Circuit for Output Balance, CMRR*

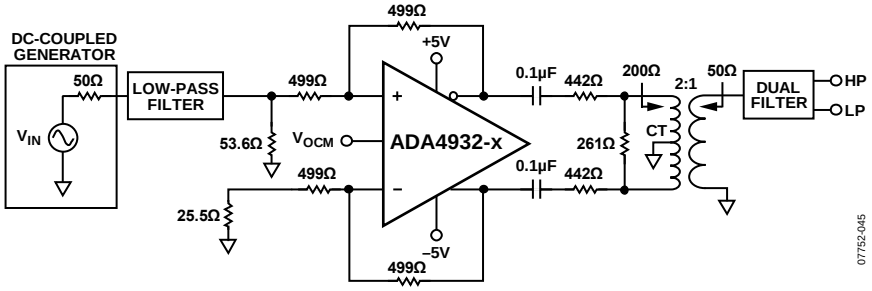



*Figure 54. Test Circuit for Distortion Measurements*

# TERMINOLOGY

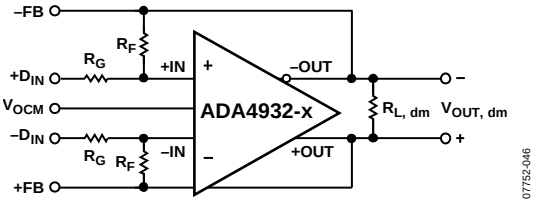



*Figure 55. Signal and Circuit Definitions*

**Differential Voltage**

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where $V_{+OUT}$ and $V_{-OUT}$ refer to the voltages at the +OUT and −OUT terminals with respect to a common ground reference. Similarly, the differential input voltage is defined as

$$V_{IN,\,dm} = (+D_{IN} - (-D_{IN}))$$

**Common-Mode Voltage**

Common-mode voltage refers to the average of two node voltages with respect to the local ground reference. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

**Balance**

Output balance is a measure of how close the output differential signals are to being equal in amplitude and opposite in phase. Output balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider midpoint with the magnitude of the differential signal (see Figure 53). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{\Delta V_{OUT,\,cm}}{\Delta V_{OUT,\,dm}} \right|$$

# THEORY OF OPERATION

The ADA4932 family differs from conventional op amps in that it has two outputs whose voltages move in opposite directions and an additional input, $V_{OCM}$. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4932 family behaves much like a standard voltage feedback op amp and facilitates single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Like an op amp, the ADA4932 family has high input impedance and low output impedance. Because it uses voltage feedback, the ADA4932 family manifests a nominally constant gain bandwidth product.

Two feedback loops are employed to control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value within the specified limits. The output common-mode voltage is forced, by the internal common-mode feedback loop, to be equal to the voltage applied to the $V_{OCM}$ input.

The internal common-mode feedback loop produces outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. This results in differential outputs that are very close to the ideal of being identical in amplitude and are exactly 180° apart in phase.

# APPLICATIONS INFORMATION

## ANALYZING AN APPLICATION CIRCUIT

The ADA4932 family uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 55). For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to $V_{OCM}$ can also be assumed to be zero. Starting from these principles, any application circuit can be analyzed.

## SETTING THE CLOSED-LOOP GAIN

Using the approach described in the Analyzing an Application Circuit section, the differential gain of the circuit in Figure 55 can be determined by

$$\left|\frac{V_{OUT,\,dm}}{V_{IN,\,dm}}\right| = \frac{R_F}{R_G}$$

This presumes that the input resistors ($R_G$) and feedback resistors ($R_F$) on each side are equal.

## ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4932 family can be estimated using the noise model in Figure 56. The input-referred noise voltage density, $v_{nIN}$, is modeled as a differential input, and the noise currents, $i_{nIN-}$ and $i_{nIN+}$, appear between each input and ground. The output voltage due to $v_{nIN}$ is obtained by multiplying $v_{nIN}$ by the noise gain, $G_N$ (defined in the $G_N$ equation that follows). The noise currents are uncorrelated with the same mean-square value, and each produces an output voltage that is equal to the noise current multiplied by the associated feedback resistance. The noise voltage density at the $V_{OCM}$ pin is $v_{nCM}$. When the feedback networks have the same feedback factor, as is true in most cases, the output noise due to $v_{nCM}$ is common mode. Each of the four resistors contributes $(4kTR_{xx})^{1/2}$. The noise from the feedback resistors appears directly at the output, and the noise from the gain resistors appears at the output multiplied by $R_F/R_G$. Table 11 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

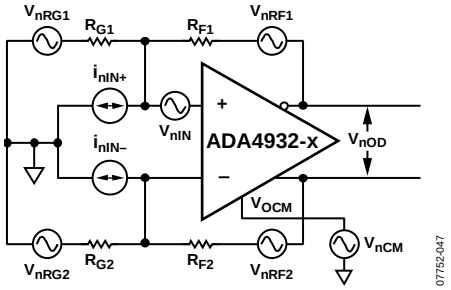



*Figure 56. Noise Model*

**Table 11. Output Noise Voltage Density Calculations for Matched Feedback Networks**

| Input Noise Contribution | Input Noise Term | Input Noise Voltage Density | Output Multiplication Factor | Differential Output Noise Voltage Density Term |
|---|---|---|---|---|
| Differential Input | $v_{nIN}$ | $v_{nIN}$ | $G_N$ | $v_{nO1} = G_N(v_{nIN})$ |
| Inverting Input | $i_{nIN-}$ | $i_{nIN-} \times (R_{F2})$ | 1 | $v_{nO2} = (i_{nIN-})(R_{F2})$ |
| Noninverting Input | $i_{nIN+}$ | $i_{nIN+} \times (R_{F1})$ | 1 | $v_{nO3} = (i_{nIN+})(R_{F1})$ |
| $V_{OCM}$ Input | $v_{nCM}$ | $v_{nCM}$ | 0 | $v_{nO4} = 0$ V |
| Gain Resistor, $R_{G1}$ | $v_{nRG1}$ | $(4kTR_{G1})^{1/2}$ | $R_{F1}/R_{G1}$ | $v_{nO5} = (R_{F1}/R_{G1})(4kTR_{G1})^{1/2}$ |
| Gain Resistor, $R_{G2}$ | $v_{nRG2}$ | $(4kTR_{G2})^{1/2}$ | $R_{F2}/R_{G2}$ | $v_{nO6} = (R_{F2}/R_{G2})(4kTR_{G2})^{1/2}$ |
| Feedback Resistor, $R_{F1}$ | $v_{nRF1}$ | $(4kTR_{F1})^{1/2}$ | 1 | $v_{nO7} = (4kTR_{F1})^{1/2}$ |
| Feedback Resistor, $R_{F2}$ | $v_{nRF2}$ | $(4kTR_{F2})^{1/2}$ | 1 | $v_{nO8} = (4kTR_{F2})^{1/2}$ |

**Table 12. Differential Input, DC-Coupled**

| Nominal Gain (dB) | $R_F$ (Ω) | $R_G$ (Ω) | $R_{IN,\,dm}$ (Ω) | Differential Output Noise Density (nV/√Hz) |
|---|---|---|---|---|
| 0 | 499 | 499 | 998 | 9.25 |
| 6 | 499 | 249 | 498 | 12.9 |
| 10 | 768 | 243 | 486 | 18.2 |

**Table 13. Single-Ended Ground-Referenced Input, DC-Coupled, $R_S$ = 50 Ω**

| Nominal Gain (dB) | $R_F$ (Ω) | $R_{G1}$ (Ω) | $R_T$ (Ω) (Std 1%) | $R_{IN,\,cm}$ (Ω) | $R_{G2}$ (Ω)[1] | Differential Output Noise Density (nV/√Hz) |
|---|---|---|---|---|---|---|
| 0 | 511 | 499 | 53.6 | 665 | 525 | 9.19 |
| 6 | 523 | 249 | 57.6 | 374 | 276 | 12.6 |
| 10 | 806 | 243 | 57.6 | 392 | 270 | 17.7 |

[1] $R_{G2} = R_{G1} + (R_S||R_T)$.

Similar to the case of a conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor,

where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When the feedback factors are matched, $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from $V_{OCM}$ goes to zero in this case. The total differential output noise density, $v_{nOD}$, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

Table 12 and Table 13 list several common gain settings, associated resistor values, input impedance, and output noise density for both balanced and unbalanced input configurations.

## IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks ($R_F/R_G$) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

The gain from the $V_{OCM}$ pin to $V_{OUT, dm}$ is equal to

$$2(\beta 1 - \beta 2)/(\beta 1 + \beta 2)$$

When $\beta 1 = \beta 2$, this term goes to zero and there is no differential output voltage due to the voltage on the $V_{OCM}$ input (including noise). The extreme case occurs when one loop is open and the other has 100% feedback; in this case, the gain from $V_{OCM}$ input to $V_{OUT, dm}$ is either +2 or −2, depending on which loop is closed. The feedback loops are nominally matched to within 1% in most applications, and the output noise and offsets due to the $V_{OCM}$ input are negligible. If the loops are intentionally mismatched by a large amount, it is necessary to include the gain term from $V_{OCM}$ to $V_{OUT, dm}$ and account for the extra noise. For example, if $\beta 1 = 0.5$ and $\beta 2 = 0.25$, the gain from $V_{OCM}$ to $V_{OUT, dm}$ is 0.67. If the $V_{OCM}$ pin is set to 2.5 V, a differential offset voltage is present at the output of (2.5 V)(0.67) = 1.67 V. The differential output noise contribution is (9.6 nV/√Hz)(0.67) = 6.4 nV/√Hz. Both of these results are undesirable in most applications; therefore, it is best to use nominally matched feedback factors.

Mismatched feedback networks also result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

As a practical summarization of the above issues, resistors of 1% tolerance produce a worst-case input CMRR of approximately 40 dB, a worst-case differential-mode output offset of 25 mV due to a 2.5 V $V_{OCM}$ input, negligible $V_{OCM}$ noise contribution, and no significant degradation in output balance error.

## CALCULATING THE INPUT IMPEDANCE FOR AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 57, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is $R_{IN, dm} = R_G + R_G = 2 \times R_G$.

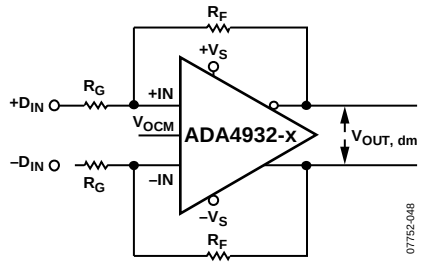



*Figure 57. ADA4932 Family Configured for Balanced (Differential) Inputs*

For an unbalanced, single-ended input signal (see Figure 58), the input impedance is

$$R_{IN, se} = \left( \frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

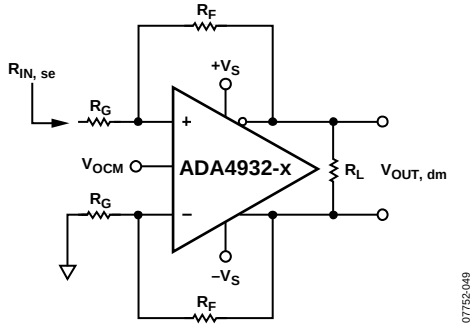



*Figure 58. ADA4932 Family with Unbalanced (Single-Ended) Input*

The input impedance of the circuit is effectively higher than it is for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor, $R_G$. The common-mode voltage at the amplifier input terminals can be easily determined by noting that the voltage at the inverting input is equal to the noninverting output voltage divided down by the voltage divider that is formed by $R_F$ and $R_G$ in the lower loop. This voltage is present at both input terminals due to negative voltage feedback and is in phase

with the input signal, thus reducing the effective voltage across $R_G$ in the upper loop and partially bootstrapping $R_G$.

### Terminating a Single-Ended Input

This section describes how to properly terminate a single-ended input to the ADA4932 family with a gain of 1, $R_F$ = 499 Ω, and $R_G$ = 499 Ω. An example using an input source with a terminated output voltage of 1 V p-p and source resistance of 50 Ω illustrates the four steps that must be followed. Note that because the terminated output voltage of the source is 1 V p-p, the open-circuit output voltage of the source is 2 V p-p. The source shown in Figure 59 indicates this open-circuit voltage.

1. The input impedance is calculated using the formula

$$R_{IN,se} = \left( \frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = \left( \frac{499}{1 - \frac{499}{2 \times (499 + 499)}} \right) = 665\,\Omega$$

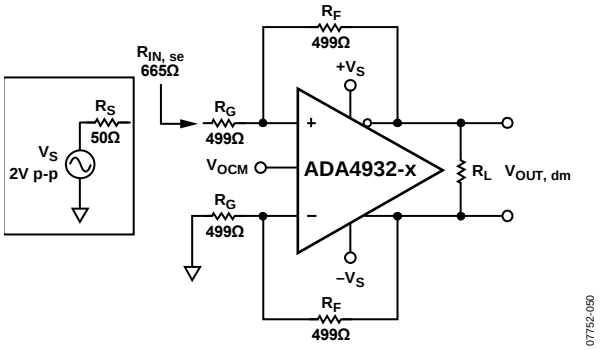



*Figure 59. Calculating Single-Ended Input Impedance, $R_{IN}$*

2. To match the 50 Ω source resistance, calculate the termination resistor, $R_T$, using $R_T||665\ \Omega = 50\ \Omega$. The closest standard 1% value for $R_T$ is 53.6 Ω.

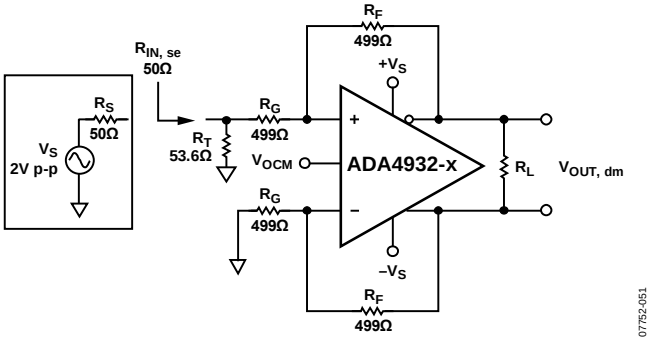



*Figure 60. Adding Termination Resistor, $R_T$*

3. Figure 60 shows that the effective $R_G$ in the upper feedback loop is now greater than the $R_G$ in the lower loop due to the addition of the termination resistors. To compensate for the imbalance of the gain resistors, add a correction resistor ($R_{TS}$) in series with $R_G$ in the lower loop. $R_{TS}$ is the Thevenin equivalent of the source resistance, $R_S$, and the termination resistance, $R_T$, and is equal to $R_S||R_T$.

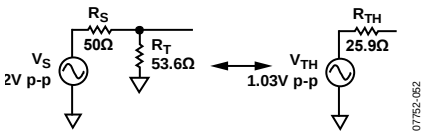



*Figure 61. Calculating the Thevenin Equivalent*

$R_{TS} = R_{TH} = R_S||R_T$ = 25.9 Ω. Note that $V_{TH}$ is greater than 1 V p-p, which was obtained with $R_T$ = 50 Ω. The modified circuit with the Thevenin equivalent (closest 1% value used for $R_{TH}$) of the terminated source and $R_{TS}$ in the lower feedback loop is shown in Figure 62.

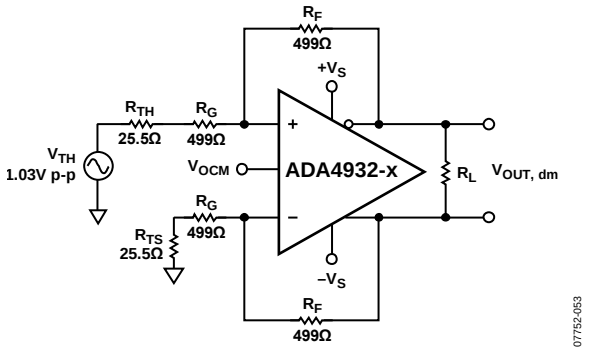



*Figure 62. Thevenin Equivalent and Matched Gain Resistors*

Figure 62 presents a tractable circuit with matched feedback loops that can be easily evaluated.

It is useful to point out two effects that occur with a terminated input. The first is that the value of $R_G$ is increased in both loops, lowering the overall closed-loop gain. The second is that $V_{TH}$ is a little larger than 1 V p-p, as it would be if $R_T$ = 50 Ω. These two effects have opposite impacts on the output voltage, and for large resistor values in the feedback loops (~1 kΩ), the effects essentially cancel each other out. For small $R_F$ and $R_G$, or high gains, however, the diminished closed-loop gain is not canceled completely by the increased $V_{TH}$. This can be seen by evaluating Figure 62.

The desired differential output in this example is 1 V p-p because the terminated input signal was 1 V p-p and the closed-loop gain = 1. The actual differential output voltage, however, is equal to (1.03 V p-p)(499/524.5) = 0.98 V p-p. To obtain the desired output voltage of 1 V p-p, a final gain adjustment can be made by increasing $R_F$ without modifying any of the input circuitry. This is discussed in Step 4.

4. The feedback resistor value is modified as a final gain adjustment to obtain the desired output voltage.

   To make the output voltage $V_{OUT}$ = 1 V p-p, calculate $R_F$ using the following formula:

$$R_F = \frac{(Desired\ V_{OUT,dm})(R_G + R_{TS})}{V_{TH}} = \frac{(1\ V\ p-p)(524.5\ \Omega)}{1.03\ V\ p-p} = 509\ \Omega$$

   The closest standard 1% value to 509 Ω is 511 Ω, which gives a differential output voltage of 1.00 V p-p.

   The final circuit is shown in Figure 63.

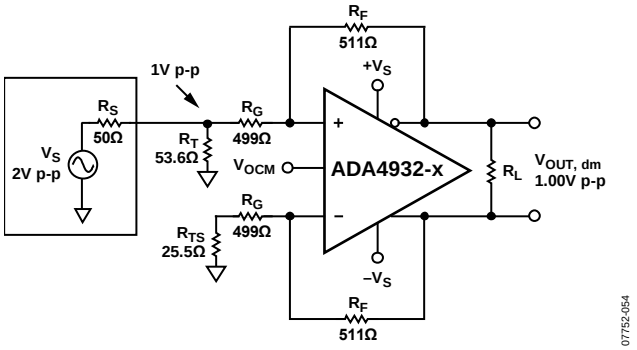



*Figure 63. Terminated Single-Ended-to-Differential System with G = 2*

## INPUT COMMON-MODE VOLTAGE RANGE

The ADA4932 family input common-mode range is shifted down by approximately one VBE, in contrast to other ADC drivers with centered input ranges such as the ADA4939 family. The downward-shifted input common-mode range is especially suited to dc-coupled, single-ended-to-differential, and single-supply applications.

For ±5 V operation, the input common-mode range at the summing nodes of the amplifier is specified as −4.8 V to +3.2 V, and is specified as +0.2 V to +3.2 V with a +5 V supply. To avoid nonlinearities, the voltage swing at the +IN and −IN terminals must be confined to these ranges.

## INPUT AND OUTPUT CAPACITIVE AC COUPLING

While the ADA4932 family is best suited to dc-coupled applications, it is nonetheless possible to use it in ac-coupled circuits. Input ac coupling capacitors can be inserted between the source and $R_G$. This ac coupling blocks the flow of the dc common-mode feedback current and causes the ADA4932 family dc input common-mode voltage to equal the dc output common-mode voltage. These ac coupling capacitors must be placed in both loops to keep the feedback factors matched. Output ac coupling capacitors can be placed in series between each output and its respective load.

## SETTING THE OUTPUT COMMON-MODE VOLTAGE

The $V_{OCM}$ pin of the ADA4932 family is internally biased with a voltage divider comprised of two 50 kΩ resistors across the supplies, with a tap at a voltage approximately equal to the midsupply point, $[(+V_S) + (-V_S)]/2$. Because of this internal divider, the $V_{OCM}$ pin sources and sinks current, depending on the externally applied voltage and its associated source resistance. Relying on the internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source or resistor divider be used with source resistance less than 100 Ω. If an external voltage divider consisting of equal resistor values is used to set $V_{OCM}$ to midsupply with greater accuracy than produced internally, higher values can be used because the external resistors are placed in parallel with the internal resistors. The output common-mode offset listed in the Specifications section assumes that the $V_{OCM}$ input is driven by a low impedance voltage source.

It is also possible to connect the $V_{OCM}$ input to a common-mode level (CML) output of an ADC; however, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the $V_{OCM}$ pin is approximately 25 kΩ. If multiple ADA4932 devices share one ADC reference output, a buffer may be necessary to drive the parallel inputs.

## HIGH PERFORMANCE PRECISION ADC DRIVER

Using a differential amplifier to drive an ADC successfully is linked to balancing each side of the differential amplifier correctly. Figure 65 shows the schematic for the ADA4932-1, AD7626, and associated circuitry. In the test circuit used, the signal source is followed by a 2.4 MHz band-pass filter. The band-pass filter eliminates harmonics of the 2.4 MHz signal and ensures that only the frequency of interest will be passed and processed by the ADA4932-1 and AD7626.

The ADA4932-1 is particularly useful when driving higher frequency inputs to the AD7626, a 10 MSPS ADC with a switched capacitor input. The resistor (R8, R9) and capacitor (C5, C6) circuit between the ADA4932-1 and AD7626 IN+ and IN− pins acts as a low-pass filter to noise. The filter limits the input bandwidth to the AD7626, but its main function is to optimize the interface between the driving amplifier and the AD7626. The series resistor isolates the driver amplifier from high frequency switching spikes from the ADC switched capacitor front end. The AD7626 data sheet shows values of 20 Ω and 56 pF. In Figure 65, these values were empirically optimized to 33 Ω and 56 pF. The resistor-capacitor combination can be optimized slightly for the circuit and input frequency being converted by simply varying the R-C combination—however, keep in mind that having the incorrect combination limits the THD and linearity performance of the AD7626. Also, increasing the bandwidth as seen by the ADC introduces more noise. Another aspect of optimization is the selection of the power supply voltages for the ADA4932-1. In the circuit, the output common-mode voltage (VCM pin) of the AD7626 is 2.048 V for the internal reference voltage of 4.096 V, and each input (IN+, IN−) swings between 0 V and 4.096 V, 180° out of phase. This provides an 8.2 V full-scale differential input to the ADC. The ADA4932-1 output stage requires about 1.4 V headroom with respect to each supply voltage for linear operation. Optimum distortion performance is obtained when the supply voltages are approximately symmetrical about the common-mode voltage. If a negative supply of −2.5 V is chosen, then a positive supply of at least +6.5 V is needed for symmetry about the common-mode voltage of 2.048 V.

Experiments performed indicate that a positive supply of 7.25 V gives the best overall distortion for a 2.4 MHz tone. Using a low jitter clock source and a single tone −1 dBFS amplitude, 2.402 MHz input to the AD7626 yielded the results shown in Figure 64 of 88.49 dB SNR and −86.17 dBc THD. At this input level, the ADC limits the SFDR to 83.8 dB. As can be seen from the plot, the harmonics of the fundamental alias back into the pass band. For example, when sampling at 10 MSPS the 3rd harmonic (7.206 MHz) will alias into the pass band at 10.000 MHz − 7.206 MHz = 2.794 MHz.

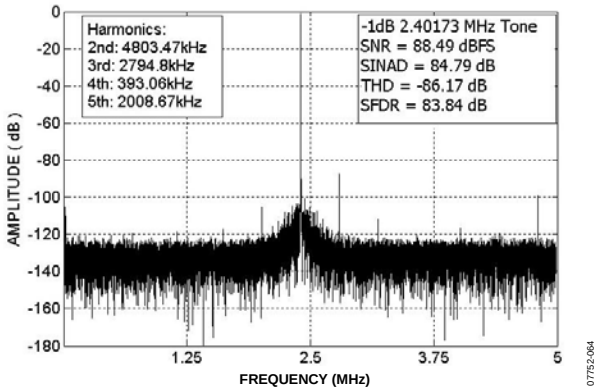



*Figure 64. AD7626 Output, 64,000 Point, FFT Plot −1 dBFS Amplitude 2.40173 MHz Input Ton, 10.000 MSPS Sampling Rate*

The nonharmonic noise admitted through the pass band of the band-pass filter used in the circuit is replaced by the average noise across the Nyquist bandwidth when calculating the SNR and THD. The performance of this or any high speed circuit is highly dependent on proper PCB layout. This includes, but is not limited to, power supply bypassing, controlled impedance lines (where required), component placement, signal routing, and power and ground planes. For a more detailed analysis of this circuit, refer to Circuit Note CN-0105.

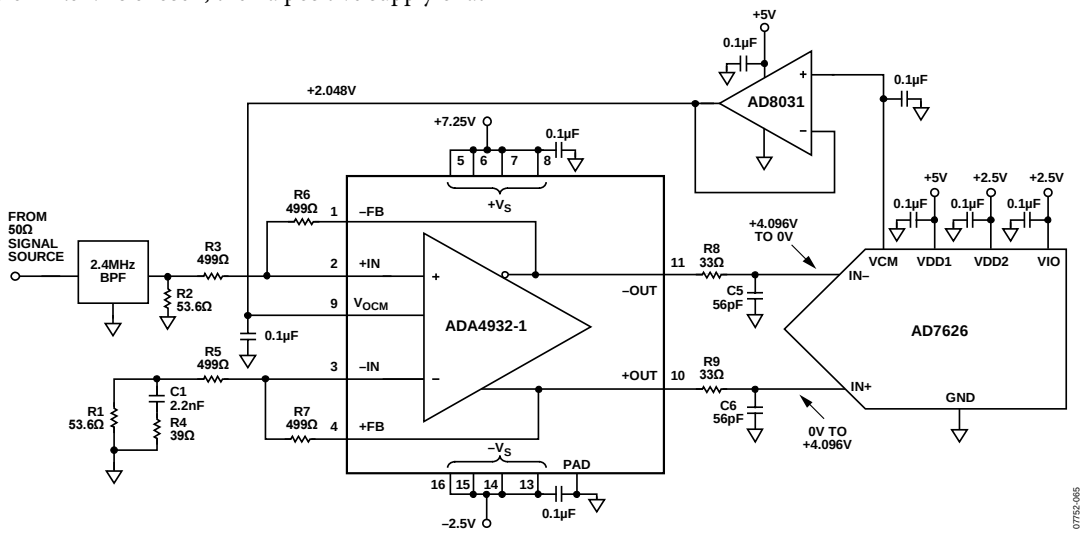



*Figure 65. ADA4932-1 Driving the AD7626 (All Connections and Decoupling Not Shown)*

# HIGH PERFORMANCE ADC DRIVING

The ADA4932 family is ideally suited for broadband dc-coupled applications. The circuit in Figure 66 shows a front-end connection for an ADA4932-1 driving an AD9245, a 14-bit, 20 MSPS/40 MSPS/65 MSPS/80 MSPS ADC, with dc coupling on the ADA4932-1 input and output. (The AD9245 achieves its optimum performance when driven differentially.) The ADA4932-1 eliminates the need for a transformer to drive the ADC and performs a single-ended-to-differential conversion and buffering of the driving signal.

The ADA4932-1 is configured with a single 3.3 V supply and a gain of 1 for a single-ended input to differential output. The 53.6 Ω termination resistor, in parallel with the single-ended input impedance of approximately 665 Ω, provides a 50 Ω termination for the source. The additional 25.5 Ω (524.5 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor driving the noninverting input.

In this example, the signal generator has a 1 V p-p symmetric, ground-referenced bipolar output when terminated in 50 Ω. The $V_{OCM}$ input is bypassed for noise reduction, and set externally with 1% resistors to maximize output dynamic range on the tight 3.3 V supply.

Because the inputs are dc-coupled, dc common-mode current flows in the feedback loops, and a nominal dc level of 0.84 V is present at the amplifier input terminals. A fraction of the output signal is also present at the input terminals as a common-mode signal; its level is equal to the ac output swing at the noninverting output, divided down by the feedback factor of the lower loop. In this example, this ripple is 0.5 V p-p × [524.5/(524.5 + 511)] = 0.25 V p-p. This ac signal is riding on the 0.84 V dc level, producing a voltage swing between 0.72 V and 0.97 V at the input terminals. This is well within the specified limits of 0.2 V to 1.5 V.

With an output common-mode voltage of 1.65 V, each ADA4932-1 output swings between 1.4 V and 1.9 V, opposite in phase, providing a gain of 1 and a 1 V p-p differential signal to the ADC input. The differential RC section between the ADA4932-1 output and the ADC provides single-pole low-pass filtering and extra buffering for the current spikes that are output from the ADC input when its SHA capacitors are discharged.

The AD9245 is configured for a 1 V p-p full-scale input by connecting its SENSE pin to VREF, as shown in Figure 66.

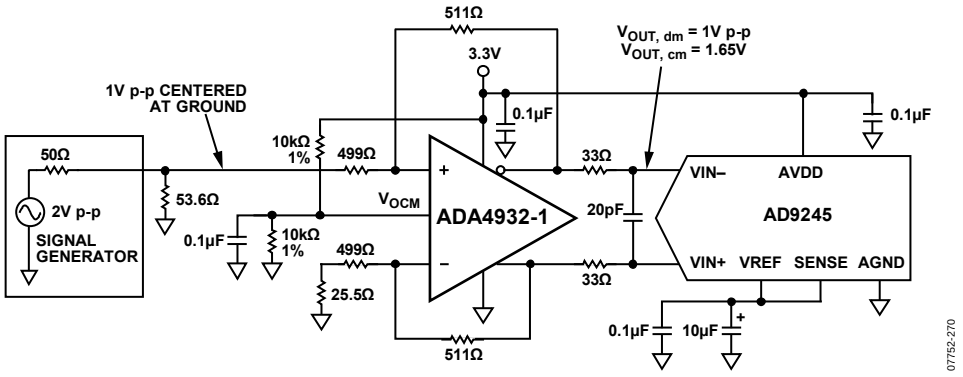



*Figure 66. ADA4932-1 Driving an AD9245 ADC with DC-Coupled Input and Output*

# LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the ADA4932 family is sensitive to the PCB environment in which it operates. Realizing its superior performance requires attention to the details of high speed PCB design.

The first requirement is a solid ground plane that covers as much of the board area around the ADA4932 family as possible. However, the area near the feedback resistors ($R_F$), gain resistors ($R_G$), and the input summing nodes (Pin 2 and Pin 3) should be cleared of all ground and power planes (see Figure 67). Clearing the ground and power planes minimizes any stray capacitance at these nodes and thus minimizes peaking of the response of the amplifier at high frequencies.

The thermal resistance, $\theta_{JA}$, is specified for the device, including the exposed pad, soldered to a high thermal conductivity 4-layer circuit board, as described in EIA/JESD51-7.

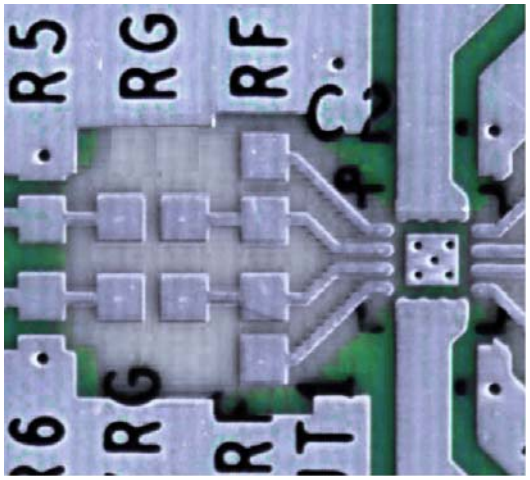



*Figure 67. Ground and Power Plane Voiding in Vicinity of $R_F$ and $R_G$*

Bypass the power supply pins as close to the device as possible and directly to a nearby ground plane. High frequency ceramic chip capacitors should be used. It is recommended that two parallel bypass capacitors (1000 pF and 0.1 µF) be used for each supply. Place the 1000 pF capacitor closer to the device. Further away, provide low frequency bulk bypassing using 10 µF tantalum capacitors from each supply to ground.

Signal routing should be short and direct to avoid parasitic effects. Wherever complementary signals exist, provide a symmetrical layout to maximize balanced performance. When routing differential signals over a long distance, keep PCB traces close together, and twist any differential wiring to minimize loop area. Doing this reduces radiated energy and makes the circuit less susceptible to interference.

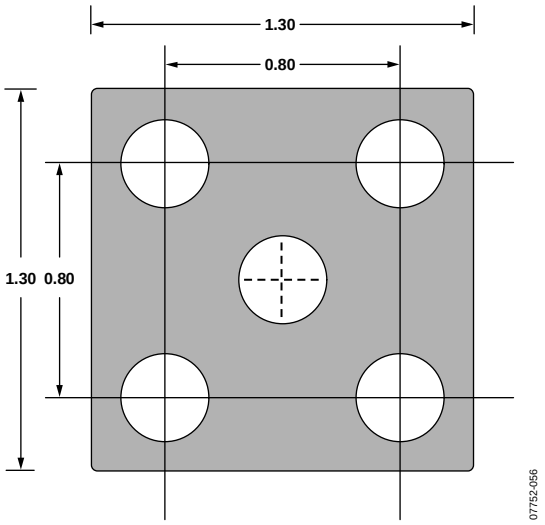



*Figure 68. Recommended PCB Thermal Attach Pad Dimensions (Millimeters)*

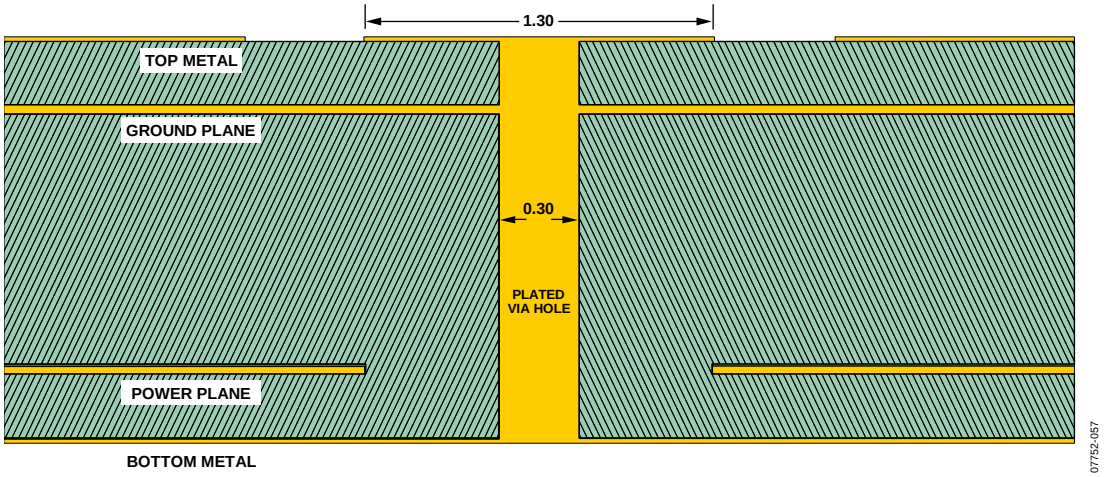



*Figure 69. Cross-Section of 4-Layer PCB Showing Thermal Via Connection to Buried Ground Plane (Dimensions in Millimeters)*

# OUTLINE DIMENSIONS

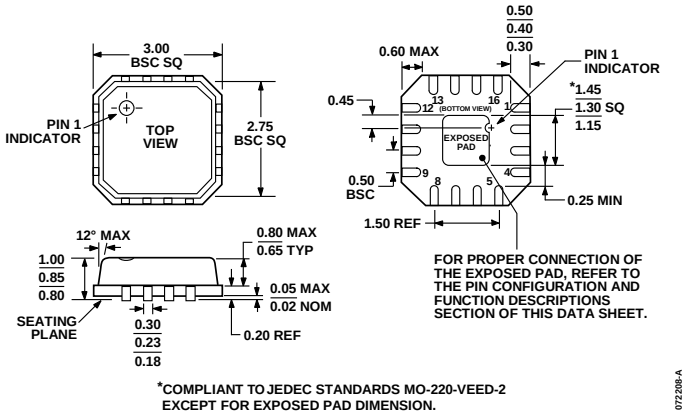



*Figure 70. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*3 mm × 3 mm Body, Very Thin Quad (CP-16-2)*
*Dimensions shown in millimeters*

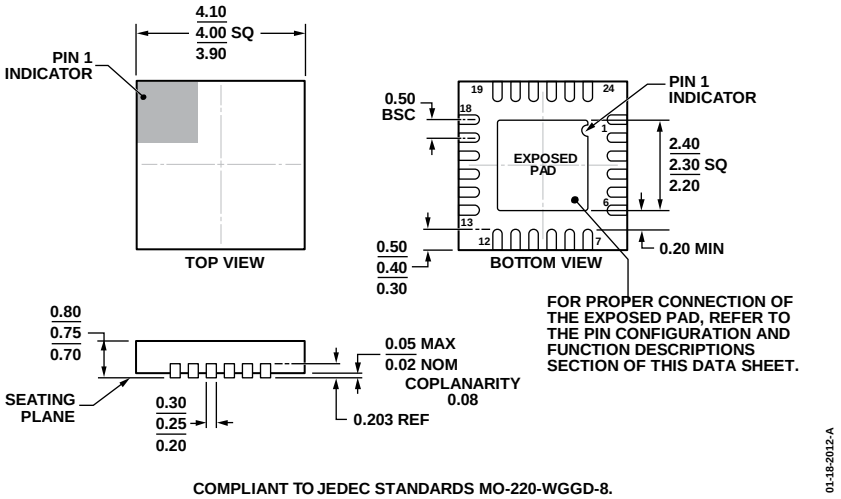



*Figure 71. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]*
*4 mm × 4 mm Body, Very Very Thin Quad (CP-24-14)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Ordering Quantity | Branding |
|---|---|---|---|---|---|
| ADA4932-1YCPZ-R2 | −40°C to +105°C | 16-Lead LFCSP_VQ | CP-16-2 | 250 | H1K |
| ADA4932-1YCPZ-RL | −40°C to +105°C | 16-Lead LFCSP_VQ | CP-16-2 | 5,000 | H1K |
| ADA4932-1YCPZ-R7 | −40°C to +105°C | 16-Lead LFCSP_VQ | CP-16-2 | 1,500 | H1K |
| ADA4932-1YCP-EBZ | | Evaluation Board | | | |
| ADA4932-2YCPZ-R2 | −40°C to +105°C | 24-Lead LFCSP_WQ | CP-24-14 | 250 | |
| ADA4932-2YCPZ-RL | −40°C to +105°C | 24-Lead LFCSP_WQ | CP-24-14 | 5,000 | |
| ADA4932-2YCPZ-R7 | −40°C to +105°C | 24-Lead LFCSP_WQ | CP-24-14 | 1,500 | |
| ADA4932-2YCP-EBZ | | Evaluation Board | | | |

[1] Z = RoHS Compliant Part.

## NOTES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