PmodMIC™ Reference Component

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Overview

The PmodMIC Reference Component synchronizes data communications between a Digilent FPGA development board and the PmodMIC board. It uses the PmodMIC to take in a 16-bit vector serially using the correct timing sequence, and outputs a 12-bit vector with the converted digital value.

The component inputs a digital signal serially from the ADCS7476 analog-to-digital converter on the PmodMIC and outputs the data to any external VHDL component. It also supplies the appropriate timing sequence to clock the AD converter.

Functional Description

Component Architecture

The VHDL component is an entity named PmodMicRefComp which has five inputs and five outputs. The input ports are a 50MHz clock, an asynchronous reset button, and the data from the ADCS7476 that is serially shifted-in on each clock cycle (SDATA). The outputs are the SCLK signal, which clocks the PmodMIC at 12.5MHz; a chip select signal (nCS), which enables the ADCS7476 chip on the PmodMIC; and as the 12-bit output vector (labeled DATA) from the ADCS7476 chip, which can be used by any external component. The START signal is used to tell the component when to start a conversion. After a conversion is done, the component activates the DONE signal. A block diagram of the component is shown in Figure 1.

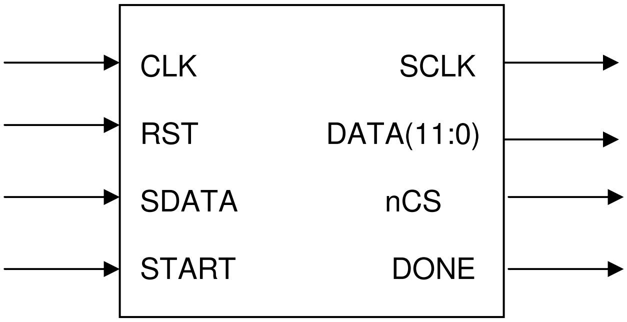

Figure 1 ***PmodMIC Reference Component***

Timing

The timing diagram in Figure 2 is used to determine the correct timing sequence for the finite state machine that clocks the PmodMIC. It is the timing sequence that is used to generate 16 bits of data using the ADCS7476 chip inside the PmodMIC. The signal nCS must be at a low or zero state while the data is generated on the falling edge of the clock signal. Immediately following the data transfer, the signal nCS must be driven high to signal when a new set of data can be generated.

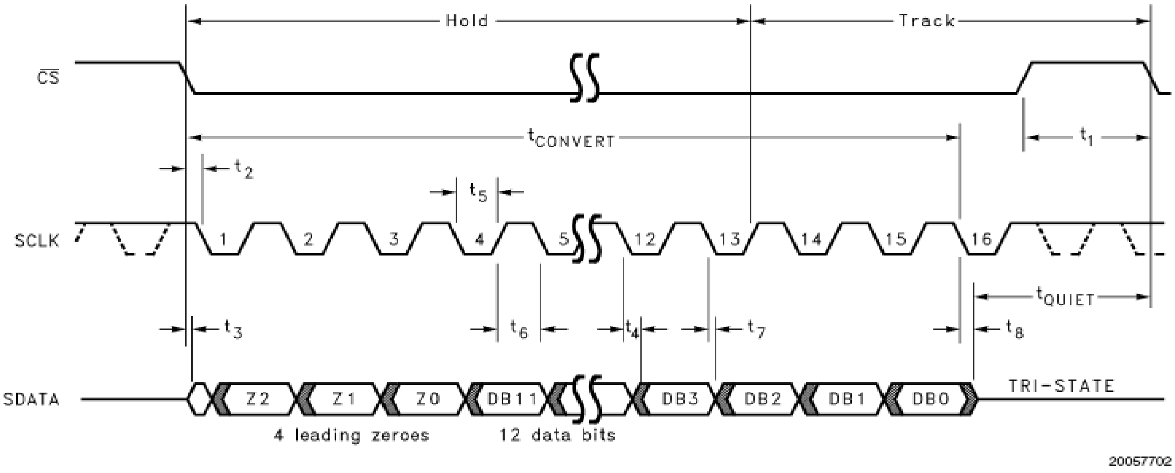

Figure 2 ***Timing Diagram of the ADCS7476 Chip on the PmodMIC***

The logic that created the timing sequence to take in the data input SDATA serially and latch in the 16-bit vector, as well as clock the nCS and SCLK outputs, was designed by creating the finite state machine shown in Figure 3.

State Machine

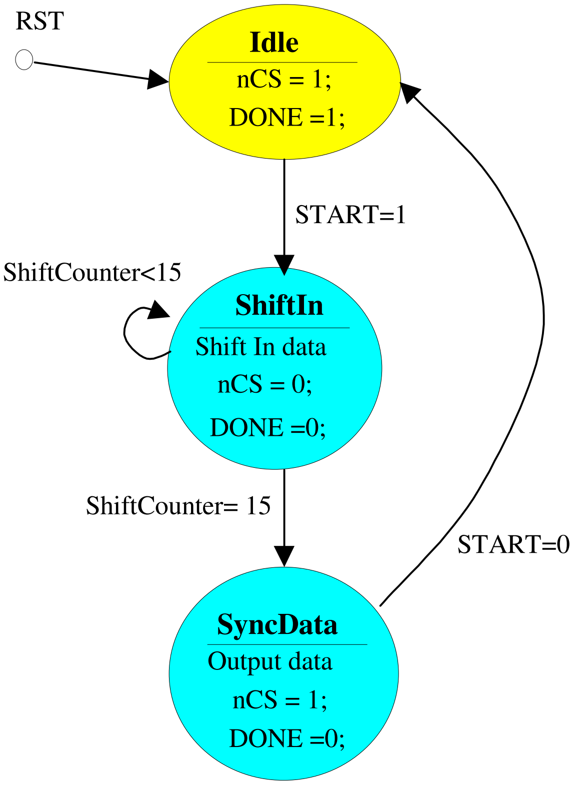

Figure 3 ***FSM of the PmodMIC Reference Component***

There are three states: Idle, ShiftIn, and SyncData. During the Idle state, the DONE output signal needs to be high in order to allow a conversion. When the START signal is going high, the state machine goes into the ShiftIn state.

In the ShiftIn state, the DONE signal goes low and the data from the PmodMIC is serially shifted-in from MSB to LSB for 16 clock cycles to ensure that all 16 bits of data have been received from each chip. After shifting is done, the state machine goes into the SyncData state.

In the SyncData state, the effective data received from the PmodMIC is placed on the 12-bit output port DATA.

If the START input signal is low the machine goes back to the Idle state, ready to accept another conversion.

No mater what the current state is, the RST input signal resets the state machine and puts it into the Idle state.