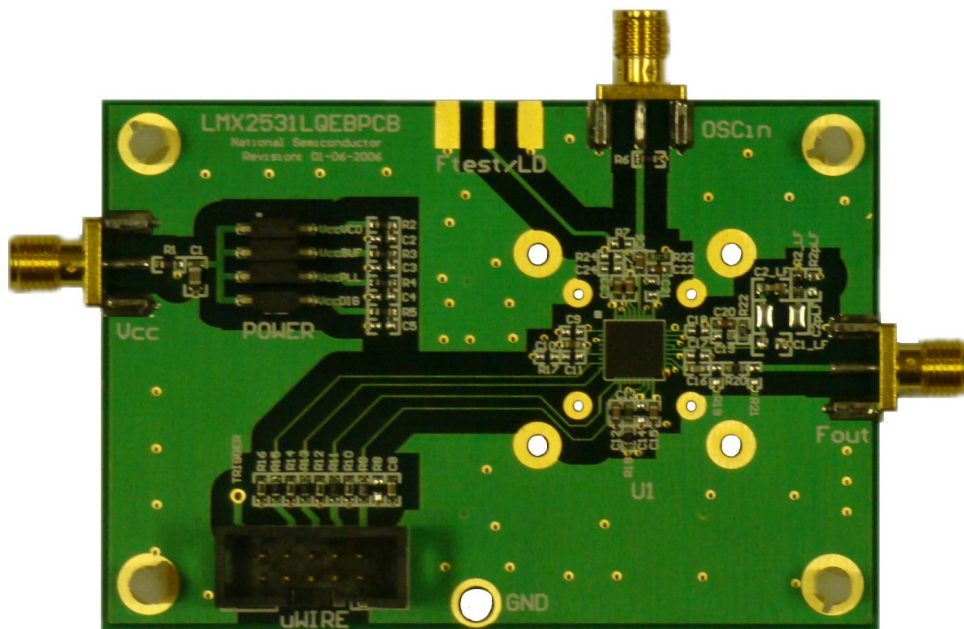




LMX2531LQ1312E

Evaluation Board Operating Instructions



National Semiconductor Corporation
Timing Devices Business Group

10333 North Meridian
Suite 400
Indianapolis, IN 46290

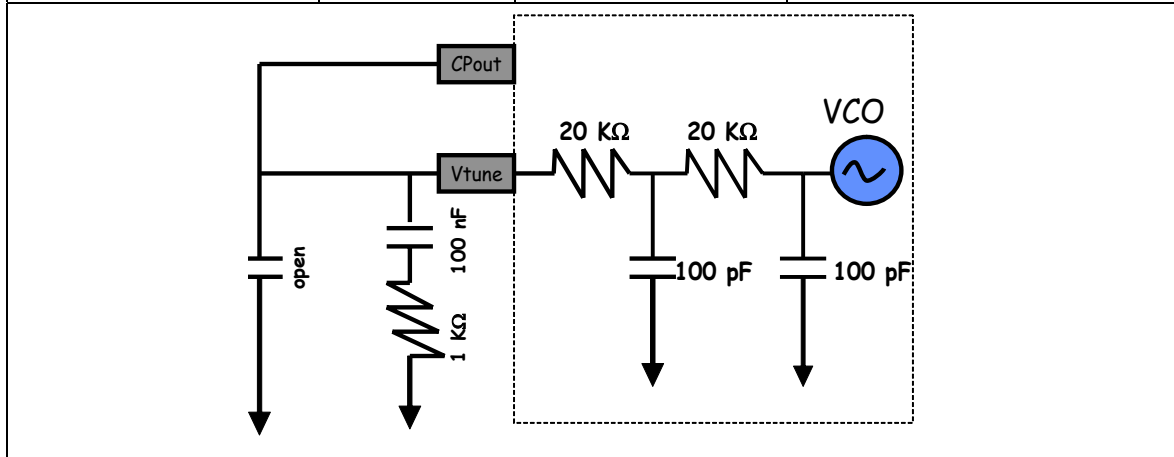
LMX2531LQ1312EFPEB Rev 4.02.2008

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Loop Filter

Loop Bandwidth	7.7 kHz	Kϕ	1440 uA (16X)
Phase Margin	61.5 deg	F_{comp}	10 MHz
Crystal Frequency	10 MHz	Output Frequency	1268 – 1360 MHz (DIV2=0) 634 - 680 MHz (DIV2=1)
Supply Voltage	3.0 Volts	VCO Gain	3 - 6 MHz/Volt



Quick Setup

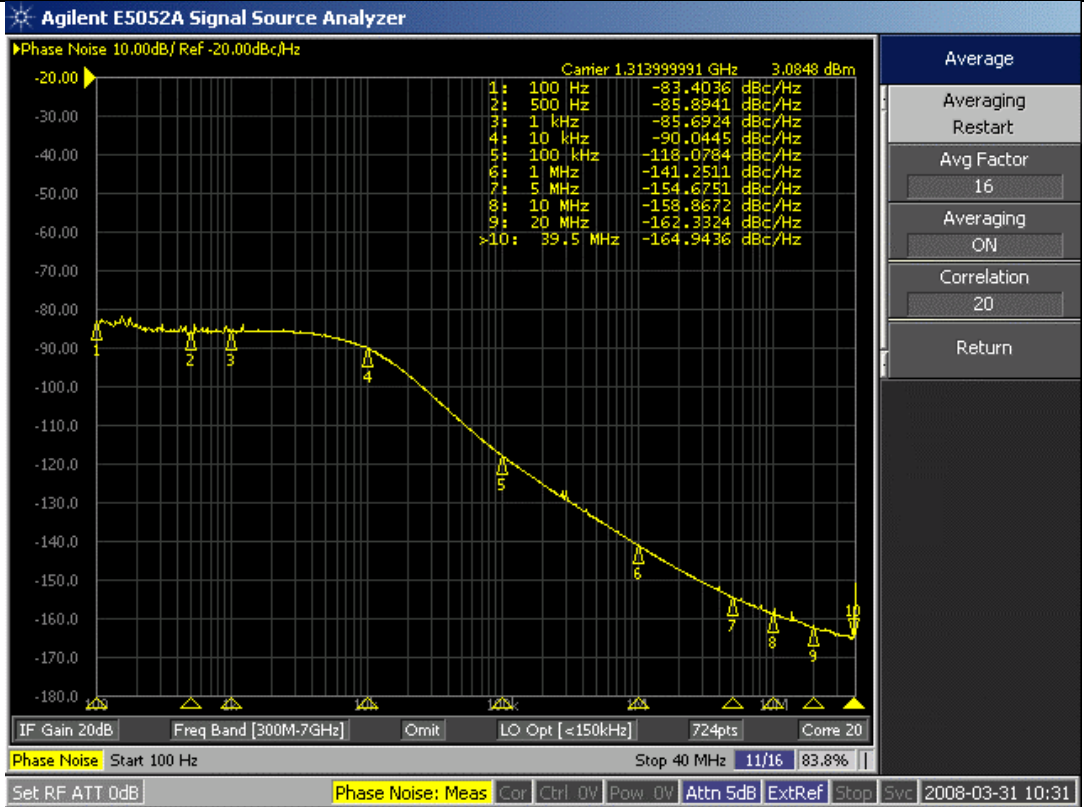
- Install the CodeLoader software which is available at www.national.com/timing.
- Attach the parallel or USB to parallel, port cable to the computer and the evaluation board.
- Connect 3.0 volts to the **Vcc** connector
- Connect the **Fout** connector to a spectrum analyzer or phase noise analyzer
- Connect a clean 10 MHz source to the **OSCin** pin. Typically, the 10 MHz output from the back of the RF test equipment is a good source. Signal generators tend to be very noisy and should be used with caution. If a signal generator is used, the signal generator phase noise contribution can be reduced by setting the signal to 80 MHz and dividing this down to a phase detector frequency of 10 MHz.
- Set up the CodeLoader software
 - Select the proper part from the menu as Select Part>PLL+VCO>LMX2531LQ1312E
 - Select the proper mode from the Mode menu
 - Load the part by pressing (Ctrl+L) or selecting Keyboard Controls->Load Device from the menu
- It is recommended to ensure proper communication with the device
 - Click the REG_RST bit on the bits/pins page and observe the current go to 0 mA
 - Unclick the REG_RST bit AND press (Ctrl+L). The current should be approximately 35 mA
 - If device does not respond to this, consult the troubleshooting section
- When using the lower frequency band with divide by 2 enabled (DIV2=1), be aware that the frequency programmed to the VCO is actually twice the output frequency of the device because the VCO frequency is being divided by 2.

Troubleshooting

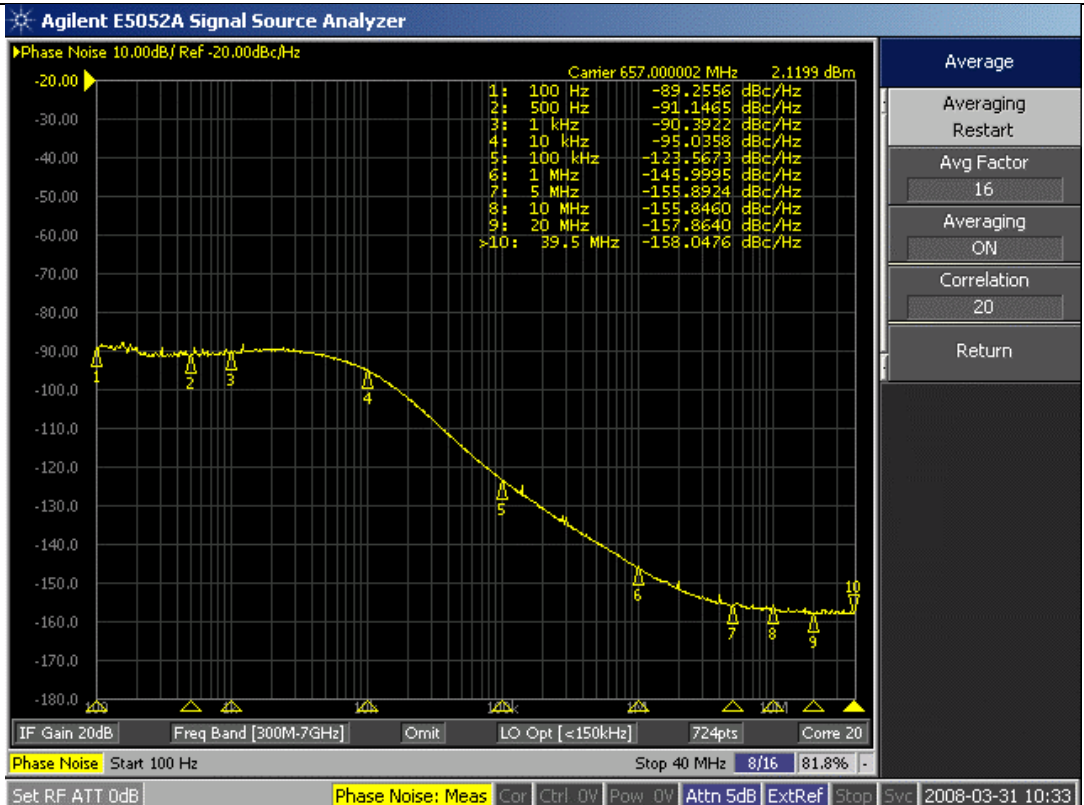
Problem	Corrective Actions
Software does not communicate with the evaluation boards	<p>All Modes</p> <ul style="list-style-type: none"> • Ensure a valid signal is presented to the OSCin connector. If a signal generator is used, ensure the RF is ON. • Consult the CodeLoader instructions for more detailed information on communication issues. (See www.national.com/timing) <p>LPT Mode (Uses Parallel Port Cable)</p> <ul style="list-style-type: none"> • Ensure that CodeLoader is selected to LPT mode on the Port Setup tab. • Ensure the proper port number is selected (LPT1, LPT2, LPT3). CodeLoader does NOT automatically detect this. • Ensure the LPT cable is securely connected to the computer and board. • Try to exit and restart CodeLoader. • Ensure the parallel port is in the correct mode <ul style="list-style-type: none"> ○ Windows often requires administrative access to write to the parallel port. ○ Ensure that the parallel port is set to “Enabled” in windows device manager. ○ A reboot upon installation of CodeLoader is sometimes necessary to get the parallel port to work. ○ Standard mode is the most reliable. This can be set in the BIOS mode of the computer as “Normal”, “Output Only”, or “AT”. <p>USB Mode (USB to Parallel Port Converter)</p> <ul style="list-style-type: none"> • On the menu, select USB>Version to verify communication with the board. • Ensure the Green LEDs are lit on the USB board. • Ensure there are no conflicts with other USB devices and reinstall the board.
Part responds to programming, but does not lock to the correct frequency	<ul style="list-style-type: none"> • Ensure there is a valid signal presented to the OSCin connector. If a signal generator is used, the RF should be set to ON. • If using the lower frequency band (DIV2=1), understand that the VCO frequency in CodeLoader should be twice the frequency at the Fout pin. • Ensure that the VCO FREQUENCY CAL bits on the Bits/Pins tab are correct. • Ensure the loop filter is optimized if the charge pump current, phase detector frequency, or loop filter values have been changed from their original settings. Ensure the integrated loop filter components on CodeLoader are set to their proper settings.
Close-in phase noise is worse than evaluation board instructions show	<ul style="list-style-type: none"> • Ensure the signal presented to OSCin connector is clean. Try another source, or if it is a signal generator, try using a higher frequency and dividing it down to the phase detector frequency. • Ensure the OSCin signal and cable provides sufficient power level. • If the phase detector frequency or charge pump current is lowered from their original settings, the in-band phase noise can be degraded, even if the loop filter is re-designed for the same loop bandwidth. If the loop bandwidth is decreased, in-band phase noise can be degraded.
Far-out Phase noise is worse than evaluation board instructions show	<ul style="list-style-type: none"> • Ensure the measurement equipment noise floor is not limiting the measurement. For spectrum analyzers, the noise floor at a particular setting can be measured by removing the RF input signal. • If the settings are changed from what the board was designed for, ensure the delta-sigma modulator is not increasing the far-out noise. To know this, tune to an integer channel and set the ORDER bit to “Reset Modulator”. The far-out phase noise should not decrease. If it does, try a loop filter with more attenuation or select a lower order delta-sigma modulator.

Phase Noise

Output Frequency = 1314 MHz
Internal Divide by 2 Disabled (DIV2=0)

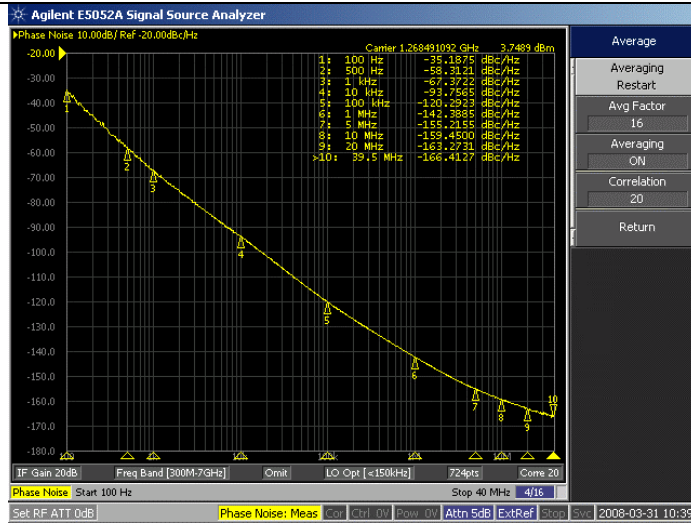


Output Frequency = 657 MHz
Internal Divide by 2 Enabled (DIV2=1)

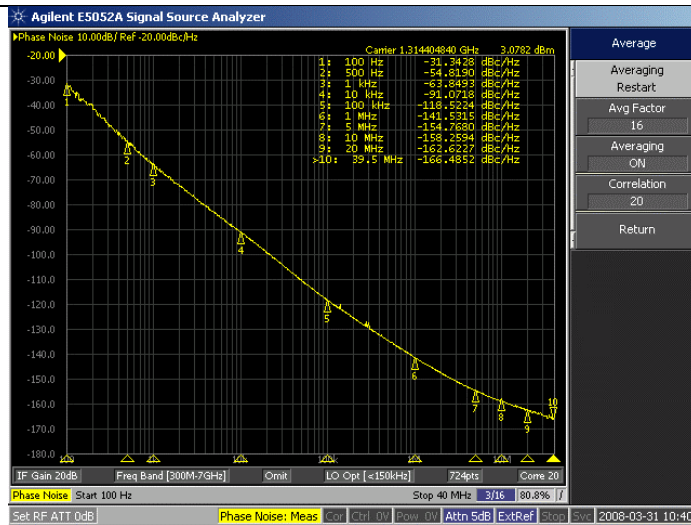


Free-Running VCO Noise (Internal Divide by 2 Disabled)

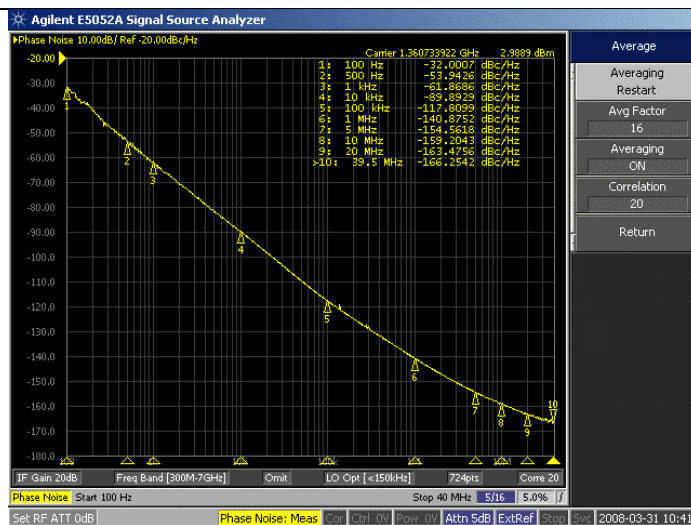
Fout = 1268 MHz



Fout = 1314 MHz



Fout = 1360 MHz

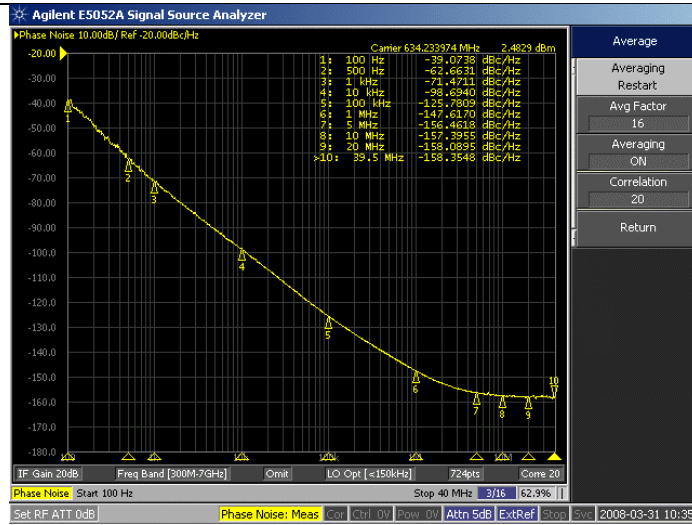


The plots to the left show the true phase noise capability of the VCO. In order to take these plots, the E5052 phase noise analyzer was used. The method was to lock the PLL to the proper frequency, then disable the EN_PLL, EN_PLLLDO1, and EN_PLLLDO2 bits. The equipment needs to be able to track the VCO phase noise to measure in this way, and one can not let the VCO drift too far off in frequency. If this kind of equipment is not available, the VCO phase noise can also be measured by making a very narrow loop bandwidth filter.

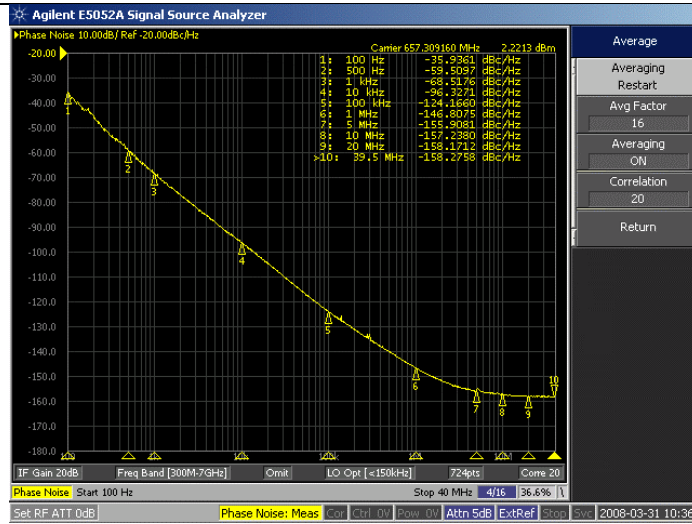
On the 1312E option especially of the LMX2531 family, pay special attention to bypassing at the VregPLL1, VregPLL2, and VregVCO pins. This option is especially sensitive to this. Phase noise degradation in the 10 – 200 kHz range can happen. Even on these plots, there is some room for optimization.

Free-Running VCO Noise (Internal Divide by 2 Enabled)

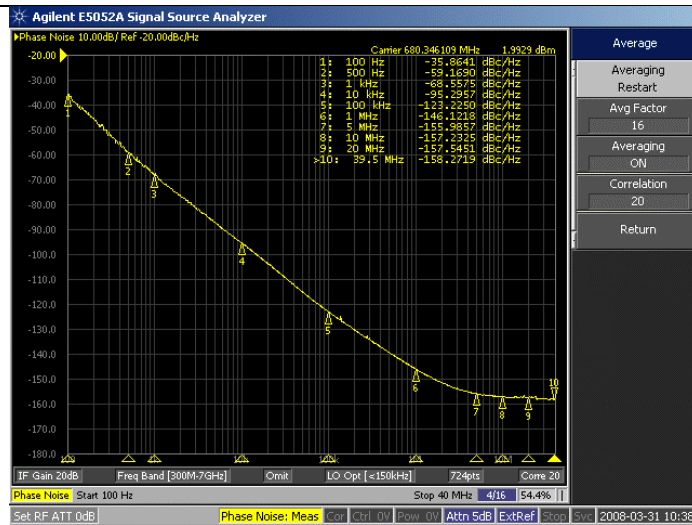
Fout = 634 MHz (1268 MHz/2)



Fout = 657 MHz (1314 MHz/2)



Fout = 680 MHz (1360 MHz/2)

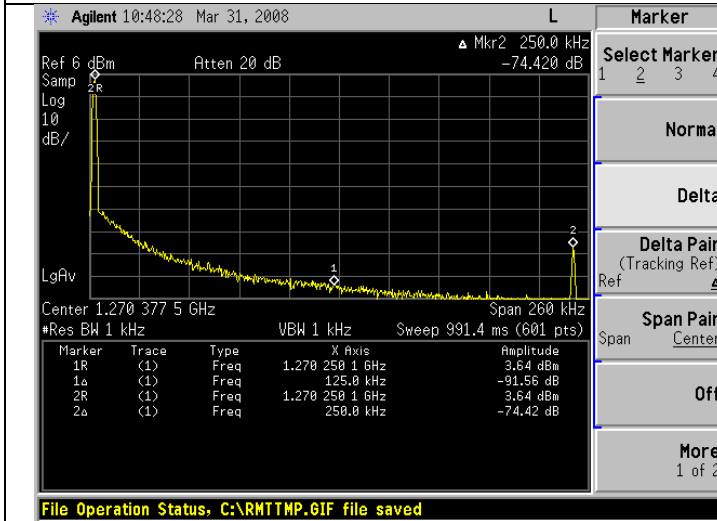


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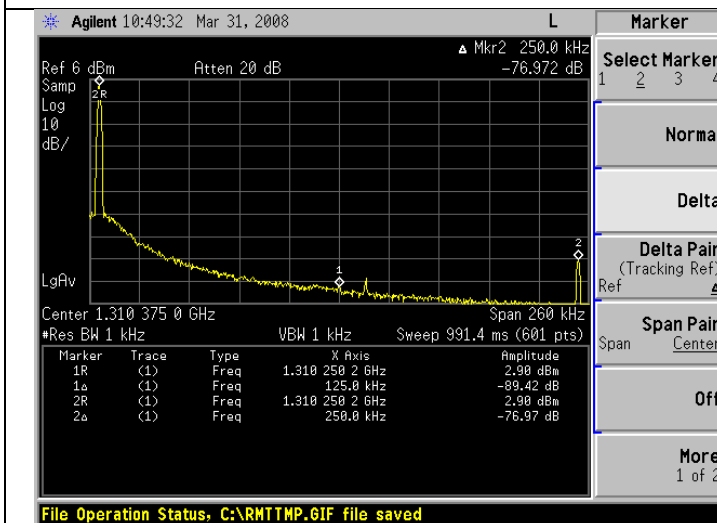
equipment needs to be able to track the VCO phase noise to measure in this way, and one can not let the VCO drift too far off in frequency. If this kind of equipment is not available, the VCO phase noise can also be measured by making a very narrow loop bandwidth filter.

When divide by 2 is enabled, the phase noise at lower offsets is about 6 dB better. At high offsets, the overall phase noise improvement may be lower because the divider is noise floor is adding to the phase noise.

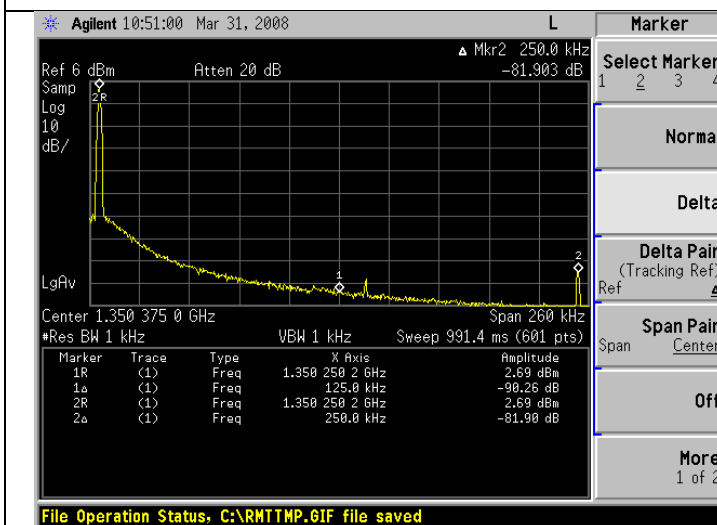
Fractional Spurs (Internal Divide by 2 Disabled)



Fractional Spur at 250 kHz offset at a worst case frequency of 1270.25 MHz is -74.4 dBc. Worst case channels occur at exactly one channel spacing above or below a multiple of the crystal frequency.

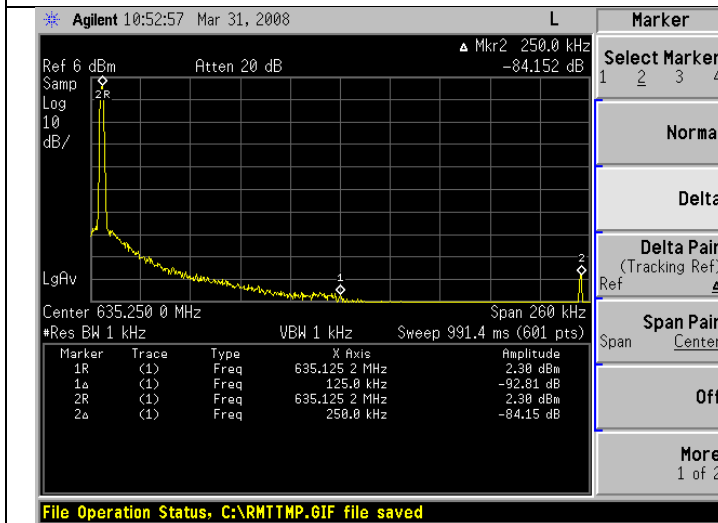


Fractional Spur at 250 kHz offset at a worst case frequency of 1310.25 MHz is -77.0 dBc.

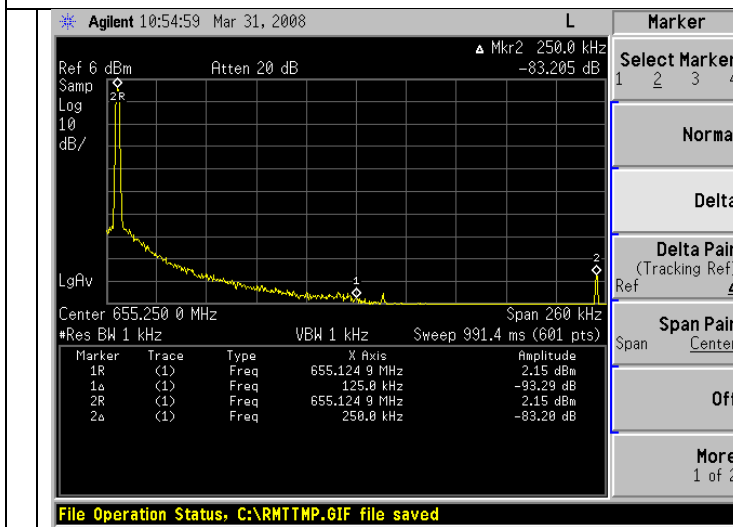


Fractional Spur at 250 kHz offset at a worst case frequency of 1350.25 MHz is -81.9 dBc.

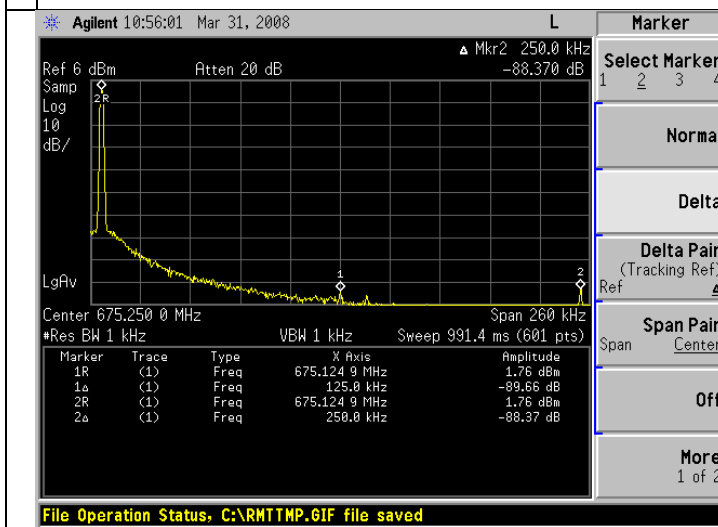
Fractional Spurs (Internal Divide by 2 Enabled)



Spur at 250 kHz offset at a frequency of 635.125 MHz is -84.2 dBc. Since this mode uses the divide by 2 mode, the channel spacing here is actually 125 kHz. If there was a fractional spur at 125 kHz, it could be eliminated by doubling the channel spacing before the divider.

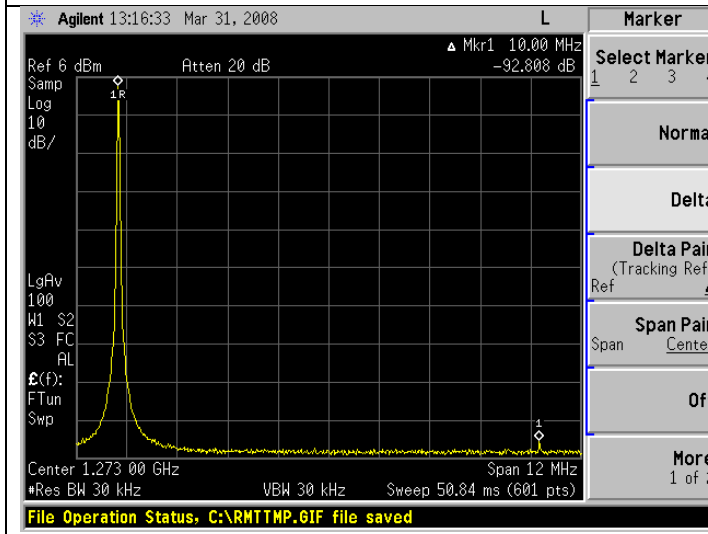


Spur at 250 kHz offset for a frequency of 655.125 MHz is -83.2 dBc.

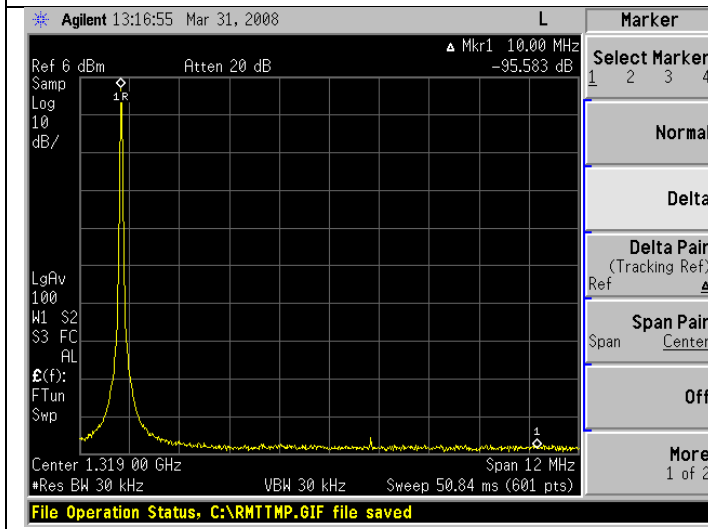


Spur at 250 kHz offset for a frequency of 675.125 MHz is -88.4 dBc. The sub-fractional spur at 125 kHz offset of -89.7 dBc is also visible.

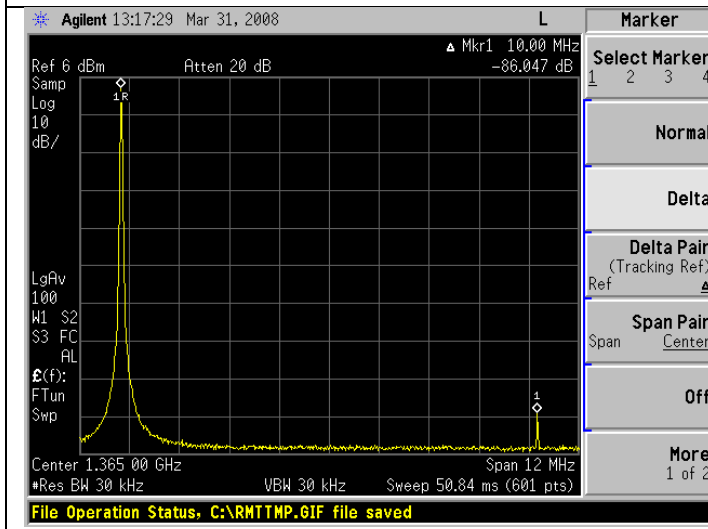
Integer Spurs (Internal Divide by 2 Enabled)



Spur at 10 MHz offset for a frequency of 1268 MHz is -92.8 dBc.

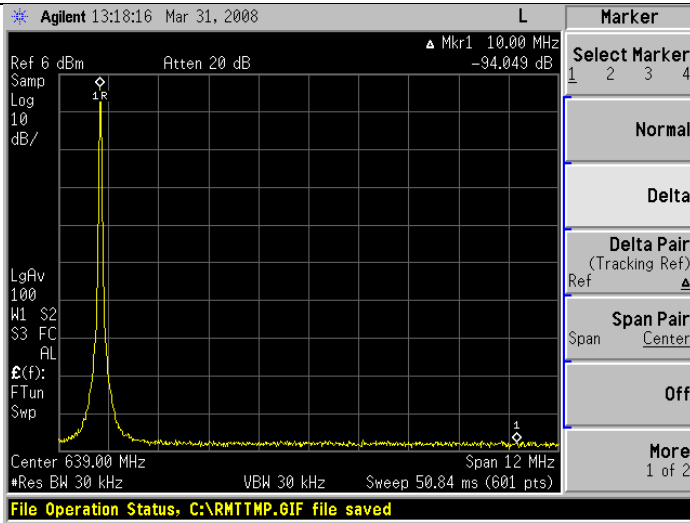


Spur at 10 MHz offset for a frequency of 1314 MHz is below the spectrum analyzer noise floor.

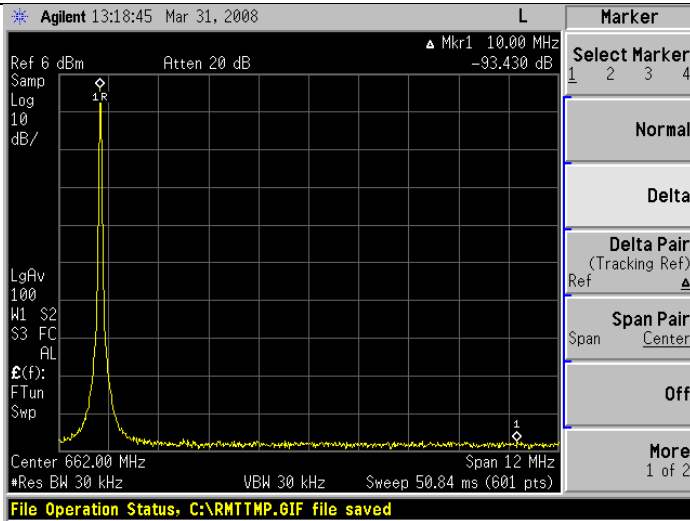


Spur at 10 MHz offset for a frequency of 1360 MHz is -86.0 dBc.

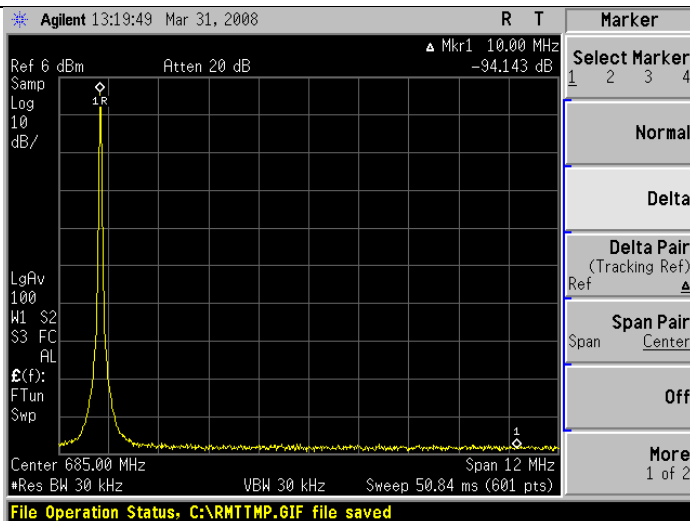
Integer Spurs (Internal Divide by 2 Enabled)



Spur at 10 MHz offset for a frequency of 634 MHz is below the spectrum analyzer noise floor.



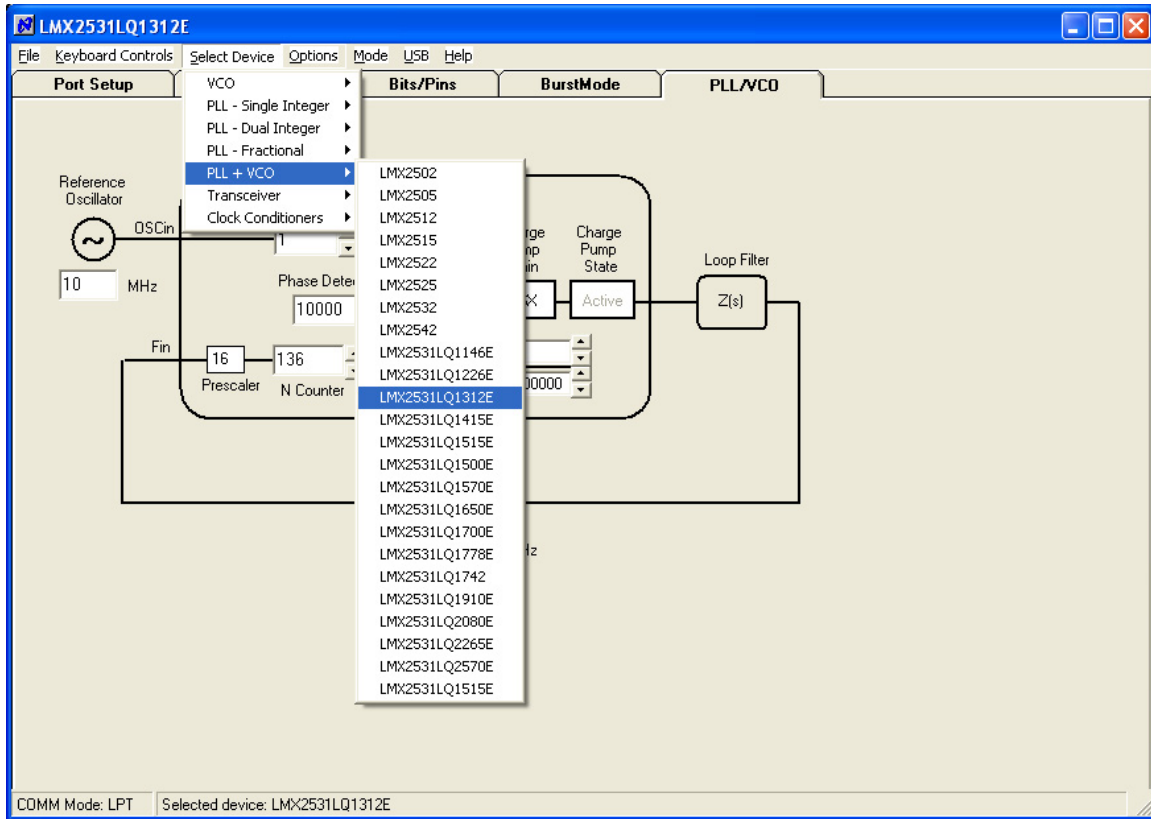
Spur at 10 MHz offset for a frequency of 657 MHz is below the spectrum analyzer noise floor.

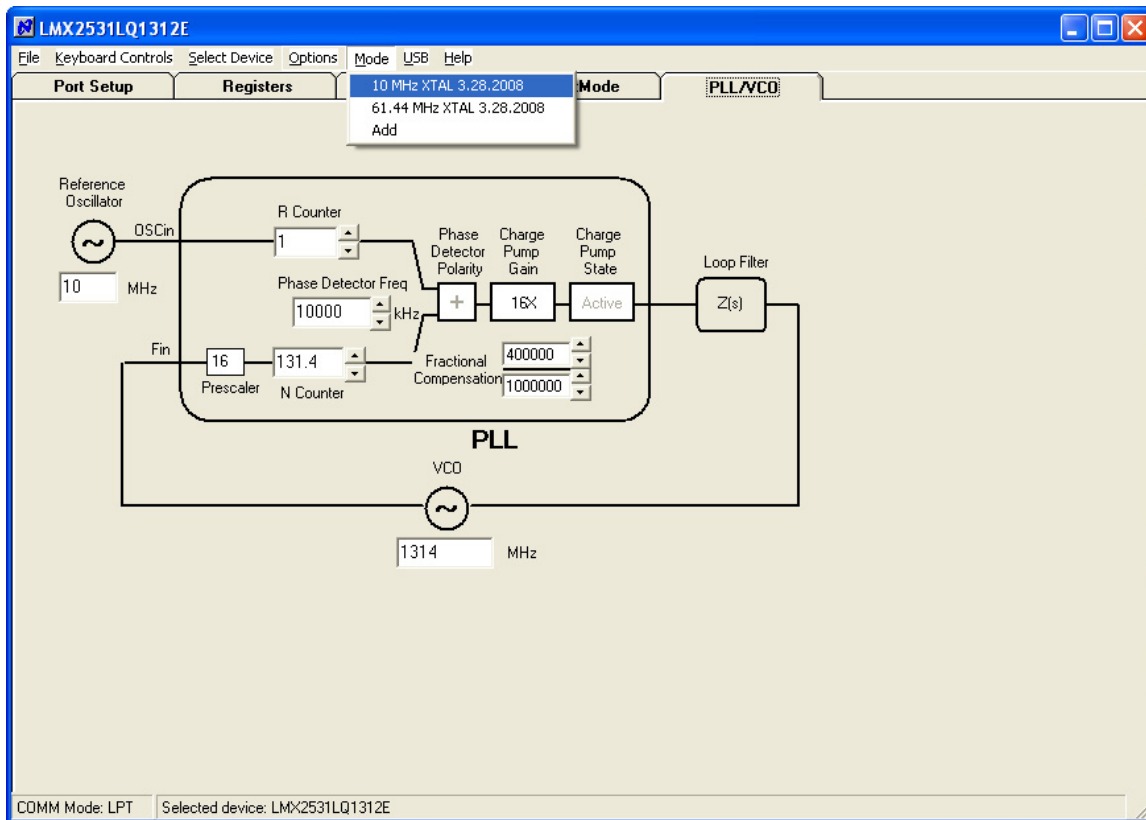


Spur at 10 MHz offset for a frequency of 685 MHz is below the spectrum analyzer noise floor.

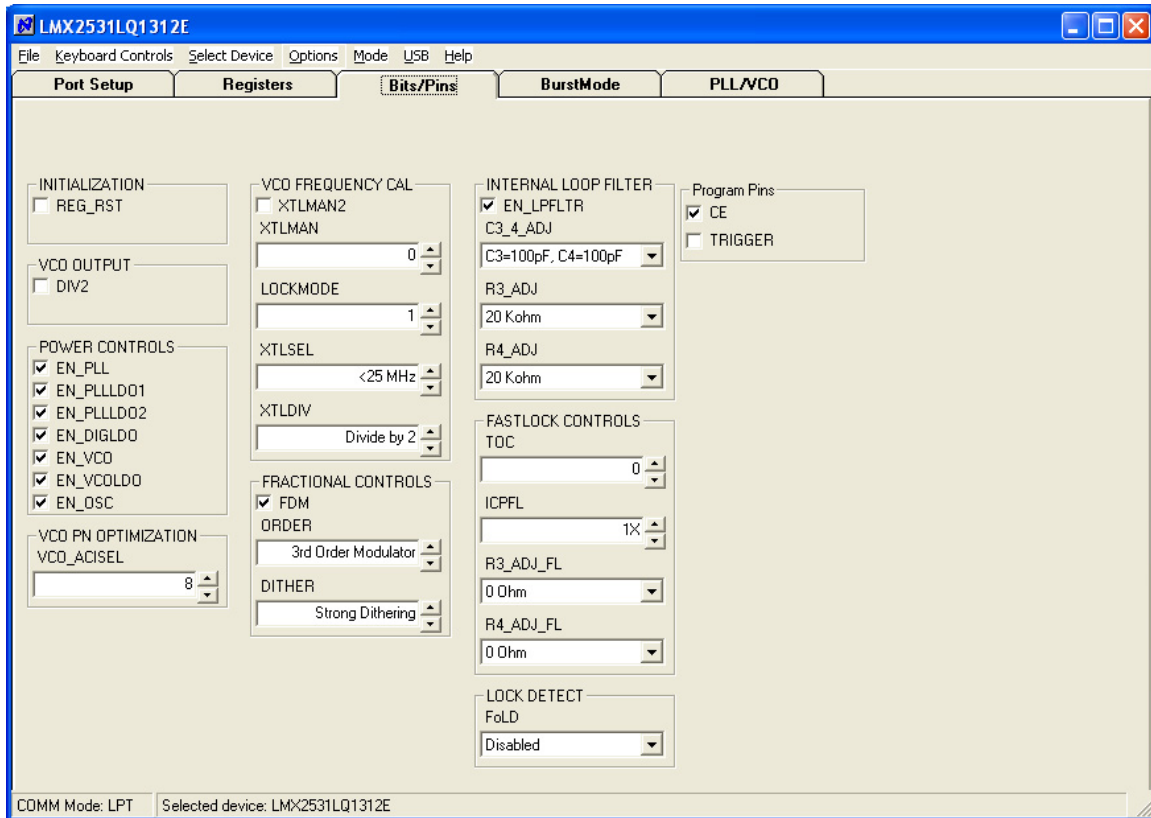
CodeLoader Settings

The CodeLoader program is designed to work with many devices. When CodeLoader is first started, it is necessary to select the correct device.



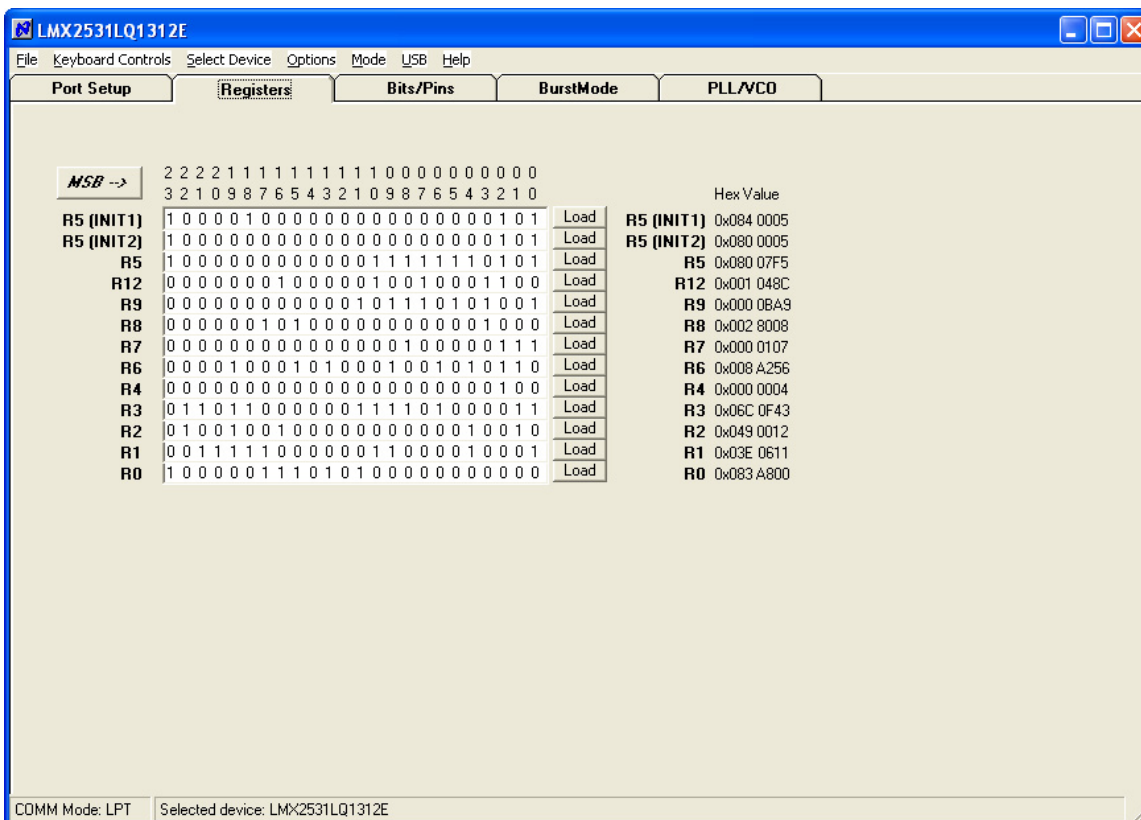


There can be different modes defined for a particular part. A mode can be recalled easily from the menu. This restores bit settings and frequencies, but not the Port Setup information. The default reference oscillator used for these instructions was 10 MHz, but there is an alternate mode for a 61.44 MHz oscillator as well. If the bits become scrambled, their original state may be recalled by choosing the appropriate mode. If the internal divide by 2 (DIV2) is enabled, the VCO frequency will not change.

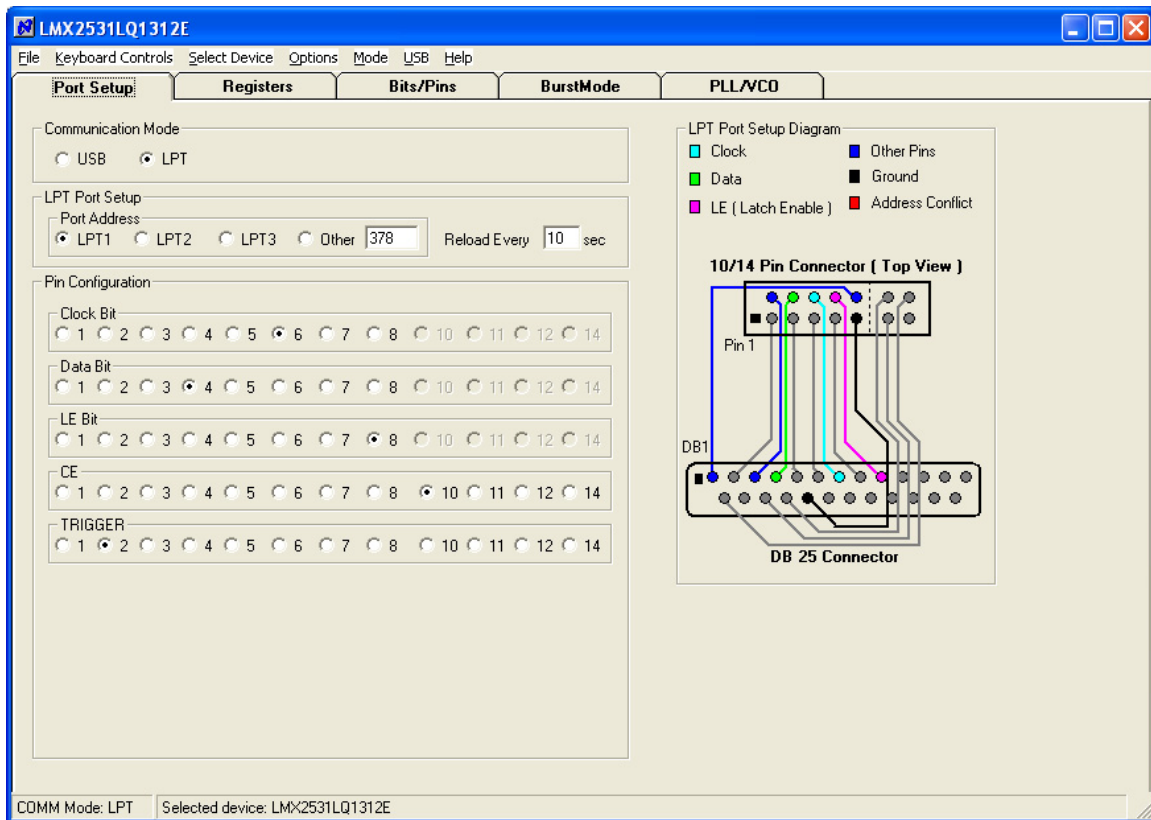


The Bits/Pins tab displays many of the bits used to program the part. Right mouse click any bit to view more information about what this does.

When the DIV2 bit is enabled, the frequency from the part will be half of that shown on the PLL/VCO tab. The frequency on the PLL/VCO tab does not reflect this because the divide by 2 is actually after the VCO. Also be sure to load the device (Ctrl+L) after changing this bit to allow the VCO to calibrate for optimal phase noise performance.

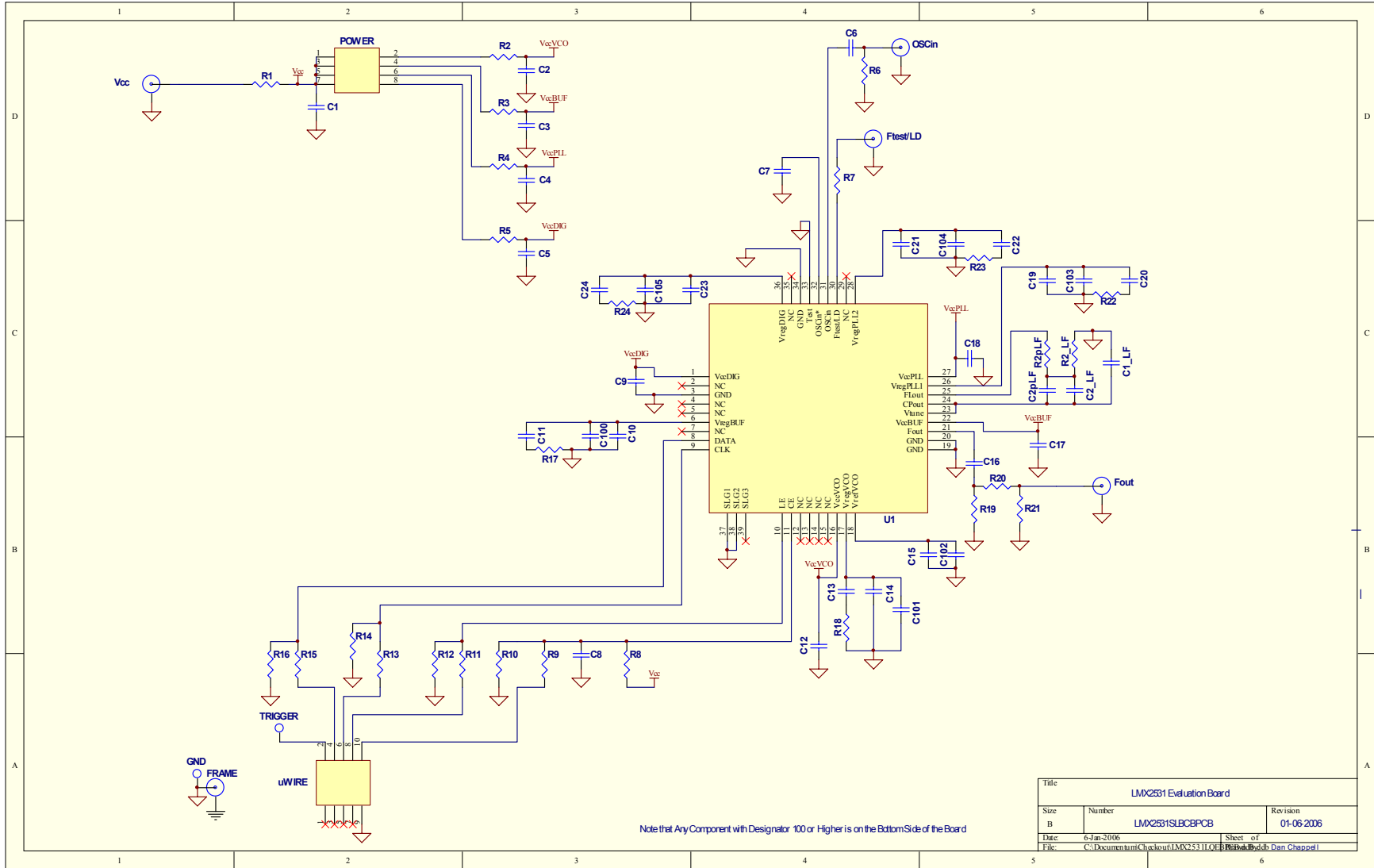


The Registers tab shows the literal bits that are being sent to the part. These are the registers every time the PLL is loaded by using the menu command or (Ctrl+L). R5 (INIT1) and R5 (INIT 2) are just the R5 register being used to properly initialize the part. So a single (Ctrl+L) will load the part.



The port setup tells CodeLoader what information goes where. If this is wrong, the part will not program. Although LPT1 is usually correct, CodeLoader does NOT automatically detect the correct port. On some laptops, it may be LPT3. Manually verification is required.

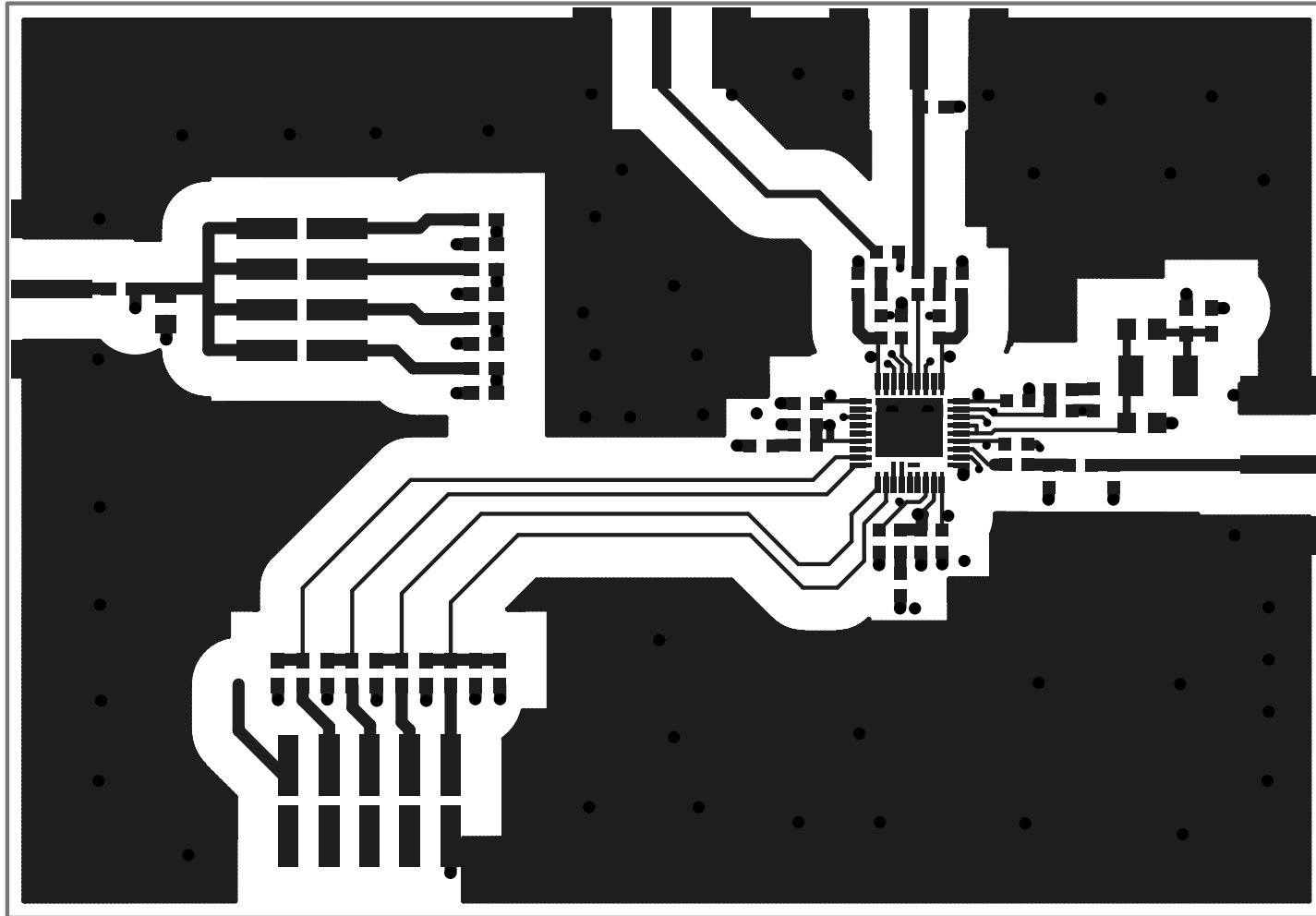
Schematic



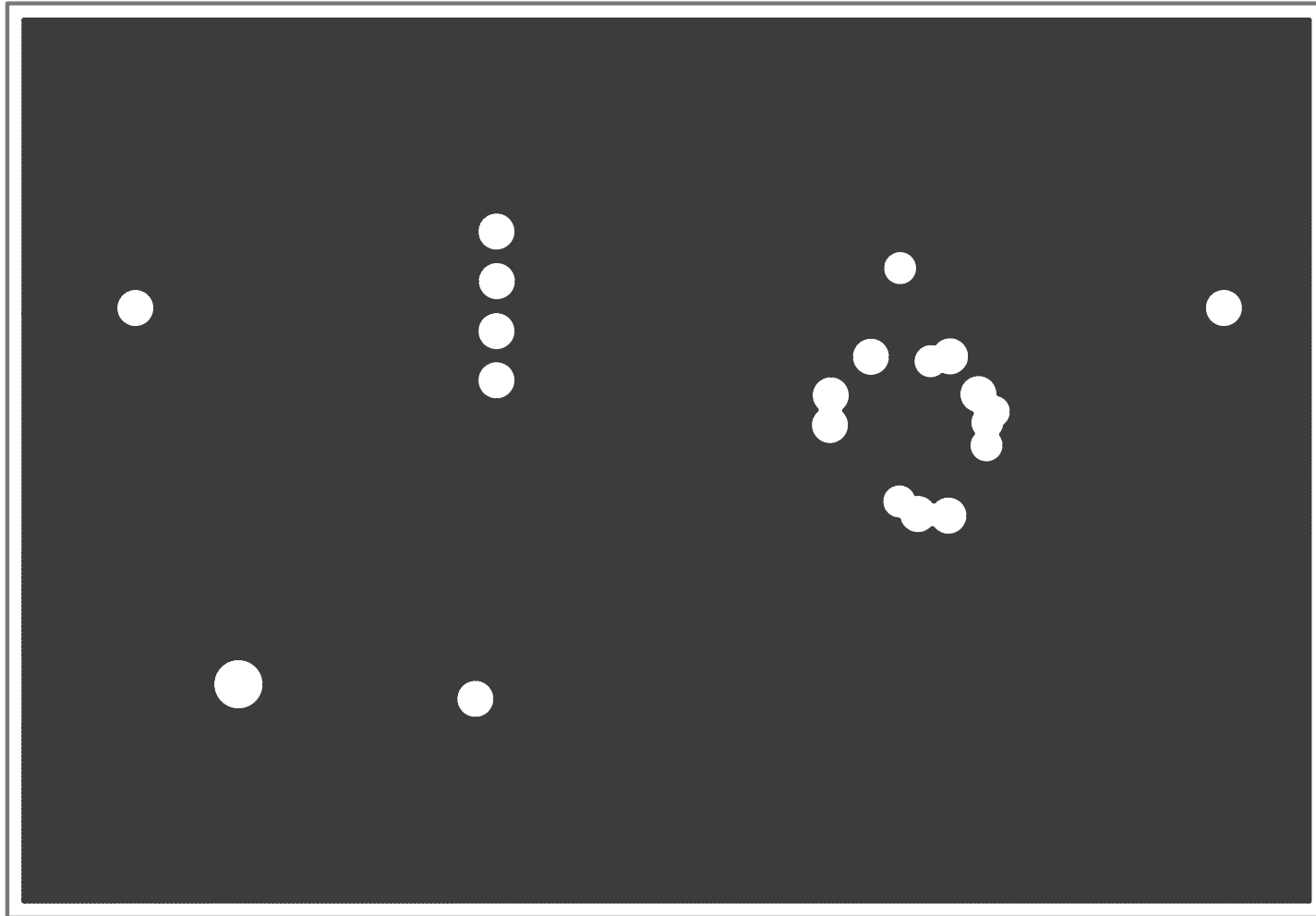
Bill of Materials

Bill of Materials				LMX2531_LF					Revision 3.28.2008	
Item	QTY	Manufacturer	Part #	Size	Tol	Voltage	Material	Value	Designators	
0	20		n/a					Open Capacitors	C1_LF, C2pLF, C2, C3, C4, C5, C9, C11, C14, C17, C18, C19, C21, C24, C100, C101, C102, C103, C104, C105	
	Open Resistors							R2pLF, R7, R8, R17, R19, R21, R24		
	Open Miscellaneous							Ftest/LD		
1	1	Kemet	C0603C101J5GAC	603	5%	50V	C0G	100pF	C16	
2	2	Kemet	C0603C103J5RAC	603	5%	50V	X7R	10nF	C10, C23	
3	1	Kemet	C0805C104K5RAC	805	5%	25V	C0G	100nF	C2_LF	
4	6	Kemet	C0603C104J3RAC	603	5%	25V	X7R	100nF	C6, C7, C12, C15, C22, C20	
5	1	Kemet	C0603C105K4RAC	603	10%	16V	X5R	1uF	C8	
6	1	Kemet	C0603C475K9PAC	603	10%	6.3V	X5R	4.7uF	C13	
7	1	Kemet	C0805C106K8PAC	805	10%	10V	X5R	10uF	C1	
8	1	Vishay	CRCW0603000ZRT1	603	5%	0.1W	Thick Film	0Ω	R20	
9	2	Panasonic	P.22AHCT-ND	603	10%	0.1W	Thick Film	0.22Ω	R22, R23	
10	2	Vishay	CRCW06033R3JRT1	603	5%	0.1W	Thick Film	3.3Ω	R1, R18	
11	4	Vishay	CRCW0603100JRT1	603	5%	0.1W	Thick Film	10Ω	R2, R3, R4, R5	
12	1	Vishay	CRCW0603510JRT1	603	5%	0.1W	Thick Film	51Ω	R6	
13	1	Vishay	CRCW0603102JRT1	603	5%	0.1W	Thick Film	1KΩ	R2_LF	
14	4	Vishay	CRCW0603103JRT1	603	5%	0.1W	Thick Film	10KΩ	R9, R11, R13, R15	
15	4	Vishay	CRCW0603123JRT1	603	5%	0.1W	Thick Film	12KΩ	R10, R12, R14, R16	
16	1	Comm Con Connectors	HTSM3203-8G2	2X4	n/a	n/a	Metal/Plastic	Header	POWER	
17	1	FCI Electronics	52601-S10-8	2X5	n/a	n/a	Metal/Plastic	Header	uWire	
18	3	Johnson Components	142-0701-851	SMA	n/a	n/a	Metal	SMA	Fout, OSCin, Vcc	
19	1	National Semiconductor	LMX2531LQEBPCB	n/a	n/a	n/a	FR4	PCB Board	n/a	
							62 mil Thick	1st Layer 10 mils		
20	1	National Semiconductor	LMX2531	LLP36	n/a	2.7	Silicon	LMX2531	U1	
21	4	Com Con Connectors	CCIJ255G	2-Pin	n/a	n/a	Metal/Plastic	Shunt	Place Across:	
									POWER: 1-2, 3-4, 5-6, 7-8	
22	4	SPC Technology	SPCS-8	0.156"	n/a	n/a	Nylon	Nylon Standoffs	Place in 4 Holes in Corners of Board	

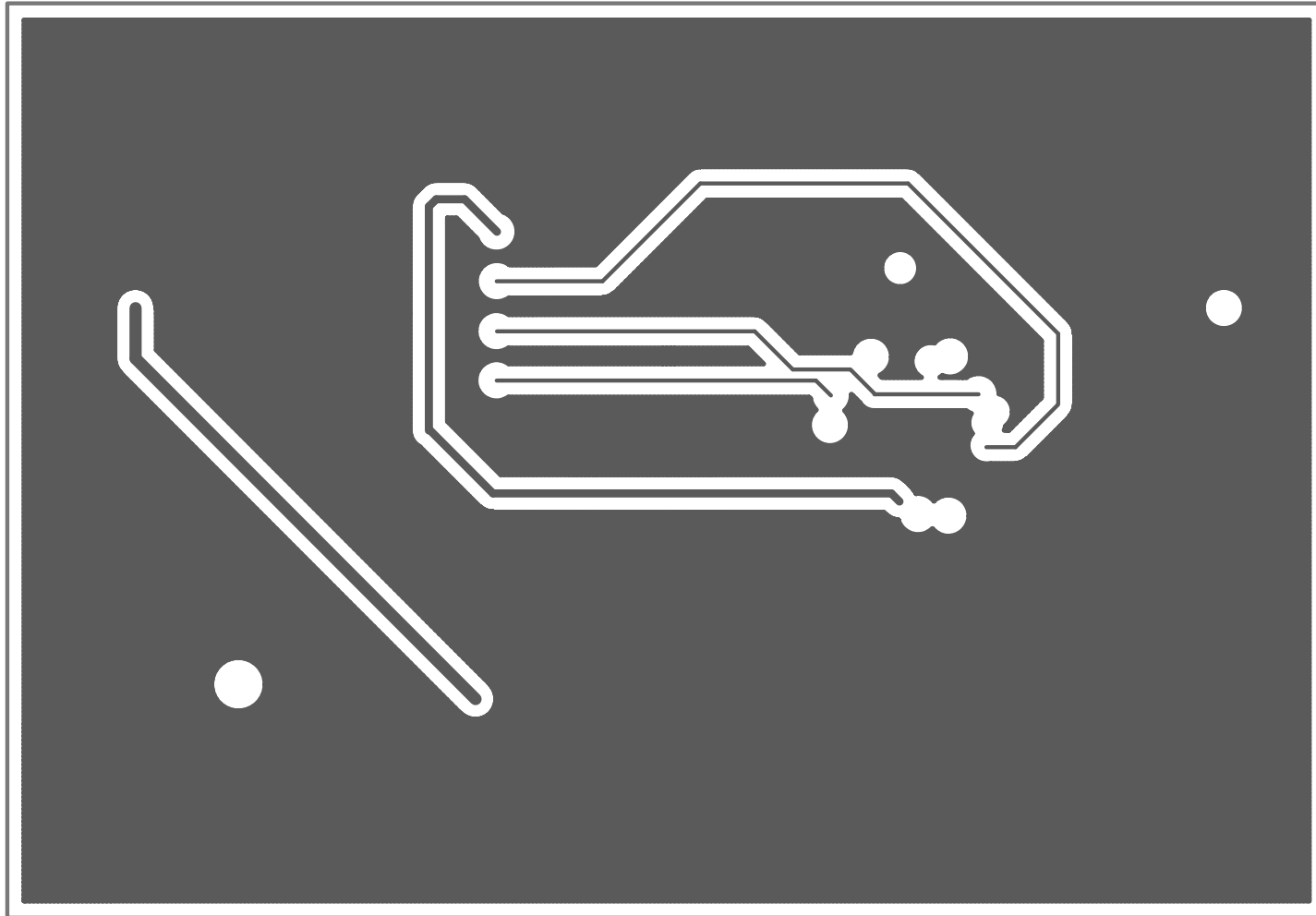
Top Layer



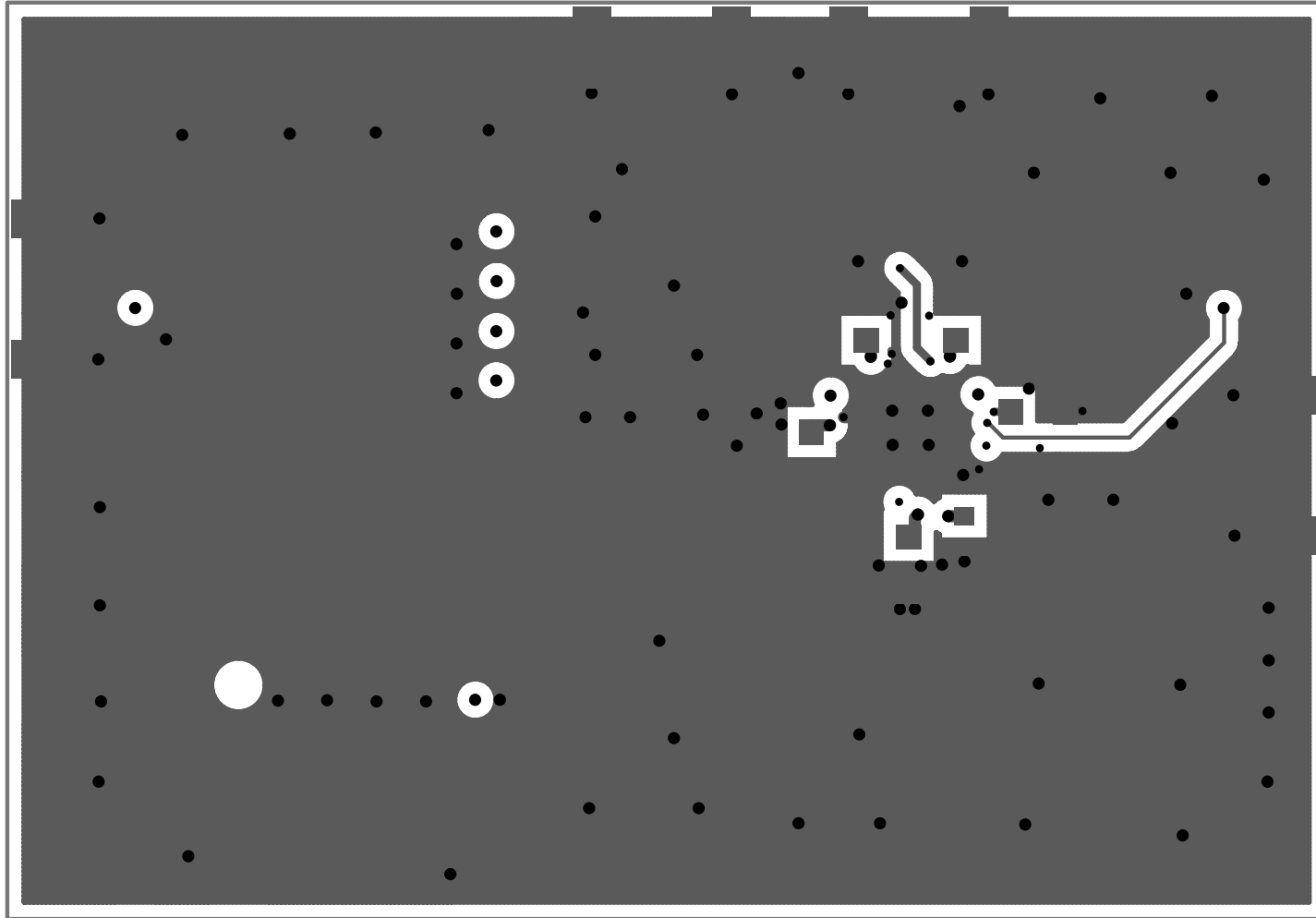
Mid Layer 1 "Ground Plane" (15 Mils Down FR4)



Mid Layer 2 "Power"

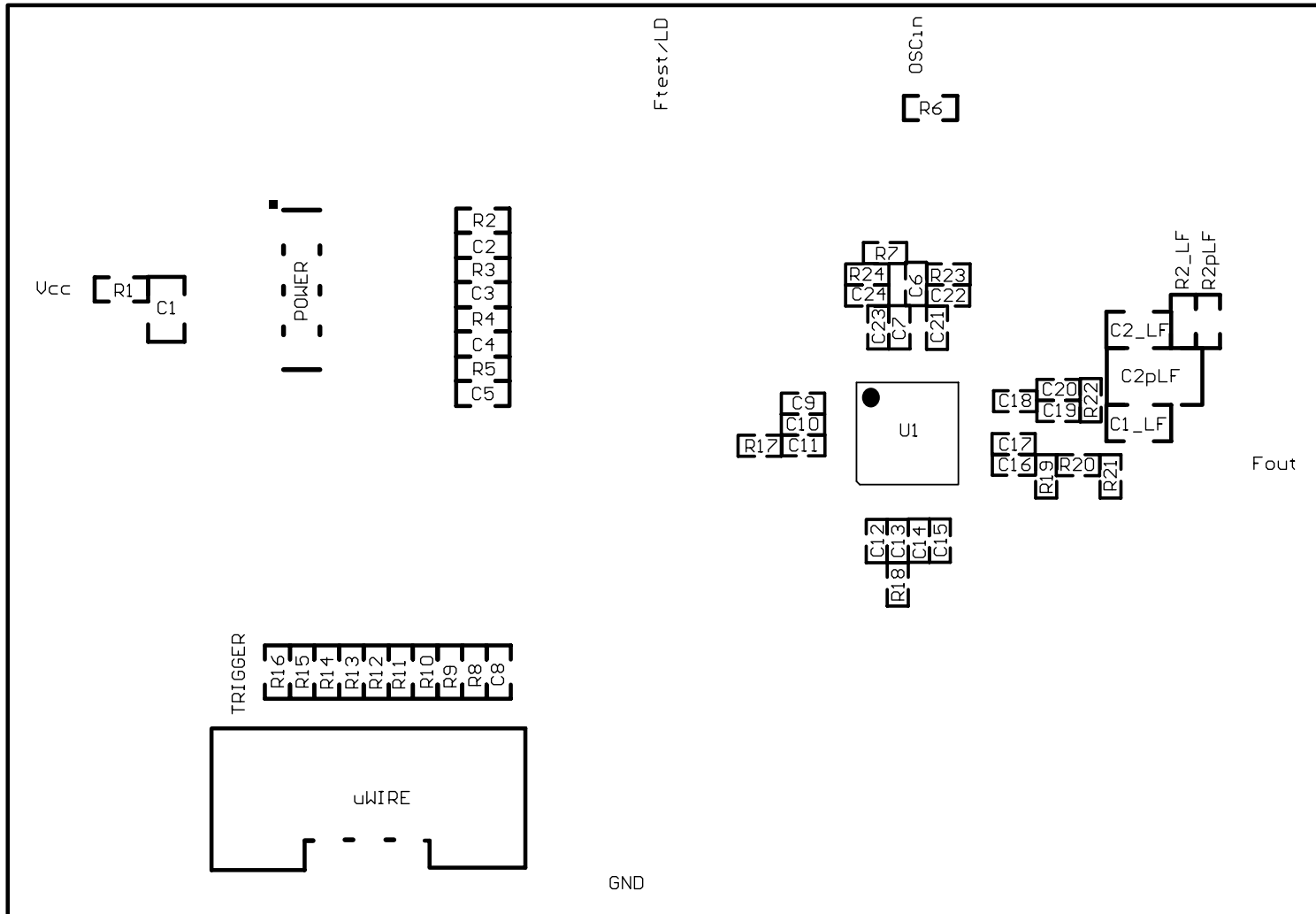


Bottom Layer "Signal"



Note: Total Board Thickness = 61 mils

Top Build Diagram



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Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
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