NP501-00020-2v0-E

FRAM
MB85RC64A

MB85RC64A is a 64K-bits FRAM LSI with serial interface (I^2C), using the ferroelectric process and CMOS process technologies for forming the nonvolatile memory cells. Because FRAM is able to write high-speed even though a nonvolatile memory, it is suitable for the log management and the storage of the resume data, etc.

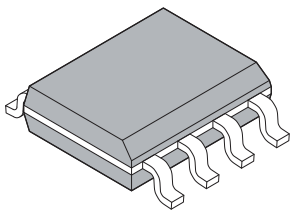
■ FEATURES

- **Bit configuration** : 8,192 words × 8 bits
- **Two-wire serial interface** : Fully controllable by two ports: serial clock (SCL) and serial data (SDA)
- **Operating frequency** : 1 MHz (Max)
- **Read/write endurance** : 10^{12} times / byte
- **Data retention** : 10 years (+ 85 ℃), 95 years (+ 55 ℃), over 200 years (+ 35 ℃)
- **Operating power supply voltage** : 2.7V to 3.6V
- **Low power consumption** : Operating power supply current 250 μA (Typ@1MHz)
  Standby current 5 μA (Typ)
- **Operating ambient temperature range** : -40 ℃ to +85 ℃
- **Package** : 8-pin plastic SOP (FPT-8P-M02)
  RoHS compliant

■ ORDERING INFORMATION

Product name	Package	Shipping form
MB85RC64APNF-G-JNE1	8-pin plastic SOP (FPT-8P-M02) 3.90mm×5.05mm, 1.27mm pitch	Tube
MB85RC64APNF-G-JNERE1	8-pin plastic SOP (FPT-8P-M02) 3.90mm×5.05mm, 1.27mm pitch	Embossed Carrier tape

■ PACKAGE EXAMPLE OF REFERENCE

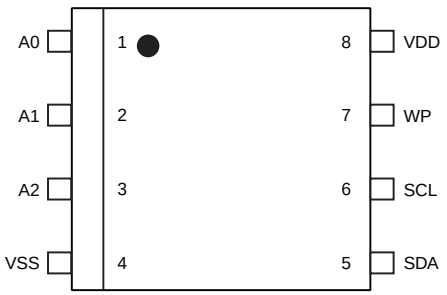


8-pin plastic SOP

(FPT-8P-M02)

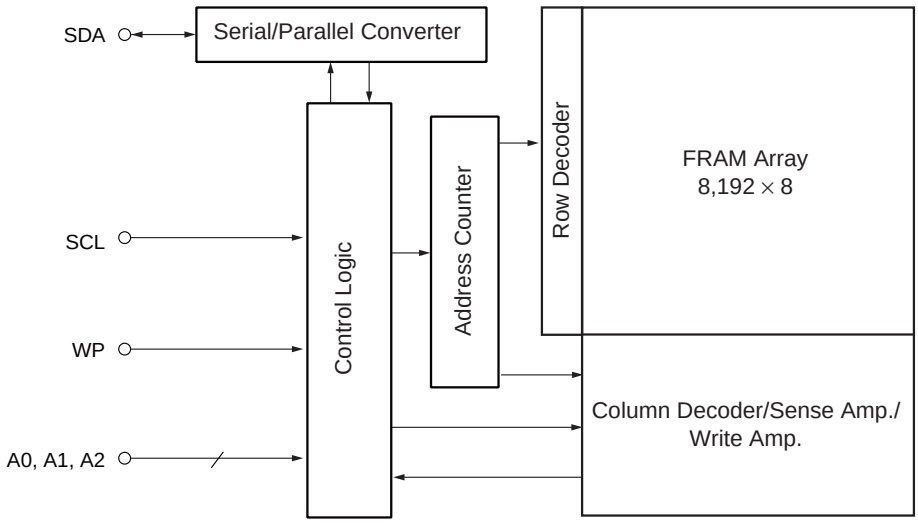
■ PIN ASSIGNMENT

(TOP VIEW)



Pin No.	Pin name	Description
1 to 3	A0 to A2	Device Address pins MB85RC64 can be connected to the same data bus up to 8 devices. Device addresses are used in order to identify each of the devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pin matches a Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A0, A1, and A2 pins are internally pulled-down and recognized as the "L" level.
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output so a pull-up resistor is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output timing serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When the Write Protect pin is the "H" level, the writing operation is disabled. When the Write Protect pin is the "L" level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The write protect pin is internally pull-down to VSS pin, and that is recognized as the "L" level (write enable) when the pin is the open state.
8	VDD	Supply Voltage pin

■ BLOCK DIAGRAM



■ I²C

MB85RC64A has a two-wire serial interface; the I²C bus, and operates as a slave device. The I²C bus defines communication roles of "master" and "slave" devices, with the master side holding the authority to initiate control. Furthermore, an I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.