

FEATURES

- Single-Chip Mixer/Oscillator and Phase-Locked Loop (PLL) Synthesizer
- Three-Band Local Oscillator and Mixer
- Inter-Integrated Circuit (I²C) Bus Protocol (Bidirectional Data Transmission)
- 30-V Tuning-Voltage Output
- Four NPN-Type Band-Switch (BS) Drivers
- Programmable Reference Divider Ratio (512, 640, or 1024)
- 5-V Power Supply
- 32-Pin Thin Shrink Small-Outline Package (TSSOP)

APPLICATIONS

- TVs
- VCR/DVD Recorders
- Set-Top Boxes

DESCRIPTION

The SN761683B is a synthesized tuner IC designed for TV tuning systems. The circuit consists of a phase-locked loop (PLL) synthesizer, three-band local oscillator and mixer, 30-V output tuning amplifier, and four NPN band-switch drivers, and is available in a small-outline package. A 15-bit programmable counter and reference divider are controlled by inter-integrated circuit (I²C) bus protocol.

**TSSOP PACKAGE
(TOP VIEW)**

| | | | |
|------------|----|----|------------|
| VLO OSC B | 1 | 32 | UHF RF IN2 |
| VLO OSC C | 2 | 31 | UHF RF IN1 |
| OSC GND | 3 | 30 | VHF RF IN2 |
| VHI OSC B | 4 | 29 | VHF RF IN1 |
| VHI OSC C | 5 | 28 | RF GND |
| UHF OSC B1 | 6 | 27 | MIX OUT2 |
| UHF OSC C1 | 7 | 26 | MIX OUT1 |
| UHF OSC C2 | 8 | 25 | BS4 |
| UHF OSC B2 | 9 | 24 | BS3 |
| IF GND | 10 | 23 | BS2 |
| IF OUT1 | 11 | 22 | BS1 |
| IF OUT2 | 12 | 21 | NC |
| VCC | 13 | 20 | ADC |
| CP | 14 | 19 | AS |
| VTU | 15 | 18 | SDA |
| XTAL | 16 | 17 | SCL |

NC – No internal connection

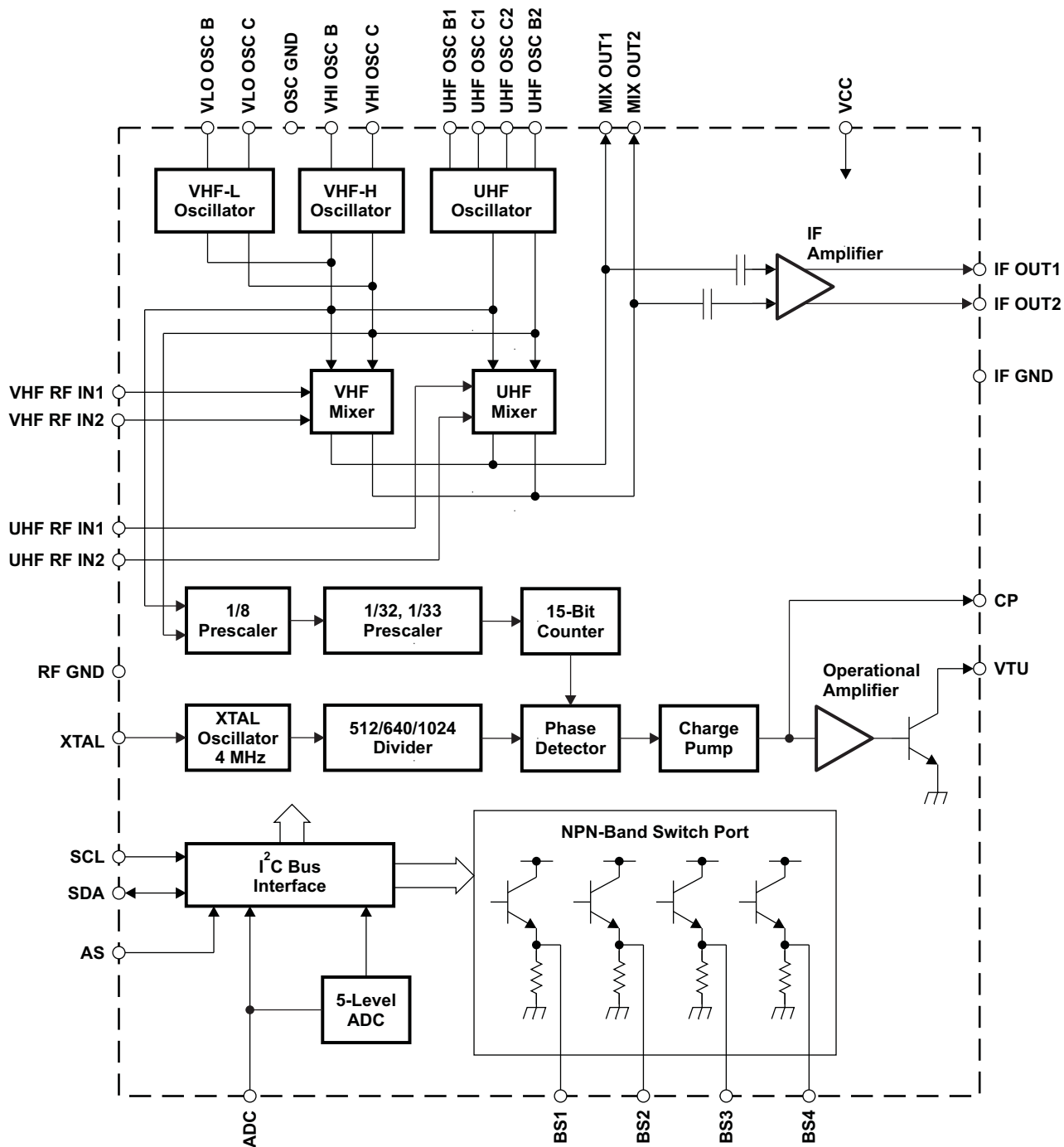


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the bipolar device.

FUNCTIONAL BLOCK DIAGRAM



B0089-02

TERMINAL FUNCTIONS

| TERMINAL NAME | NO. | DESCRIPTION | SCHEMATIC |
|------------------|-----|--|---------------------------|
| ADC | 20 | ADC input | Figure 1 |
| AS | 19 | Address selection input | Figure 2 |
| BS1 | 22 | Band-switch 1 output (NPN emitter follower) | Figure 3 |
| BS2 | 23 | Band-switch 2 output (NPN emitter follower) | Figure 3 |
| BS3 | 24 | Band-switch 3 output (NPN emitter follower) | Figure 3 |
| BS4 | 25 | Band-switch 4 output (NPN emitter follower) | Figure 3 |
| CP | 14 | Charge-pump output | Figure 4 |
| IF GND | 10 | IF ground | |
| IF OUT1 | 11 | IF output 1 | Figure 5 |
| IF OUT2 | 12 | IF output 2 | Figure 5 |
| MIX OUT1 | 26 | Mixer output 1 | Figure 6 |
| MIX OUT2 | 27 | Mixer output 2 | Figure 6 |
| NC | 21 | No connection | |
| OSC GND | 3 | Oscillator ground | |
| RF GND | 28 | RF ground | |
| SCL | 17 | Serial clock input | Figure 7 |
| SDA | 18 | Serial data input/output | Figure 8 |
| UHF OSC B1 | 6 | UHF oscillator base 1 | Figure 9 |
| UHF OSC B2 | 9 | UHF oscillator base 2 | Figure 9 |
| UHF OSC C1 | 7 | UHF oscillator collector 1 | Figure 9 |
| UHF OSC C2 | 8 | UHF oscillator collector 2 | Figure 9 |
| UHF RF IN1 | 31 | UHF RF input 1 | Figure 10 |
| UHF RF IN2 | 32 | UHF RF input 2 | Figure 10 |
| VCC | 13 | Supply voltage for mixer/oscillator/PLL: 5 V | |
| VHF RF IN1 | 29 | VHF RF input 1 | Figure 11 |
| VHF RF IN2 | 30 | VHF RF input 2 | Figure 11 |
| VHI OSC B | 4 | VHF HIGH oscillator base | Figure 12 |
| VHI OSC C | 5 | VHF HIGH oscillator collector | Figure 12 |
| VLO OSC B | 1 | VHF LOW oscillator base | Figure 13 |
| VLO OSC C | 2 | VHF LOW oscillator collector | Figure 13 |
| VTU | 15 | Tuning voltage amplifier output | Figure 14 |
| XTAL | 16 | 4-MHz crystal oscillator input | Figure 15 |

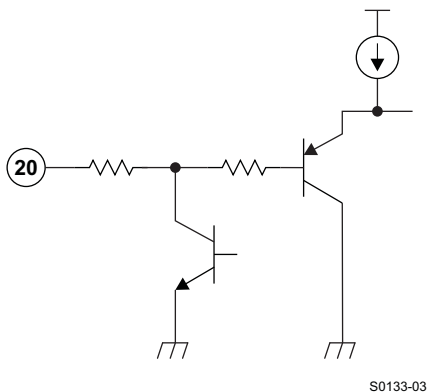


Figure 1.

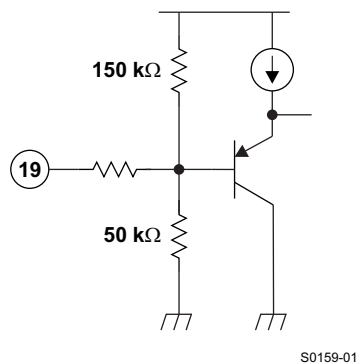


Figure 2.

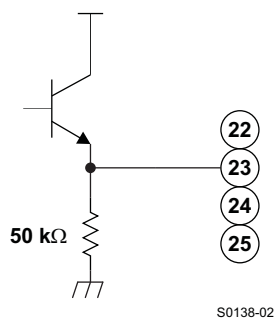


Figure 3.

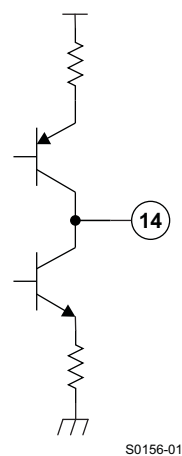


Figure 4.

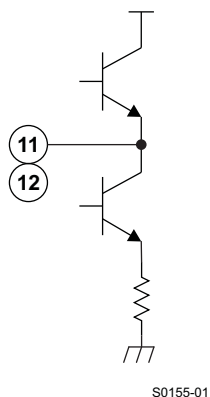


Figure 5.

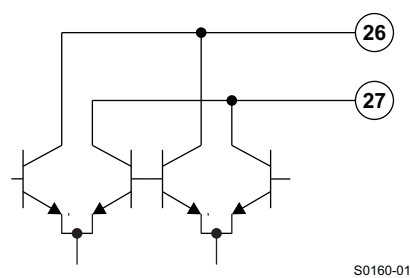


Figure 6.

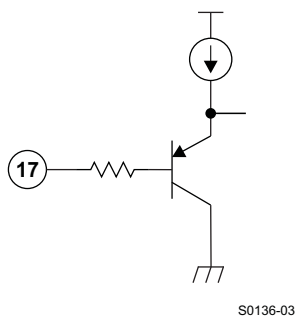


Figure 7.

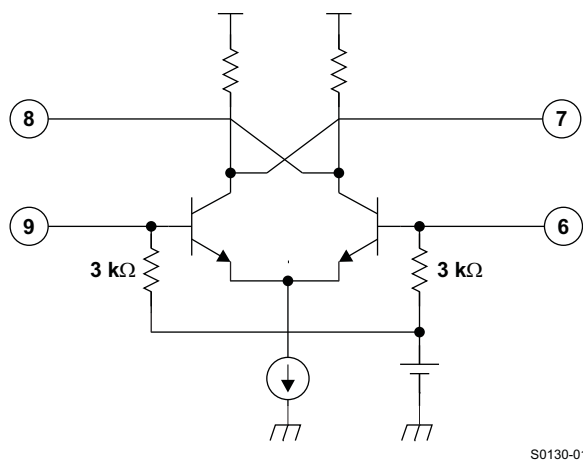


Figure 9.

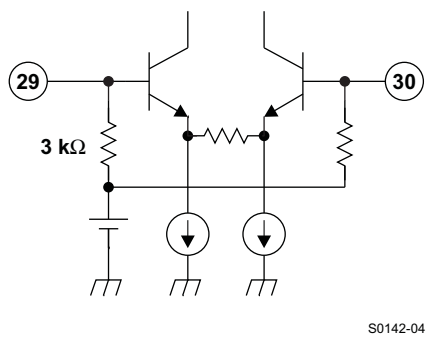


Figure 11.

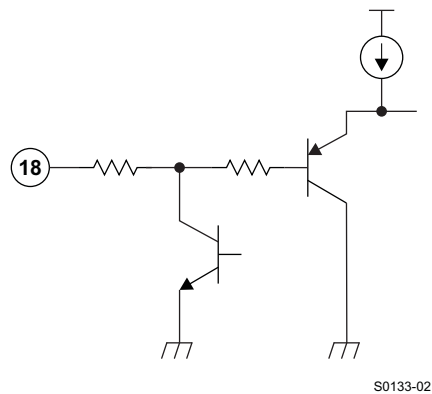


Figure 8.

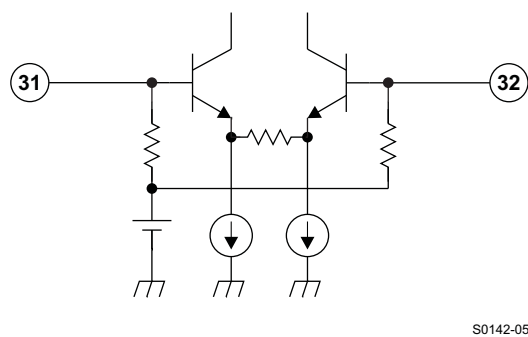


Figure 10.

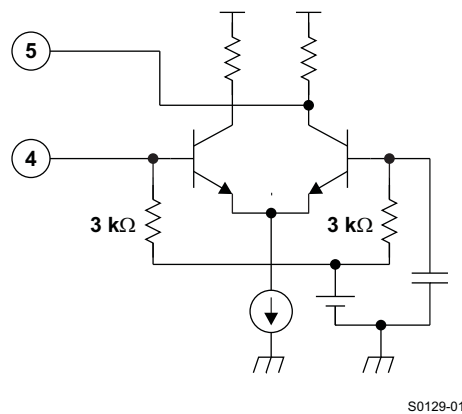


Figure 12.

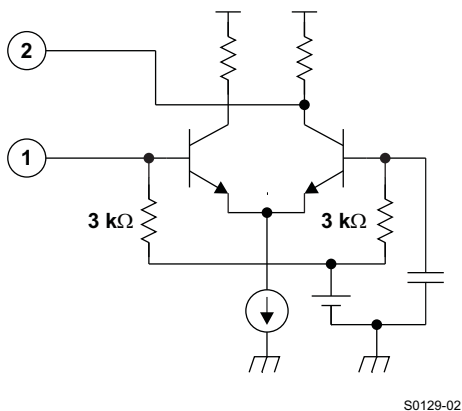


Figure 13.

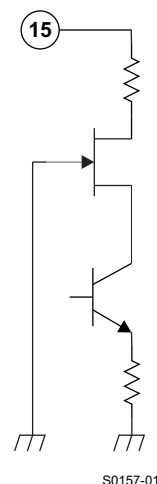


Figure 14.

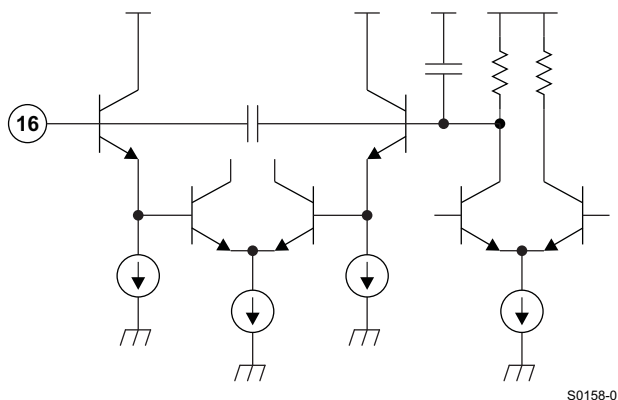


Figure 15.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|----------------------|---|--|------|------|------|
| V _{CC} | Supply voltage range ⁽²⁾ | VCC | –0.4 | 6.5 | V |
| V _{GND} | Input voltage range 1 ⁽²⁾ | RF GND, OSC GND | –0.4 | 0.4 | V |
| V _{VTU} | Input voltage range 2 ⁽²⁾ | VTU | –0.4 | 35 | V |
| V _{IN} | Input voltage range 3 ⁽²⁾ | All other pins | –0.4 | 6.5 | V |
| P _D | Continuous total dissipation ⁽³⁾ | T _A ≤ 25°C | | 1040 | mW |
| T _A | Operating free-air temperature range | | –20 | 85 | °C |
| T _{stg} | Storage temperature range | | –65 | 150 | °C |
| T _{JC} | Maximum junction temperature | | | 150 | °C |
| t _{SC(max)} | Maximum short-circuit time | All pins to VCC, All pins to IFGND, OSCGND, RFGND | | 10 | s |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Voltage values are with respect to IF GND.

(3) Derating factor is 8.33 mW/°C for T_A ≥ 25°C.

Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------------|-------------|-----|-----|------|
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V _{TU} | Tuning supply voltage | | 30 | 33 | V |
| I _{BS} | Output current of band switch | One port on | | 10 | mA |
| T _A | Operating free-air temperature | –20 | | 85 | °C |

Total Device and Serial Interface Electrical Characteristics

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|--|---|-----|-----------------|------|
| I _{CC1} | Supply current 1 | | | 60 | | mA |
| I _{CC2} | Supply current 2 | One band switch on (I _{BS} = 10 mA) | | 70 | | mA |
| V _{IH} | High-level input voltage | SCL, SDA | 2.8 | | V _{CC} | V |
| V _{IL} | Low-level input voltage | SCL, SDA | | | 1.4 | V |
| I _{IH} | High-level input current | SCL, SDA | | | 10 | μA |
| I _{IL} | Low-level input current | SCL, SDA | –10 | | | μA |
| V _{POR} | Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode) | | 2.1 | 2.8 | 3.6 | V |
| I²C Interface | | | | | | |
| V _{ASH} | Address-select high-input voltage | AS | V _{CC} = 5 V | 4.5 | 5 | V |
| V _{ASM1} | Address-select mid1-input voltage | AS | V _{CC} = 5 V | 2 | 3 | V |
| V _{ASM2} | Address-select mid2-input voltage | AS | V _{CC} = 5 V | 1 | 1.5 | V |
| V _{ASL} | Address-select low-input voltage | AS | V _{CC} = 5 V | | 0.5 | V |
| I _{ASH} | Address-select high-input current | AS | | | 140 | μA |
| I _{ASL} | Address-select low-input current | AS | –50 | | | μA |
| V _{ADC} | ADC input voltage | See Table 8 | 0 | | V _{CC} | V |
| I _{ADH} | ADC high-level input current | V _{ADC} = V _{CC} | | | 10 | μA |
| I _{ADL} | ADC low-level input current | V _{ADC} = 0 V | –50 | | | μA |
| V _{OL} | Low-level output voltage | SDA | V _{CC} = 5 V, I _{OL} = 3 mA | | 0.4 | V |
| I _{SDAH} | High-level output leakage current | SDA | V _{SDA} = 5.5 V | | 10 | μA |
| f _{SCL} | Clock frequency | SCL | | 100 | 400 | kHz |
| t _{hd(DAT)} | Data hold time | See Figure 16 | 0 | | | μs |
| t _(BUF) | Bus free time | See Figure 16 | 1.3 | | | μs |
| t _{hd(STA)} | Start hold time | See Figure 16 | 0.6 | | | μs |
| t _(LOW) | SCL-low hold time | See Figure 16 | 1.3 | | | μs |
| t _(HIGH) | SCL-high hold time | See Figure 16 | 0.6 | | | μs |
| t _{su(STA)} | Start setup time | See Figure 16 | 0.6 | | | μs |
| t _{su(DAT)} | Data setup time | See Figure 16 | 0.1 | | | μs |
| t _r | SCL, SDA rise time | See Figure 16 | | | 0.3 | μs |
| t _f | SCL, SDA fall time | See Figure 16 | | | 0.3 | μs |
| t _{su(STO)} | Stop setup time | See Figure 16 | 0.6 | | | μs |

PLL and Band-Switch Electrical Characteristics

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $T_A = -20^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---|--|-----|------|-------|------------|
| N | Divider ratio | 15-bit frequency word | 256 | | 32767 | |
| f_{XTAL} | Crystal oscillator frequency | $R_{XTAL} = 25\ \Omega \text{ to } 300\ \Omega$ | 3.2 | 4 | 4.48 | MHz |
| Z_{XTAL} | Crystal oscillator input impedance | | | 1.6 | | k Ω |
| V_{IXTAL2} | Minimum reference input sensitivity | XTAL 4 MHz, AC coupling with 0.1- μ F capacitor | | | 100 | mVp-p |
| V_{VTUL} | Tuning amplifier low-level output voltage | $R_L = 27\text{ k}\Omega$, $V_{TU} = 33\text{ V}$ | | 0.4 | 0.5 | V |
| I_{VTUOFF} | Tuning amplifier leakage current (OFF) | OS = 1, $V_{TU} = 33\text{ V}$ | | | 10 | μ A |
| I_{CPH} | Charge-pump high-level input current | CP = 1 | | 280 | | μ A |
| I_{CPL} | Charge-pump low-level input current | CP = 0 | | 60 | | μ A |
| V_{CP} | Charge-pump output voltage | PLL locked | | 1.95 | | V |
| I_{CPOFF} | Charge-pump leakage current | T2 = 0, T1 = 1, $V_{CP} = 2\text{ V}$, $T_A = 25^\circ\text{C}$ | -15 | | 15 | nA |
| I_{BS} | Band-switch driver output current | | | | 10 | mA |
| V_{BS1} | Band-switch driver output voltage | $I_{BS} = 10\text{ mA}$ | 3 | | | V |
| V_{BS2} | | $I_{BS} = 10\text{ mA}$, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ | 3.5 | 3.9 | | |
| I_{BSOFF} | Band-switch driver leakage current | $V_{BS} = 0\text{ V}$ | | | 3 | μ A |

Mixer, Oscillator, IF Amplifier Electrical Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, measured in [Figure 17](#) reference measurement circuit at 50- Ω system,
IF filter characteristics: $f_{\text{peak}} = 43\text{ MHz}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|------------------------------|-----|-----|-----|--------|
| G _{c1} | Conversion gain (mixer-IF amplifier), VHF-LOW ⁽¹⁾ | f _{in} = 58 MHz | 22 | 25 | 28 | dB |
| G _{c3} | | f _{in} = 130 MHz | 22 | 25 | 28 | |
| G _{c4} | Conversion gain (mixer-IF amplifier), VHF-HIGH ⁽¹⁾ | f _{in} = 136 MHz | 22 | 25 | 28 | dB |
| G _{c6} | | f _{in} = 364 MHz | 22 | 25 | 28 | |
| G _{c7} | Conversion gain (mixer-IF amplifier), UHF ⁽¹⁾ | f _{in} = 370 MHz | 26 | 29 | 32 | dB |
| G _{c9} | | f _{in} = 804 MHz | 25 | 28 | 31 | |
| NF ₁ | Noise figure, VHF-LOW | f _{in} = 55.25 MHz | 9.5 | | | dB |
| NF ₃ | | f _{in} = 127.25 MHz | 9.5 | | | |
| NF ₄ | Noise figure, VHF-HIGH | f _{in} = 133.25 MHz | 10 | | | dB |
| NF ₆ | | f _{in} = 361.25 MHz | 10 | | | |
| NF ₇ | Noise figure, UHF | f _{in} = 367.25 MHz | 11 | | | dB |
| NF ₉ | | f _{in} = 801.25 MHz | 11 | | | |
| CM ₁ | 1% cross-modulation distortion, VHF-LOW ⁽²⁾ | f _{in} = 55.25 MHz | 89 | | | dBμV |
| CM ₃ | | f _{in} = 127.25 MHz | 89 | | | |
| CM ₄ | 1% cross-modulation distortion, VHF-HIGH ⁽²⁾ | f _{in} = 133.25 MHz | 86 | | | dBμV |
| CM ₆ | | f _{in} = 361.25 MHz | 86 | | | |
| CM ₇ | 1% cross-modulation distortion, UHF ⁽²⁾ | f _{in} = 367.25MHz | 87 | | | dBμV |
| CM ₉ | | f _{in} = 801.25 MHz | 87 | | | |
| V _{IFO1} | IF output voltage, VHF-LOW ⁽³⁾ | f _{in} = 55.25 MHz | 117 | | | dBμV |
| V _{IFO3} | | f _{in} = 127.25 MHz | 117 | | | |
| V _{IFO4} | IF output voltage, VHF-HIGH ⁽³⁾ | f _{in} = 133.25 MHz | 117 | | | dBμV |
| V _{IFO6} | | f _{in} = 361.25 MHz | 117 | | | |
| V _{IFO7} | IF output voltage, UHF ⁽³⁾ | f _{in} = 367.25MHz | 117 | | | dBμV |
| V _{IFO9} | | f _{in} = 801.25 MHz | 117 | | | |
| Φ _{OSC1} | Phase noise, VHF-LOW ⁽⁴⁾ | f _{in} = 55.25 MHz | 88 | | | dBc/Hz |
| Φ _{OSC3} | | f _{in} = 127.25 MHz | 88 | | | |
| Φ _{OSC4} | Phase noise, VHF-HIGH ⁽⁴⁾ | f _{in} = 133.25 MHz | 86 | | | dBc/Hz |
| Φ _{OSC6} | | f _{in} = 361.25 MHz | 86 | | | |
| Φ _{OSC7} | Phase noise, UHF ⁽⁴⁾ | f _{in} = 367.25MHz | 84 | | | dBc/Hz |
| Φ _{OSC9} | | f _{in} = 801.25 MHz | 84 | | | |
| Prescaler beat ⁽⁵⁾ | | | 25 | | | dBμV |

(1) IF = 43 MHz, RF input level = 80 dB μV

(2) $f_{\text{undes}} = f_{\text{des}} \pm 6\text{ MHz}$, Pin = 80 dB μV , AM 1 kHz, 30%, DES/CM = S/I = 46 dB

(3) IF = 45.75 MHz

(4) Offset = 10 kHz, RF input level = 70 dB μV

(5) Design parameter, not tested

FUNCTIONAL DESCRIPTION

I²C Bus Mode

I²C Write Mode (R/W = 0)

Table 1. Write Data Format

| | MSB | | | | | | | LSB | |
|-----------------------|-----|-----|-----|-----|-----|-----|-----|---------|------------------|
| Address byte (ADB) | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | R/W = 0 | A ⁽¹⁾ |
| Divider byte 1 (DB1) | 0 | N14 | N13 | N12 | N11 | N10 | N9 | N8 | A ⁽¹⁾ |
| Divider byte 2 (DB2) | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 | A ⁽¹⁾ |
| Control byte (CB) | 1 | CP | T2 | T1 | T0 | RSA | RSB | OS | A ⁽¹⁾ |
| Band-switch byte (BB) | X | X | X | X | BS4 | BS3 | BS2 | BS1 | A ⁽¹⁾ |

(1) Acknowledge

Table 2. I²C Write-Mode Data-Symbol Description

| SYMBOL | DESCRIPTION | DEFAULT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|---|------------------------|---------------|-----------------|---------------|-----------|---|---|---|-----|-----|---|---|---|---------|-----|---|---|---|----------|-----|---|---|------------------|----------|------------|---|---|---|-----|-----|---|---|------------------|-----|------------|---|---|------------------|-----|------------|---|---|------------------|-----|-----------------|---------------|
| MA1, MA0 | Address set bits (see Table 3) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| N14–N0 | Programmable counter set bits $N = N14 \times 2^{14} + N13 \times 2^{13} + \dots + N1 \times 2 + N0$ Oscillation frequency = $f_r \times 8 \times N$ f_r = Reference frequency = 4 MHz/Reference divider | Nn = 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CP | Charge-pump current set bit 60 μ A (CP = 0), 280 μ A (CP = 1) | CP = 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T2–T0 | Test bits (see Table 4) Normal mode: T2 = 0, T1 = 0, T0 = 1/0 | T2 = 0, T1 = 0, T0 = 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RSA, RSB | Reference divider ratio selection bits (see Table 6) | RSA = 0, RSB = 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| OS | Tuning amplifier control bit Tuning voltage on (OS = 0) Tuning voltage off, high impedance (OS = 1) | OS = 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BS4–BS1 | Band-switch ports control bits BS3 = 1: BS3 port ON BS3 = 0: BS3 port OFF Band selection by BS1, BS2, and BS4 bits: <table><thead><tr><th>BS1</th><th>BS2</th><th>BS4</th><th>SELECTED BAND</th><th>"ON" PORT</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>UHF</td><td>BS4</td></tr><tr><td>1</td><td>0</td><td>0</td><td>VHF-LOW</td><td>BS1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>VHF-HIGH</td><td>BS2</td></tr><tr><td>1</td><td>1</td><td>0⁽¹⁾</td><td>VHF-HIGH</td><td>(BS1, BS2)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>UHF</td><td>BS4</td></tr><tr><td>1</td><td>0</td><td>1⁽¹⁾</td><td>UHF</td><td>(BS1, BS4)</td></tr><tr><td>0</td><td>1</td><td>1⁽¹⁾</td><td>UHF</td><td>(BS2, BS4)</td></tr><tr><td>1</td><td>1</td><td>1⁽¹⁾</td><td>UHF</td><td>(BS1, BS2, BS4)</td></tr></tbody></table> ⁽¹⁾ These bit patterns are forbidden, due to limitation of band-switch output current. | BS1 | BS2 | BS4 | SELECTED BAND | "ON" PORT | 0 | 0 | 0 | UHF | BS4 | 1 | 0 | 0 | VHF-LOW | BS1 | 0 | 1 | 0 | VHF-HIGH | BS2 | 1 | 1 | 0 ⁽¹⁾ | VHF-HIGH | (BS1, BS2) | 0 | 0 | 1 | UHF | BS4 | 1 | 0 | 1 ⁽¹⁾ | UHF | (BS1, BS4) | 0 | 1 | 1 ⁽¹⁾ | UHF | (BS2, BS4) | 1 | 1 | 1 ⁽¹⁾ | UHF | (BS1, BS2, BS4) | BSn = 0 (UHF) |
| BS1 | BS2 | BS4 | SELECTED BAND | "ON" PORT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | UHF | BS4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | VHF-LOW | BS1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | VHF-HIGH | BS2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 ⁽¹⁾ | VHF-HIGH | (BS1, BS2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | UHF | BS4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 ⁽¹⁾ | UHF | (BS1, BS4) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 ⁽¹⁾ | UHF | (BS2, BS4) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 ⁽¹⁾ | UHF | (BS1, BS2, BS4) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | Don't care | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 3. Address Selection

| MA1 | MA0 | VOLTAGE APPLIED ON AS INPUT |
|-----|-----|---|
| 0 | 0 | LOW: 0 V to 0.1 V _{CC} |
| 0 | 1 | MID2: open, or 0.2 V _{CC} to 0.3 V _{CC} |
| 1 | 0 | MID1: 0.4 V _{CC} to 0.6 V _{CC} |
| 1 | 1 | HIGH: 0.9 V _{CC} to V _{CC} |

Table 4. Test Bits ⁽¹⁾

| T2 | T1 | T0 | DEVICE OPERATION | NOTE |
|----|----|----|------------------------|-------------------|
| 0 | 0 | 0 | Normal operation | |
| 0 | 0 | 1 | Normal operation | Default |
| 0 | 1 | X | Charge pump is off. | |
| 1 | 1 | 0 | Charge pump is sink. | |
| 1 | 1 | 1 | Charge pump is source. | |
| 1 | 0 | X | Test mode | ADC not available |

(1) Not used for other bit patterns

Table 5. Reference Divider Ratio

| RSA | RSB | REFERENCE DIVIDER RATIO |
|-----|-----|-------------------------|
| X | 0 | 640 |
| 0 | 1 | 1024 |
| 1 | 1 | 512 |

Example of I²C Data-Write Sequences

Telegram Examples

Start – ADB – DB1 – DB2 – CB – BB – Stop

Start – ADB – DB1 – DB2 – Stop

Start – ADB – CB – BB – Stop

Abbreviations

ADB: Address byte

DB1: Divider byte 1

DB2: Divider byte 2

CB: Control byte

BB: Band-switch byte

Start: Start condition

Stop: Stop condition

Note: Following bytes after band-switch byte (BB) are ignored.

Start – ADB – DB1 – DB2 – CB – BB – (ignored) – (ignored) – Stop

Start – ADB – CB – BB – (ignored) – (ignored) – Stop

I²C Read Mode (R/W = 1)

Table 6. Read Data Format

| | MSB | | | | | | | LSB | |
|--------------------|-----|----|---|---|---|---|-----|-----|---------|
| Address byte (ADB) | 1 | 1 | 0 | 0 | 0 | 0 | MA1 | MA0 | R/W = 1 |
| Status byte (SB) | POR | FL | 1 | 1 | 1 | 1 | A2 | A1 | A0 |

(1) Acknowledge

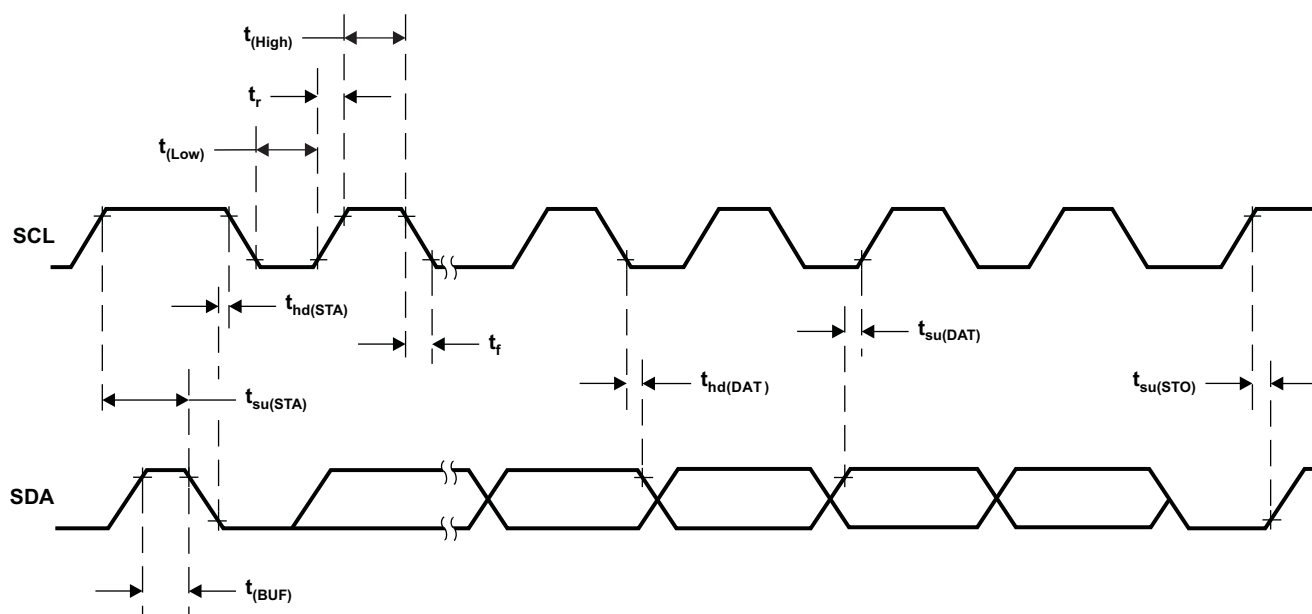
Table 7. I²C Read-Mode Data-Symbol Description

| SYMBOL | DESCRIPTION | DEFAULT |
|----------|---|---------|
| MA1, MA0 | Address set bits (see Table 3) | |
| POR | Power-on reset flag bit POR set: Power on POR reset: End-of-data transmission procedure | POR = 1 |
| FL | In-lock flag bit PLL locked (FL = 1) PLL unlocked (FL = 0) | |
| A2–A0 | Digital data bits of ADC (see Table 8) | |

Table 8. ADC Level

| A2 | A1 | A0 | VOLTAGE APPLIED ON ADC INPUT ⁽¹⁾ |
|----|----|----|---|
| 1 | 0 | 0 | 0.6 V _{CC} to V _{CC} |
| 0 | 1 | 1 | 0.45 V _{CC} to 0.6 V _{CC} |
| 0 | 1 | 0 | 0.3 V _{CC} to 0.45 V _{CC} |
| 0 | 0 | 1 | 0.15 V _{CC} to 0.3 V _{CC} |
| 0 | 0 | 0 | 0 to 0.15 V _{CC} |

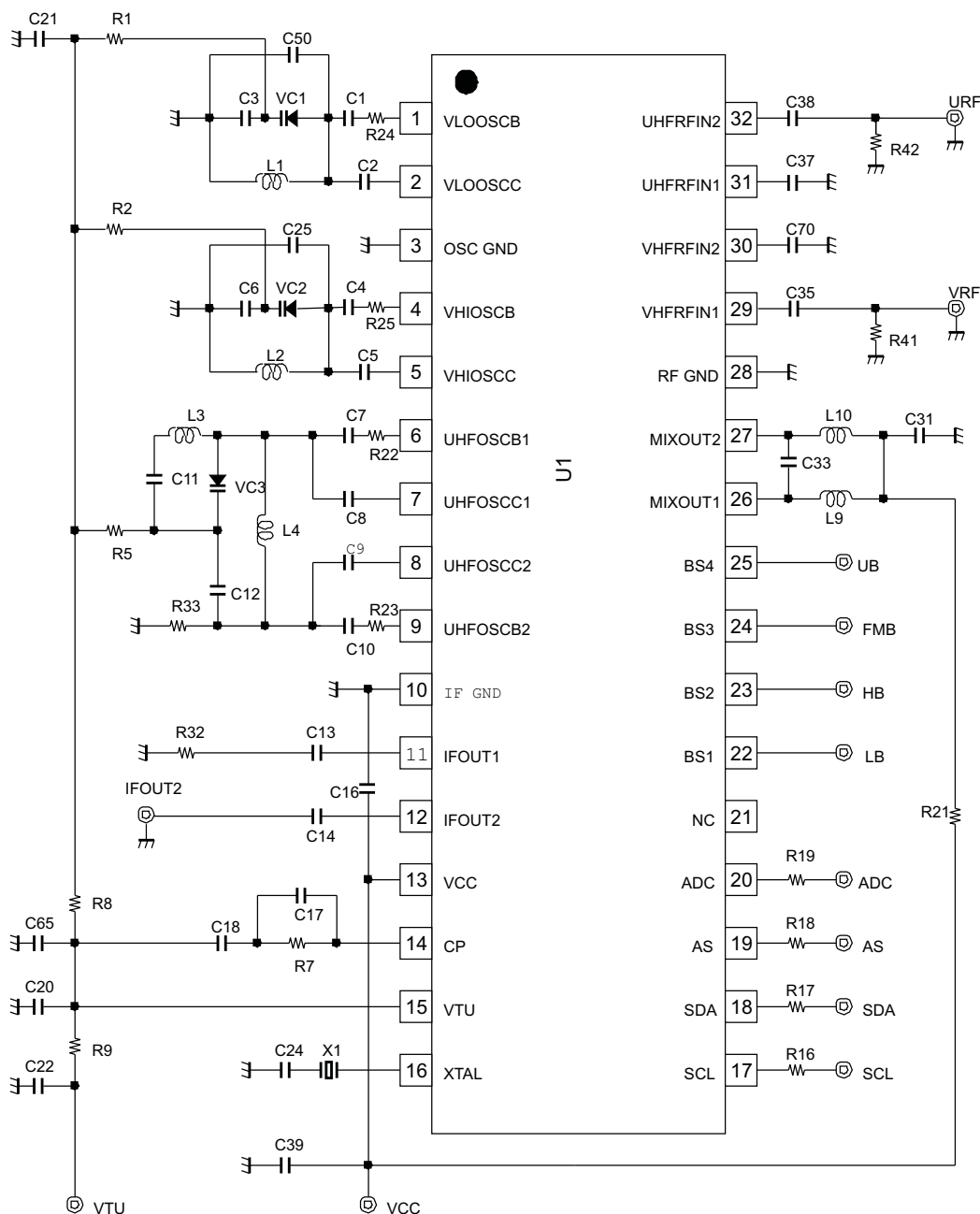
(1) Accuracy is $0.03 \times V_{CC}$.



T0101-01

Figure 16. I²C Timing Chart

APPLICATION INFORMATION



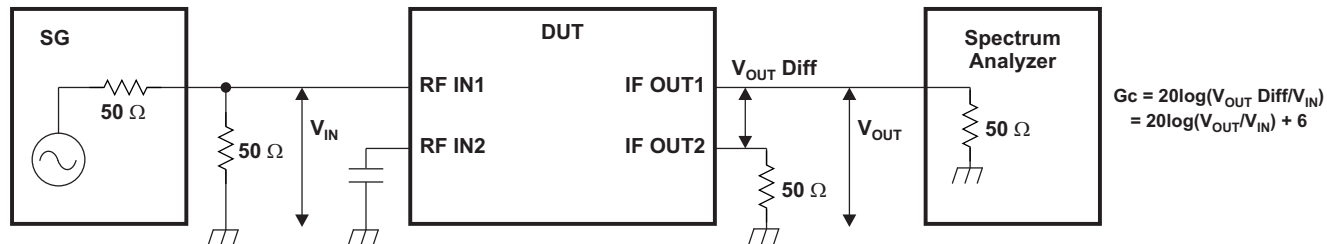
NOTE: This application information is advisory, and a performance check is required for actual application circuits. TI assumes no responsibility for the consequences of use of this circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

Figure 17. Reference Measurement Circuit

Table 9. Component Values for Measurement Circuit

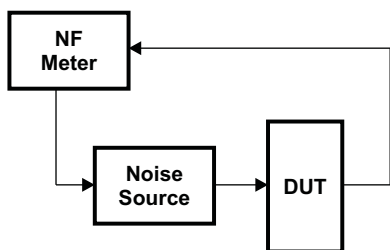
| PART NAME | VALUE | PART NAME | VALUE |
|-----------|-------|-----------|------------------------|
| C1 | 1p | L1 | φ3mm, 8T, wire 0.32mm |
| C2 | 1p | L2 | φ2.4mm, 4T, wire 0.4mm |
| C3 | 47p | L3 | φ3mm, 2T, wire 0.4mm |
| C4 | 2p | L4 | φ2mm, 3T, wire 0.4mm |
| C5 | 3p | L9 | φ3mm, 15T, wire 0.25mm |
| C6 | 68p | L10 | φ3mm, 15T, wire 0.25mm |
| C7 | 1.5p | R1 | 33k |
| C8 | 1p | R2 | 33k |
| C9 | 1p | R5 | 22k |
| C10 | 1.5p | R7 | 22k |
| C11 | 100p | R8 | 33k |
| C12 | 12p | R9 | 22k |
| C13 | 2.2n | R16 | 330 |
| C14 | 2.2n | R17 | 330 |
| C16 | 4.7n | R18 | 330 |
| C17 | 2.2n | R19 | 330 |
| C18 | 0.1u | R21 | 0 |
| C20 | 2.2n | R22 | 20 |
| C21 | 2.2n | R23 | 20 |
| C22 | 2.2n | R24 | 20 |
| C24 | 68p | R25 | 20 |
| C25 | open | R32 | 51 |
| C31 | 4.7n | R33 | 22k |
| C33 | 22p | R41 | 51 |
| C35 | 2.2n | R42 | 51 |
| C37 | 2.2n | U1 | SN761683B |
| C38 | 2.2n | VC1 | 1T363A |
| C39 | 4.7n | VC2 | 1T363A |
| C50 | 3p | VC3 | 1T363A |
| C65 | 2.2n | X1 | Crystal 4 MHz |
| C70 | 2.2n | | |

TEST CIRCUITS



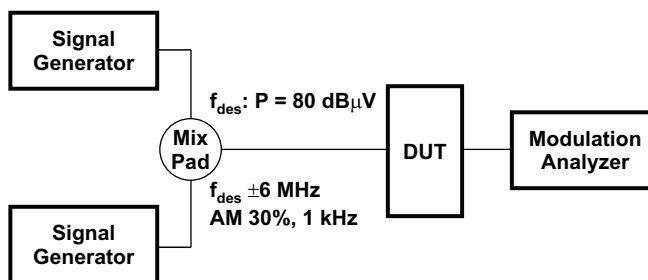
S0145-01

Figure 18. Conversion Gain-Measurement Circuit



B0090-01

Figure 19. Noise-Figure Measurement Circuit



B0091-01

Figure 20. 1% Cross-Modulation Distortion Measurement Circuit

TYPICAL CHARACTERISTICS

Band-Switch Driver Output Voltage (BS1–BS4)

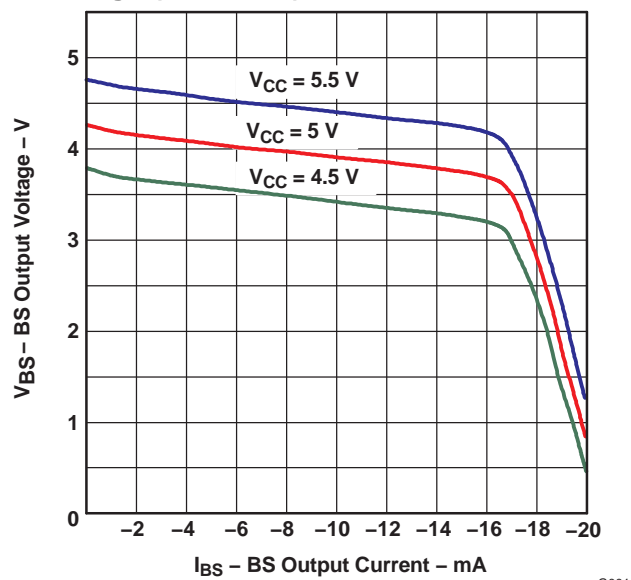


Figure 21. BS Output Current vs Output Voltage

S-Parameter

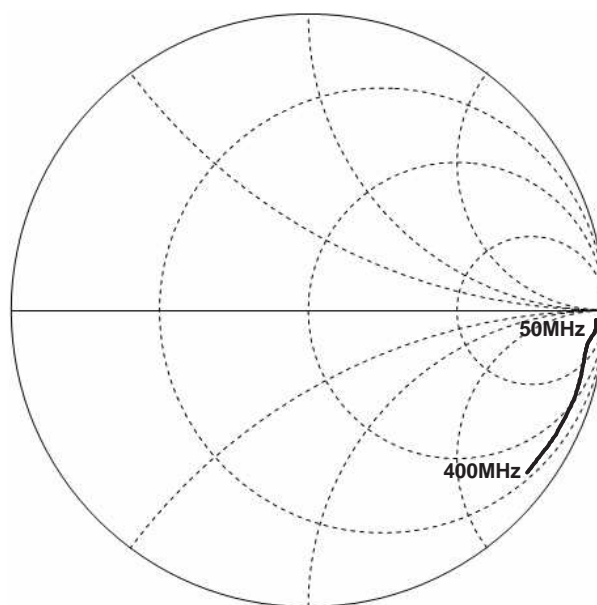


Figure 22. VHF Input

TYPICAL CHARACTERISTICS (continued)

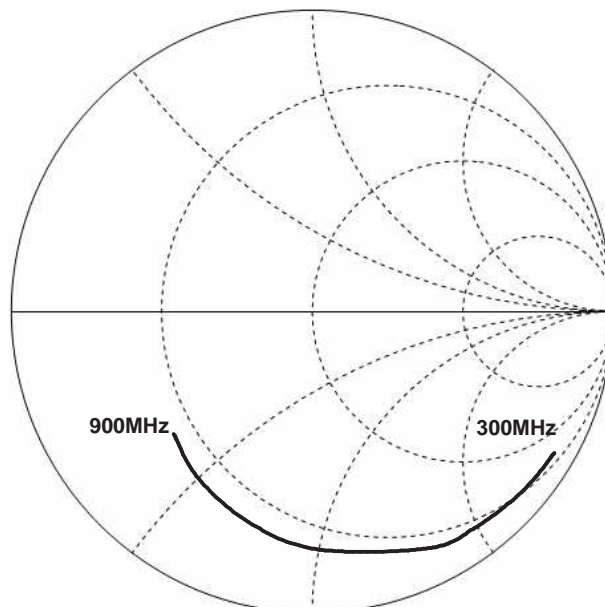


Figure 23. UHF Input

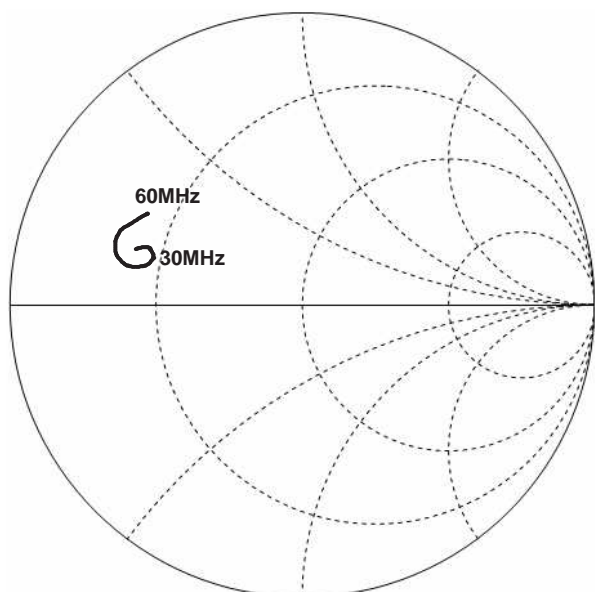


Figure 24. IF Output

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------|---------|
| SN761683BDA | OBSOLETE | TSSOP | DA | 32 | | TBD | Call TI | Call TI | -20 to 85 | | |
| SN761683BDAG4 | OBSOLETE | TSSOP | DA | 32 | | TBD | Call TI | Call TI | -20 to 85 | | |
| SN761683BDAR | OBSOLETE | TSSOP | DA | 32 | | TBD | Call TI | Call TI | -20 to 85 | SN761683B | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

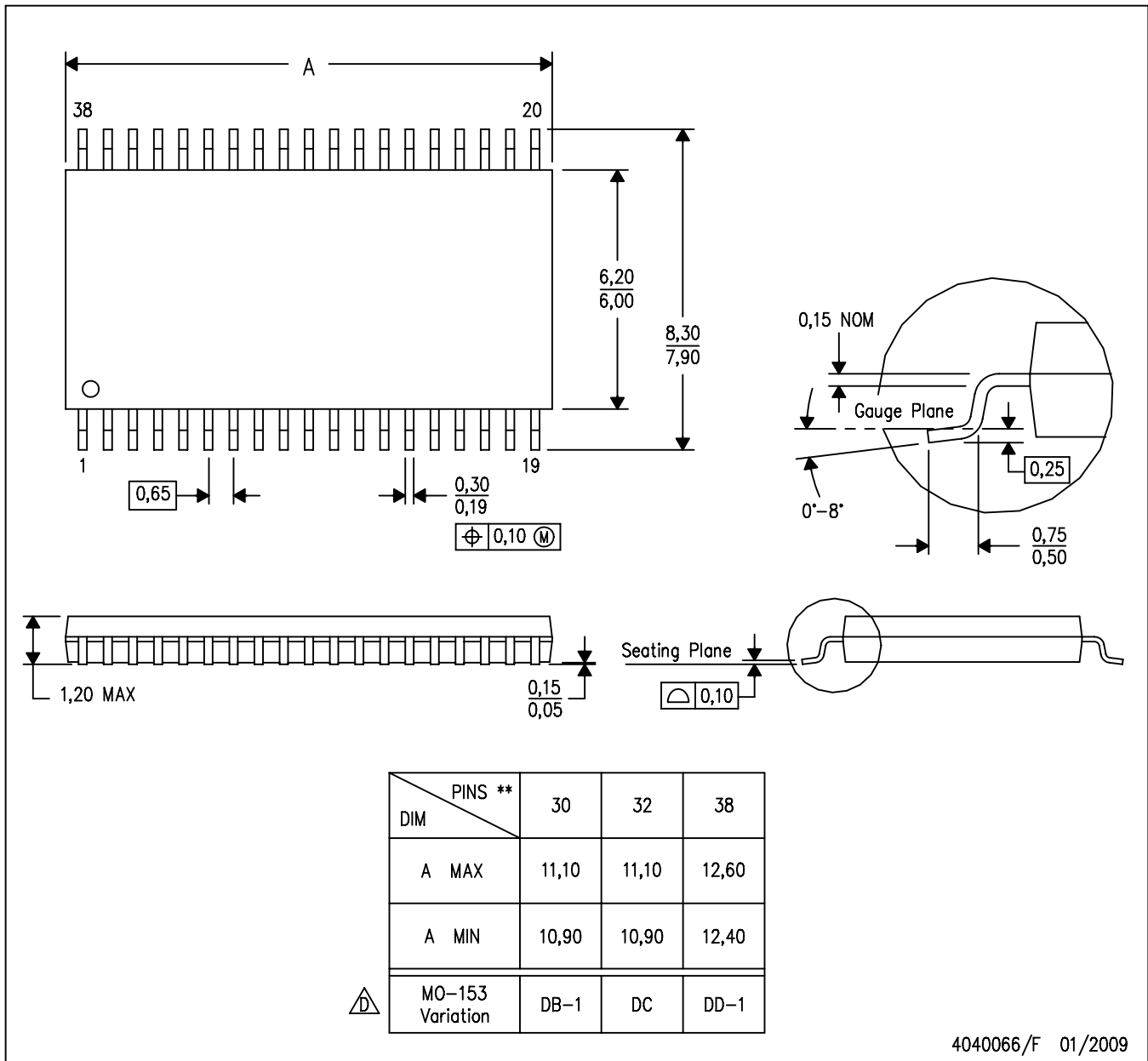
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DA (R-PDSO-G**)

38 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-153, except 30 pin body length.

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