DRV8308 Brushless DC Motor Controller

1 Features

- Three-Phase Brushless DC Motor Controller
  - Fully Digital Speed Loop With Programmable Gain and Loop Filters
  - Clock Input or PWM Inputs for Speed Control
- Operating Supply Voltage 8.5 to 32 V
- Drives 10- to 130-mA Gate-Drive Current to 6 N-Channel MOSFETs With Adjustable Slew Rates
- Supports Sensor-based Sinusoidal and Trapezoidal Commutation Control With Tunable Delay
- Flexible Configuration Methods:
  - Serial Control
  - Internal OTP Memory
  - External EEPROM
- 5-V Linear Regulator and Switched Power Output for Hall Sensors
- SPI Control Interface
- Low-power Standby Mode
- Locked Rotor Detection and Restart
- Integrated Overcurrent, Overvoltage, and Overtemperature Protection
- 6- × 6-mm QFN Package, 0.5-mm Pitch

2 Applications

- Pumps and Industrial Equipment
- Currency Counters
- Printers

3 Description

The DRV8308 device is a three half-bridge pre-driver that drives up to 130 mA to six N-type MOSFETs with a single power supply. Aimed at sensored three-phase brushless DC motors, this pre-driver includes configurable a digital speed loop, speed controls, and commutation modes to optimize motor performance. When properly tuned, the DRV8308 device can drive motors with less than 0.1% cycle jitter and fast torque compensation.

The integrated digital speed loop allows the motor to maintain speed under variable loads with programmable gain and loop filters. The adjustable slew rates can also lower the switching noise and improve EMC.

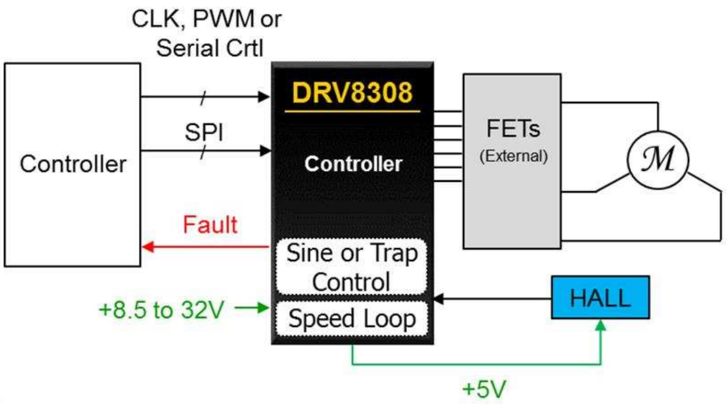
The DRV8308 device also supports both the 120° and 180° commutation modes with the ability to adjust the delay to increase power efficiency. For high-performance systems, sinusoidal (180°) commutation mode is used to minimize acoustic noise and torque ripple. Jitter caused by non-ideal Hall placement and matching can be eliminated once constant speed is reached by switching from three Hall sensor phases to just a single Hall sensor.

In addition to advanced programmability features to tune the motor’s performance, the SPI interface also provides detailed fault reporting such as locked rotor detection, overcurrent, overtemperature, and overvoltage, as well as charge pump short and failure, to provide robust protection and intelligence to the overall system design.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
DRV8308RHAR	RHA (40)	6 mm × 6 mm
DRV8308RHAT	RHA (40)	6 mm × 6 mm

4 Simplified Schematic



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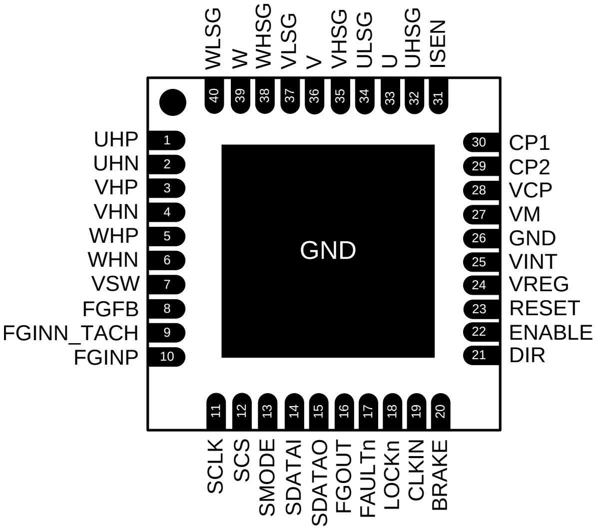
5 Revision History

Date	Revision	Notes
February 2014	*	Initial Release

6 Terminal Configurations and Functions

40 RHA (QFN) PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NUMBER			
POWER AND GROUND				
CP1	30	I/O	Charge pump flying capacitor	Connect a 0.1-μF 35-V capacitor between CP1 and CP2
CP2	29	I/O		
GND	26, PPAD	I	Ground reference. Terminal 26 and the Power Pad are internally connected.	Connect to board GND
VCP	28	I/O	Charge pump storage capacitor	Connect a 1-μF 35-V ceramic capacitor to VM
VINT	25	I/O	Internal 1.8-V core voltage regulator bypass	Bypass to GND with a 1-μF 6.3-V ceramic capacitor
VM	27	I	Motor supply voltage	Connect to motor supply voltage. Bypass to GND with a 0.1-μF ceramic capacitor, plus a large electrolytic capacitor (47 μF or larger is recommended), with a voltage rating of 1.5× to 2.5× VM.
VREG	24	I/O	5-V regulator output. Active when ENABLE is active.	Bypass to GND with a 0.1-μF 10-V ceramic capacitor. Can provide 5-V power to Hall sensors.
VSW	7	O	Switched VM power output. When ENABLE is active, VM is applied to this terminal.	Can be used for powering Hall elements, along with added series resistance.
CONTROL				
BRAKE	20	I	Causes motor to brake. Polarity is programmable. Internal pulldown resistor.	
CLKIN	19	I	The clock input, used in Clock Frequency mode and Clock PWM mode. Internal pulldown resistor.	
DIR	21	I	Sets motor rotation direction. Polarity is programmable. Internal pulldown resistor.	
ENABLE	22	I	Enables and disables motor. Polarity is programmable. Internal pulldown resistor.	

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(1) I = input, O = output, OD = open-drain output, I/O = input/output

Terminal Functions (continued)

TERMINAL		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NUMBER			
FAULTn	17	OD	Fault indicator – active low when overcurrent, overtemperature, or rotor stall detected. Open-drain output.	
FGOUT	16	OD	Outputs a TACH signal generated from the FG amplifier or Hall sensors. Open-drain output.	
LOCKn	18	OD	Outputs a signal that indicates the speed loop is locked. Open-drain output.	
RESET	23	I	Active high to reset all internal logic. Internal pulldown resistor.	
SERIAL INTERFACE				
SCLK[2]	11	I/OD	Serial clock	SPI mode: Serial clock input. Data is clocked on rising edges. Internal pulldown resistor. EEPROM mode: Connect to EEPROM CLK. Open-drain output requires external pullup.
SCS[2]	12	I/OD	Serial chip select	SPI mode: Active high enables serial interface operation. Internal pulldown resistor. EEPROM mode: Connect to EEPROM CS. Open-drain output requires external pullup.
SDATAI	14	I	Serial data input	SPI mode: Serial data input. Internal pulldown resistor. EEPROM mode: Serial data input. Connect to EEPROM DO terminal.
SDATAO	15	OD	Serial data output	SPI mode: Serial data output. Open-drain output. EEPROM mode: Connect to EEPROM DI. Open-drain output requires external pullup.
SMODE	13	I	Serial mode	SPI mode: leave open or connect to ground for SPI interface mode. EEPROM mode: Connect to logic high to for EEPROM mode.
POWER STAGE INTERFACE				
ISEN	31	I	Low-side current sense resistor	Connect to low-side current sense resistor
U	33	I	Measures motor phase voltages for V_{FETOCP}	Connect to motor windings
V	36	I		
W	39	I		
UHSG	32	O	High-side FET gate outputs	Connect to high-side 1/2-H N-channel FET gate
VHSG	35	O		
WHSG	38	O		
ULSG	34	O	Low-side FET gate outputs	Connect to low-side 1/2-H N-channel FET gate
VLSG	37	O		
WLSG	40	O		
HALL AND FG INTERFACE				
FGFB	8	O	FG amplifier feedback terminal	Connect feedback network to FGIN–
FGINN_TACH	9	I[3]	FG amplifier negative input or TACH input	Connect to FG trace and filter components. When using a TACH with FGSEL= 3, connect a logic-level TACH signal. If unused, connect FGFB to FG–.
FGINP	10	I/O	FG amplifier positive input	Connect to FG trace and filter components on the PCB (if used).

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(2) In SPI mode, these terminals are inputs; in EEPROM mode, they are open-drain outputs.
(3) When using FG amp, this terminal is an analog input. If in TACH mode, this is a logic-level input.

Terminal Functions (continued)

TERMINAL		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NUMBER			
UHP	1	I	Hall sensor U positive input	Connect to Hall sensors. Noise filter capacitors may be desirable, connected between the + and – Hall inputs.
UHN	2	I	Hall sensor U negative input	
VHP	3	I	Hall sensor V positive input	
VHN	4	I	Hall sensor V negative input	
WHP	5	I	Hall sensor W positive input	
WHN	6	I	Hall sensor W negative input	

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)(2)(3)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	35	V
Charge pump and high side gate drivers (VCP, UHSG, VHSG, WHSG)	–0.3	50	V
Output terminal, low side gate drivers, charge pump flying cap and switched VM power supply voltage (U, V, W, ULSG, VLSG, WLSG, CP1, CP2 VSW)	–0.6	40	V
Internal core voltage regulator (VINT)	–0.3	2.0	V
Linear voltage regulator output (VREG)	–0.3	5.5	V
Sense current terminal (ISEN)	–0.3	2.0	V
Digital terminal voltage range (SCLK, SCS, SMODE, SDATAI, SDATAO, FGOUT, FAULTn, LOCKn, CLKIN, BRAKE, DIR, ENABLE, RESET)	–0.5	5.75	V
Hall sensor input terminal voltage (UHP, UHN, VHP, VHN, WHP, WHN, FGFB, FGINN/TACH, FGINP)	0	VREG	V
Continuous total power dissipation	See Thermal Information		
Operating junction temperature range, T_J	–40	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed

7.2 Handling Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{stg}	Storage temperature range	–60	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range, ENABLE = 1, motor operating (1)		8.5		32	V
V_{MDIS}	Motor power supply voltage range, ENABLE = 0, motor not operating		4.5		35	
I_{VREG}	VREG output current (2)		0		30	mA
I_{VSW}	VSW output current (2)		0		30	
f_{HALL}	Hall sensor input frequency (3)		0		30	kHz
f_{CLKIN}	Frequency on CLKIN	SPDMODE = 00 (Clock frequency mode)	0		90	
		SPDMODE = 01 (Clock PWM mode)	16		50 (4)	

(1) Note that at VM < 12 V, gate drive output voltage tracks VM voltage
(2) Power dissipation and thermal limits must be observed
(3) f_{HALL} of 50 Hz to 6.7 kHz is best
(4) Operational with frequencies above 50 kHz, but resolution is degraded

7.4 Thermal Information

THERMAL METRIC[1]		DRV8308	UNIT
		RHA (40 TERMINALS)	
θ_{JA}	Junction-to-ambient thermal resistance[2]	32.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	24.5	
θ_{JB}	Junction-to-board thermal resistance[4]	9.9	
ψ_{JT}	Junction-to-top characterization parameter[5]	2.7	
ψ_{JB}	Junction-to-board characterization parameter[6]	10.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	2.7	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VM SUPPLY						
I_{VM}	VM active current	ENABLE = active, VREG and VSW open		12	18	mA
I_{STBY}	VM standby current	ENABLE = inactive			120	µA
V_{RESET}	VM logic reset voltage	VM falling			4.6	V
		VM rising	5.0			
VREG SUPPLY						
V_{VREG}	Output voltage	I_{OUT} = 1 to 30 mA	4.75	5	5.25	V
I_{VREG}	Output current				30	mA
VSW SUPPLY						
$R_{DS(ON)}$	VSW switch on-resistance	I_{OUT} = 1 to 30 mA		9	20	Ω
I_{VSW}	Output current				30	mA
INTERNAL CLOCK OSCILLATOR						
f_{CLK50}	Internal CLK50 clock frequency			50		MHz
LOGIC-LEVEL INPUTS AND OUTPUTS						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		1.5		5.5	V
I_{IL}	Low-level input current		–50		50	µA
I_{IH}	High-level input current	V_{IN} = 3.3 V, RESET, DIR, BRAKE, CLKIN, SCS, SCLK, SDATAI, SMODE	20		100	µA
		V_{IN} = 3.3 V, ENABLE	6		9	
V_{HYS}	Input hysteresis voltage		0.1	0.3	0.5	V
R_{PD}	Input pulldown resistance	RESET, DIR, BRAKE, CLKIN, SCS, SCLK, SDATAI, SMODE	50	100	150	kΩ
		ENABLE	350		550	
OPEN DRAIN OUTPUTS						
V_{OL}	Low-level output voltage	I_{OUT} = 2.0 mA			0.5	V
I_{OH}	Output leakage current	V_{OUT} = 3.3 V			1	µA
FG AMPLIFIER AND COMPARATOR						
V_{IO}	FG amplifier input offset voltage		–7		7	mV
I_{IB}	FG amplifier input bias current		–1		1	µA
V_{ICM}	FG amplifier input common mode voltage range		1.5		3.5	V
A_V	FG amplifier open loop voltage gain		45			dB
GBW	FG amplifier gain bandwidth product		500			kHz
V_{REF+}	FG comparator positive reference voltage		–20%	V_{VREG} / 2	20%	V
V_{IT+}	FG comparator positive threshold		–20%	V_{VREG} / 1.8	20%	V
V_{IT-}	FG comparator negative threshold		–20%	V_{VREG} / 2	20%	V
HALL SENSOR INPUTS						
V_{HYS}	Hall amplifier hysteresis voltage		15	20	25	mV
ΔV_{HYS}	Hall amplifier hysteresis difference	Between U, V, W	–5		5	mV
V_{ID}	Hall amplifier input differential		50			mV
V_{CM}	Hall amplifier input common mode voltage range		1.5		3.5	V
I_{IN}	Input leakage current	H_x+ = H_x-	–10		10	µA
t_{HDEG}	Hall deglitch time			20		µs
MOSFET DRIVERS						

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUTH}	High-side gate drive output voltage	I_O = 100 μA, VM ≥ 12V		VM + 10		V
V_{OUTL}	Low-side gate drive output voltage	I_O = 100 μA		10		V
I_{OUT}	Peak gate drive current	IDRIVE = 000		10		mA
		IDRIVE = 001		20		
		IDRIVE = 010		30		
		IDRIVE = 011		50		
		IDRIVE = 100		90		
		IDRIVE = 101		100		
		IDRIVE = 110		110		
		IDRIVE = 111		130		
CYCLE-BY-CYCLE CURRENT LIMITER						
$V_{LIMITER}$	Voltage limit across R_{ISENSE} for the current limiter		0.225	0.25	0.275	V
t_{BLANK}	Time that $V_{LIMITER}$ is ignored, from the start of the PWM cycle	OCPDEG = 00		2.0		µs
		OCPDEG = 01		3.0		
		OCPDEG = 10		3.75		
		OCPDEG = 11		6		
PROTECTION CIRCUITS						
$V_{SENSEOCP}$	Voltage limit across R_{ISENSE} for overcurrent protection		1.7	1.8	1.9	V
$t_{SENSEOCP}$	Deglitch time for $V_{SENSEOCP}$ to trigger	OCPDEG = 00		1.6		µs
		OCPDEG = 01		2.3		
		OCPDEG = 10		3		
		OCPDEG = 11		5		
V_{FETOCP}	Voltage limit across each external FET’s drain to source for overcurrent protection	OCPTH = 00	200	250	400	mV
		OCPTH = 01	400	500	600	
		OCPTH = 10	600	750	850	
		OCPTH = 11	850	1000	1200	
t_{FETOCP}	Deglitch time for V_{FETOCP} to trigger	OCPDEG = 00		1.6		µs
		OCPDEG = 01		2.26		
		OCPDEG = 10		3		
		OCPDEG = 11		5		
V_{UVLO}	VM undervoltage lockout	VM rising		8		V
		VM falling		7.8		
V_{OVLO}	VM overvoltage lockout	VM rising, OVTH = 0	32	34	36	V
		VM rising, OVTH = 1			29	
t_{RETRY}	Fault retry time after RLOCK or OTS	RETRY = 1		5		s
T_{TSD}	Thermal shutdown die temperature		150	160		°C
t_{LOCK}	Locked rotor detect time	LRTIME = 00		1		s
		LRTIME = 01		3		
		LRTIME = 10		5		
		LRTIME = 11		10		
V_{CPFAIL}	VCP failure threshold (CPFAIL bit)			VM + 3.0		V

7.6 SPI Timing Requirements

T_A = 25°C, over recommended operating conditions unless otherwise noted

NUMBER[1]	PARAMETER	TEST CONDITIONS[2]	MIN	MAX	UNIT
1	t_{CYC}	Clock cycle time	62		ns
2	t_{CLKH}	Clock high time	25		
3	t_{CLKL}	Clock low time	25		
4	$t_{SU(SDATI)}$	Setup time, SDATI to SCLK	5		
5	$t_{H(SDATI)}$	Hold time, SDATI to SCLK	1		
6	$t_{SU(SCS)}$	Setup time, SCS to SCLK	5		
7	$t_{H(SCS)}$	Hold time, SCS to SCLK	1		
8	$t_{L(SCS)}$	Inactive time, SCS (between writes)	100		
9	$t_{D(SDATO)}$	Delay time, SCLK to SDATO (during read)		10	
	t_{AWAKE}	Wake time (ENABLE active to high-side gate drive enabled)		1	ms
	t_{SPI}	Delay from power-up or RESET low until serial interface functional		10	μs

(1) These numbers refer to the corresponding number in Figure 1
(2) SMODE = Low

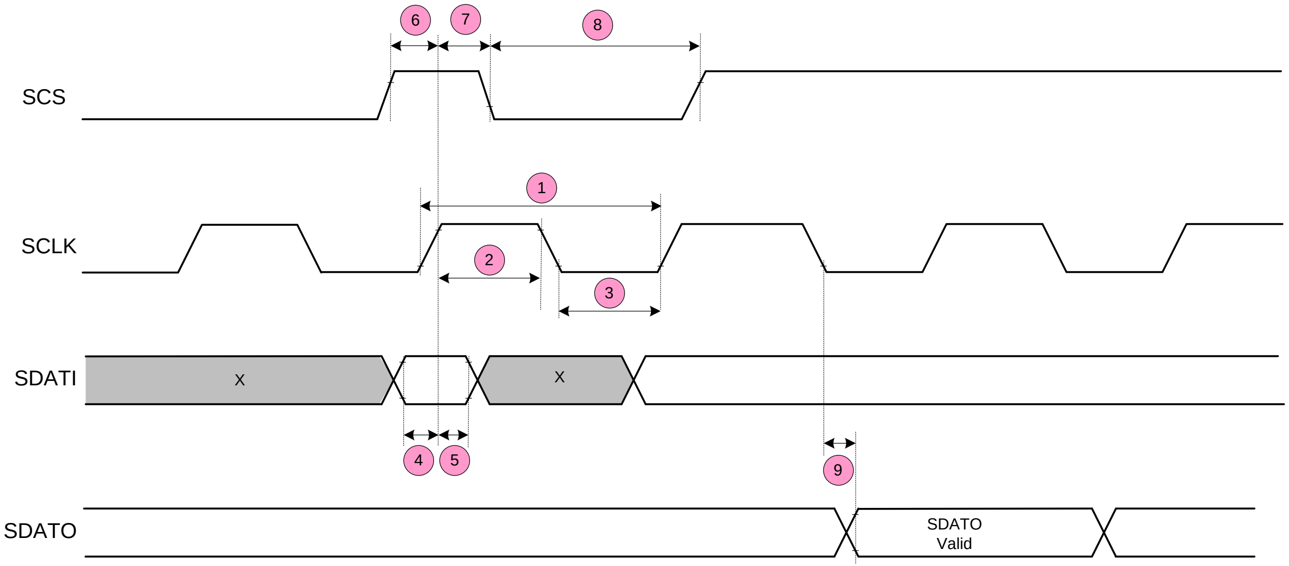


Figure 1. SPI Timing Requirements

8 Detailed Description

8.1 Overview

The DRV8308 device controls 3-phase brushless DC motors using a speed and direction input interface and Hall signals from the motor. The device drives N-channel MOSFETs with 10-V V_{GS}, and a configurable gate drive current of 10 to 130 mA.

There are three modes of speed input: clock frequency, clock duty cycle (pulse-width modulation), and an internal register that specifies duty cycle. In the clock frequency mode, the device's digital speed control system matches motor speed with the input clock's frequency. Motor speed is either determined from the Halls sensors or signal on the FG input, which can be generated from a board trace underneath the motor that senses magnetic reluctance. The speed control system offers digital tuning of pole and zero frequencies and integrator gain. When properly tuned, the DRV8308 can drive motors with < 0.1% cycle jitter and fast torque compensation for varying loads. The duty cycle speed modes operate in open-loop without speed control.

When the DRV8308 device powers up, the configuration registers are set from either the one-time programmable (OTP) non-volatile memory, or from an external EEPROM (depending on the SMODE terminal). After power-up, registers can be set in realtime over SPI, and the OTP memory can be permanently written once.

When the DRV8308 device begins spinning a motor, it initially uses all three Hall sensor phases to commutate. After a constant speed is reached, the LOCKn terminal is pulled low and only one Hall sensor becomes used; this feature reduces jitter by eliminating the error caused by non-ideal Hall device placement and matching. Also at this time, commutation transitions to sine wave current drive (if enabled), which minimizes acoustic noise and torque ripple. Commutation timing can be tuned using the ADVANCE register for optimal performance and power efficiency.

Numerous protection circuits prevent system components from being damaged during adverse conditions. Monitored aspects include motor voltage and current, gate drive voltage and current, device temperature, and rotor lockup. When a fault occurs, the DRV8308 device stops driving and pulls FAULTn low, in order to prevent FET damage and motor overheating.

The DRV8308 device is packaged in a compact 6 × 6-mm, 40-terminal QFN with a 0.5-mm terminal pitch, and operates through an industrial ambient temperature range of –40°C to 85°C.

8.2 Functional Block Diagram

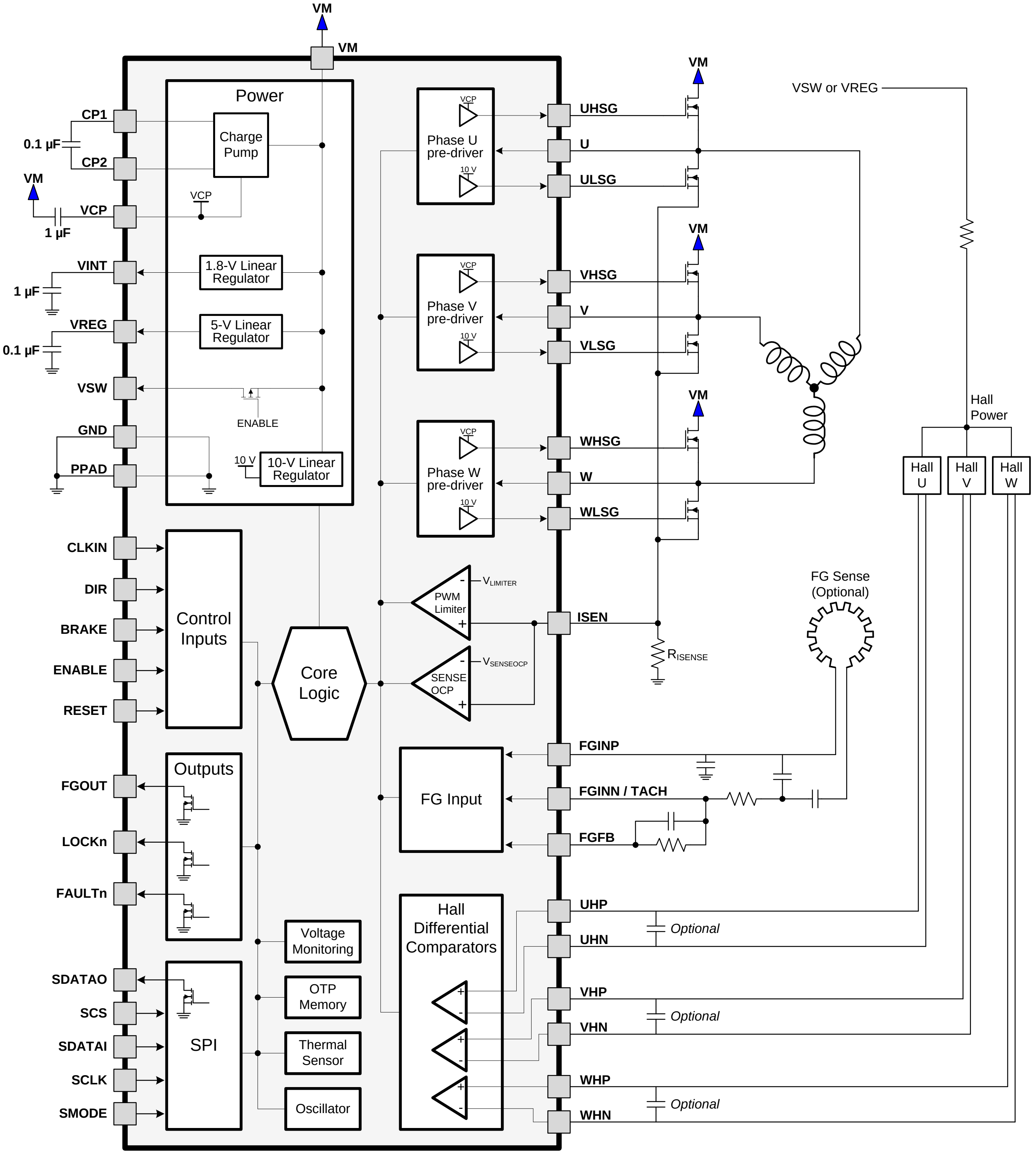


Figure 2.

8.3 Feature Description

8.3.1 Hall Comparators

Three comparators are provided to process the raw signals from Hall effect transducers to commutate the motor. The Hall amplifiers sense zero crossings of the differential inputs and pass the information to digital logic.

The Hall amplifiers have hysteresis, and their detect threshold is centered at 0. Note, hysteresis is defined as shown in Figure 3:

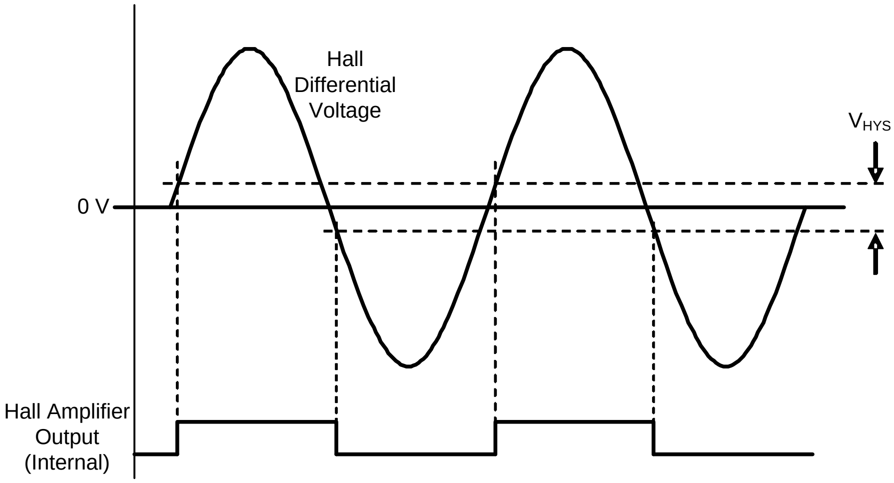


Figure 3. Hall Amplifier Hysteresis

In addition to the hysteresis, the Hall inputs are deglitched with a circuit that ignores any extra Hall transitions for a period of 20 µs after sensing a valid transition. This prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

If excessive noise is still coupled into the Hall comparator inputs, it may be necessary to add capacitors between the + and – inputs of the Hall comparators, and (or) between the input or inputs and ground.

The ESD protection circuitry on the Hall inputs implements a diode to VREG. Because of this diode, the voltage on the Hall inputs should not exceed the VREG voltage.

Since VREG is disabled in standby mode (ENABLE inactive), the Hall inputs should not be driven by external voltages in standby mode. If the Hall sensors are powered from VREG or from VSW, this is specified by the DRV8308 device; however, if the Hall sensors are powered externally, they should be disabled if the DRV8308 is put into standby mode. In addition, they should be powered-up before enabling the motor, or an invalid Hall state may cause a delay in motor operation.

8.3.2 FG Amplifier, Comparator, and FG Output

An FG amplifier and comparator provide rotational feedback from an external magnetic reluctance sensor. A diagram of the FG circuit is shown in Figure 4:

Feature Description (continued)

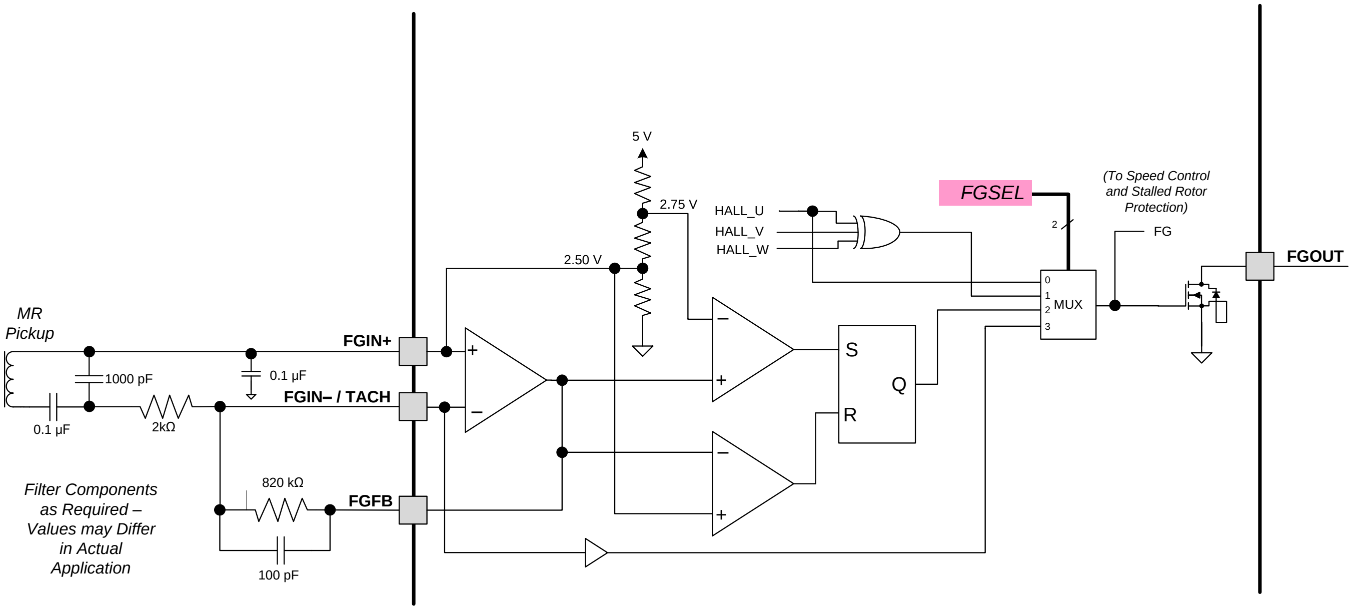


Figure 4. FG Circuit Diagram

The output of the FG amplifier is provided on a terminal, so the gain of the FG amplifier can be set by the user. Filter circuits can also be implemented.

Note that the FG signal is also fed back internally to the speed control circuits.

The FG signal that the DRV8308 device uses can be generated from a PCB trace under a motor, or it can be input from a logic-level TACH input, or it can be synthesized from the Hall sensor transitions (selectable by register FGSEL). If generated from Hall transitions, the resulting output can be either an exclusive-or function of the three Hall sensors, or the same as the HALL_U input, as shown in Figure 5.

Selection of FG operating mode is through the FGSEL register bits.

The FGOUT terminal is an open-drain output and requires an external pullup resistor to the logic supply.

Feature Description (continued)

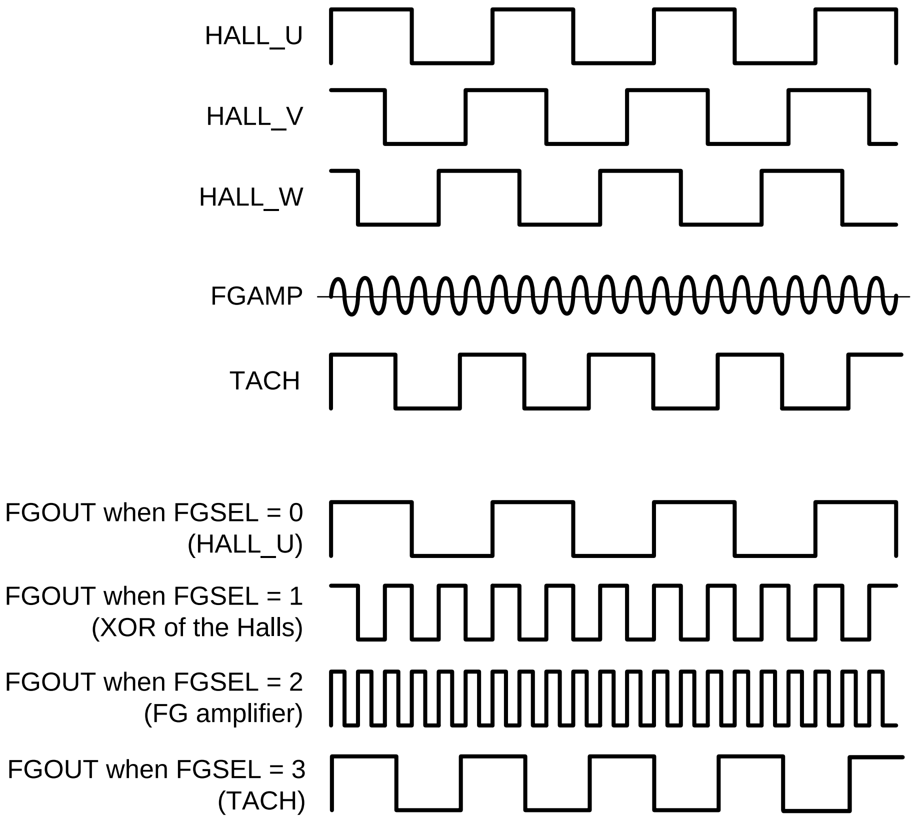


Figure 5.

8.3.3 Enable, Reset, and Clock Generation

The ENABLE terminal is used to start and stop motor operation. ENABLE can be programmed to be active high or active low, depending on the state of the ENPOL bit; if ENPOL = 0, ENABLE is active high. If ENPOL = 1, the ENABLE terminal is active low.

The polarity of ENABLE cannot be modified during operation through register writes; it is controlled only by the contents of the ENPOL bit in OTP memory.

When ENABLE is active, operation of the motor is enabled. When ENABLE is made inactive, the speed control loop is reset, and the motor either brakes or coasts depending on the state of the BRKMOD bit. After motor rotation has stopped (when no transitions occur on the FGOUT terminal for a period of 1 s), the DRV8308 device enters a low-power standby state. In the standby state, the motor driver circuitry is disabled (all gate drive outputs are driven low, so the FET outputs are high-impedance), the gate drive regulator and charge pump are disabled, the VREG regulator and VSW power switch are disabled, and all analog circuitry is placed into a low power state. The digital circuitry in the device still operates in standby mode.

All internal logic is reset in three different ways:

1. Upon device power-up.
2. When VM drops below V_{RESET}.
3. When the RESET terminal is high while ENABLE is active.

If RESET is high while ENABLE is inactive, then the registers read as 1. If the RESET terminal is not needed, it can be connected to GND. The RESET input is deglitched with a 10-µs timer on assertion and deassertion.

An internal clock generator provides all timing for the DRV8308 device. The master oscillator runs at 100 MHz. This clock is divided to a nominal 50-MHz frequency that clocks the remainder of the digital logic.

Feature Description (continued)

8.3.4 Commutation

For 3-phase brushless DC motors, rotor position feedback is provided from Hall effect transducers mounted on the motor. These transducers provide three overlapping signals, each 60° apart. The windings are energized in accordance with the signals from the Hall sensors to cause the motor to move.

In addition to the Hall sensor inputs, commutation is affected by a direction control, which alters the direction of motion by reversing the commutation sequence. Control of commutation direction is by the DIRPOL register bit as well as the DIR input terminal. The DIRPOL register bit is combined with the terminal with an exclusive-OR function as follows:

Table 1. Direction Behavior

DIR Terminal	DIRPOL Register Bit	Resulting DIR for Commutation
0	0	0
0	1	1
1	0	1
1	1	0

If the commanded direction is changed while the motor is moving, the device either brakes or allows the motor to coast, depending on the state of the BRKMODE bit, until the motor stops. The stopped condition is determined by measuring the period of the HALL_U signal; when the period exceeds 160 ms, typical operation resumes and the motor starts spinning in the commanded direction. This prevents excessive current flow in the output stage if the motor is reversed while running at speed.

The DRV8308 device supports three commutation modes: standard 120° commutation using three Hall sensors, 120° commutation using a single Hall sensor, and 180° sine-wave-drive commutation.

In standard 120° commutation, mis-positioning of the Hall sensors can cause motor noise, vibration, and torque ripple. 120° commutation using a single Hall sensor (single-Hall commutation) can improve motor torque ripple and vibration because it relies on only one Hall edge for timing.

180° sine-wave-drive commutation is even more advanced, and excites the windings with a waveform that delivers nearly sinusoidal current to each winding.

8.3.4.1 120° 3-Hall Commutation

In standard 120° commutation, the motor phases are energized using simple combination logic based on all three Hall sensor inputs.

Standard 120° commutation is in accordance with Table 2, Figure 6, and Figure 7:

Table 2. Standard 120° Commutation (1)

STATE	HALL INPUTS						PRE-DRIVE OUTPUTS					
	DIR = 1			DIR = 0			Phase U		Phase V		Phase W	
	U_H	V_H	W_H	U_H	V_H	W_H	U_HSGATE	U_LSGATE	V_HSGATE	V_LSGATE	W_HSGATE	W_LSGATE
1	L	L	H	H	H	L	L	L	PWM	L / !PWM (2)	L	H
2	L	H	H	H	L	L	PWM	L / !PWM (2)	L	L	L	H
3	L	H	L	H	L	H	PWM	L / !PWM (2)	L	H	L	L
4	H	H	L	L	L	H	L	L	L	H	PWM	L / !PWM (2)
5	H	L	L	L	H	H	L	H	L	L	PWM	L / !PWM (2)
6	H	L	H	L	H	L	L	H	PWM	L / !PWM (2)	L	L
1X	H	H	H	L	L	L	L	L	L	L	L	L
2X	L	L	L	H	H	H	L	L	L	L	L	L

(1) Hall sensor is "H" if the positive input terminal voltage is higher than the negative input terminal voltage. States 1X and 2X are illegal input combinations.
(2) During states where the phase is driven with a PWM signal, using asynchronous rectification, the LS gate is held off (L); using synchronous rectification, the LS gate is driven with the inverse of the HS gate.

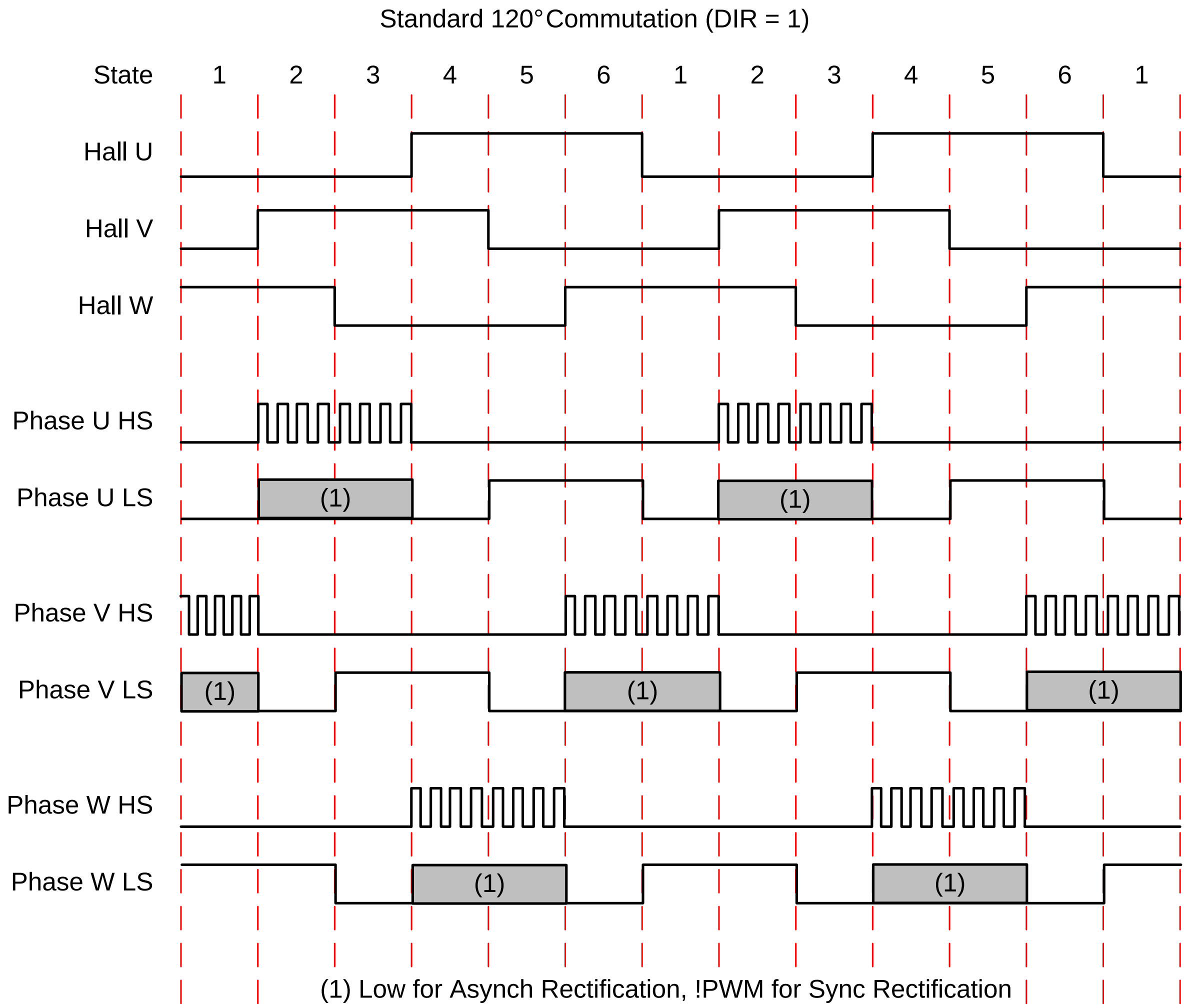


Figure 6. Standard 120° Commutation (DIR = 1)

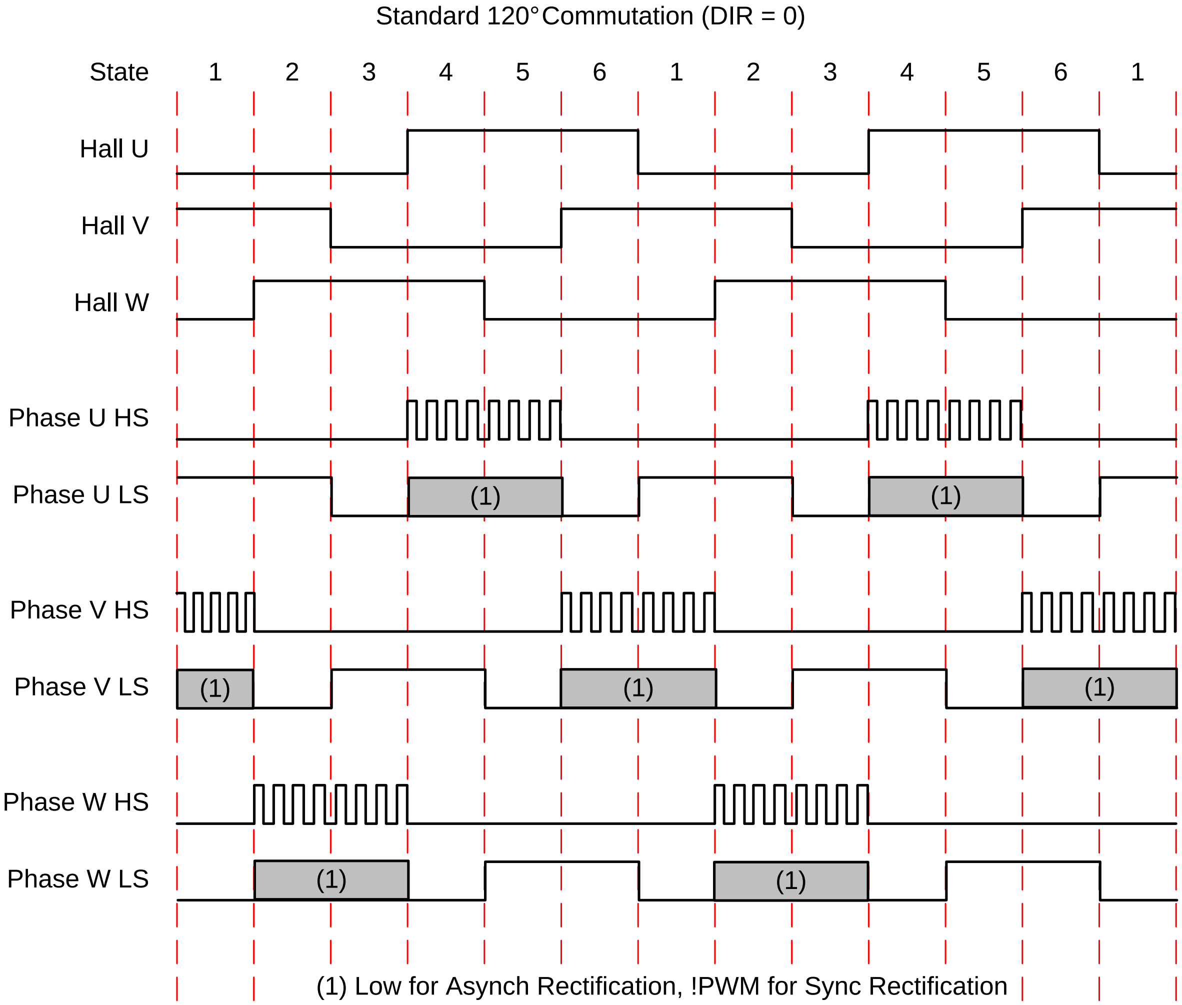


Figure 7. Standard 120° Commutation (DIR = 0)

8.3.4.2 120° Single-Hall Commutation

To generate commutation timing for single-Hall commutation, a digital timer is used to create a clock that runs at 960× the Hall sensor frequency. Only one Hall sensor input, HALL_U, is used for commutation; this eliminates any torque ripple caused by mechanical or electrical offsets of individual Hall sensors.

Single-Hall commutation is only enabled when the register BASIC = 0 and the motor is operating at a nearly constant speed or speed-locked condition. To control this function, logic is used to determine when the speed is constant and the speed control loop is locked. This logic generates the LOCK signal. The LOCK signal is also output on the LOCKn terminal.

Except in PWM input modes, LOCK is also prevented from being signaled if the speed control loop integrator is saturated (either at 0 or full-scale), which indicates that the speed control loop is not locked.

Until LOCK goes active (for example, at start-up, stop, or application of a sudden load that causes motor speed to drop very quickly), standard 120° commutation is used. Because of this, three Hall sensors are required regardless of which commutation method is used.

The commutation timer drives a counter that can be offset with a value programmed in the ADVANCE register. This value allows the phase of commutation to be shifted relative to the actual Hall sensor transitions. Note that the phase advance is not functional in standard 120° commutation. The phase advance also has an automatic mode where the advance value is scaled according to motor speed (see Auto Gain and Advance Compensation).

Timing of 120° single-Hall commutation is essentially the same as standard 120° commutation shown previously. However, there are small time differences of when the transitions occur.

8.3.4.3 180° Sine-Wave-Drive Commutation

180° sine-wave-drive commutation uses a single Hall sensor to generate commutation timing, as described for 120° single-Hall commutation. In addition, the value of the commutation timer modulates the duty cycle of the outputs in accordance with a fixed pattern that approximates sinusoidal current through the windings.

The output of the commutation block is a 12-bit modulation value for each motor phase (U, V, and W) that represents the duty cycle modulation of the PWM for each output. Note that during 120° commutation, these values are either 0 or set to a constant value derived from the MOD120 register.

To make a smooth transition from 120° operation to 180° operation the MOD120 register should be set to a value of 3970.

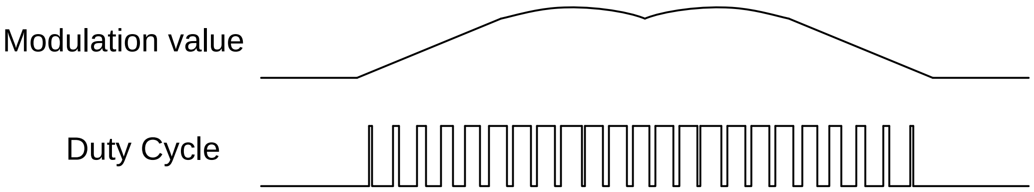


Figure 8.

During 180° sine-wave-drive commutation, commutation transitions occur midway between Hall transitions. The PWM duty cycle is modulated to provide sinusoidal current waveforms. Commutation (shown for asynchronous rectification) is in accordance with the table and diagrams below. Note that the diagrams show a representation of duty cycle, not level, for the PWM states.

Table 3. Commutation for Asynchronous Rectification(1)

STATE	HALL INPUTS						PRE-DRIVE OUTPUTS					
	DIR = 1			DIR = 0			Phase U		Phase V		Phase W	
	U_H	V_H	W_H	U_H	V_H	W_H	U_HSGATE	U_LSGATE	V_HSGATE	V_LSGATE	W_HSGATE	W_LSGATE
1	L	L	H	H	H	L	PWM	L / !PWM(2)	PWM	L / !PWM(2)	L	H
2	L	H	H	H	L	L	PWM	L / !PWM(2)	PWM	L / !PWM(2)	L	H
3	L	H	L	H	L	H	PWM	L / !PWM(2)	L	H	PWM	L / !PWM(2)
4	H	H	L	L	L	H	PWM	L / !PWM(2)	L	H	PWM	L / !PWM(2)
5	H	L	L	L	H	H	L	H	PWM	L / !PWM(2)	PWM	L / !PWM(2)
6	H	L	H	L	H	L	L	H	PWM	L / !PWM(2)	PWM	L / !PWM(2)
1X	H	H	H	L	L	L	L	L	L	L	L	L
2X	L	L	L	H	H	H	L	L	L	L	L	L

(1) Hall sensor is "H" if the positive input terminal voltage is higher than the negative input terminal voltage. States 1X and 2X are illegal input combinations.

(2) During states where the phase is driven with a PWM signal, using asynchronous rectification, the LS gate is held off (L); using synchronous rectification, the LS gate is driven with the inverse of the HS gate.

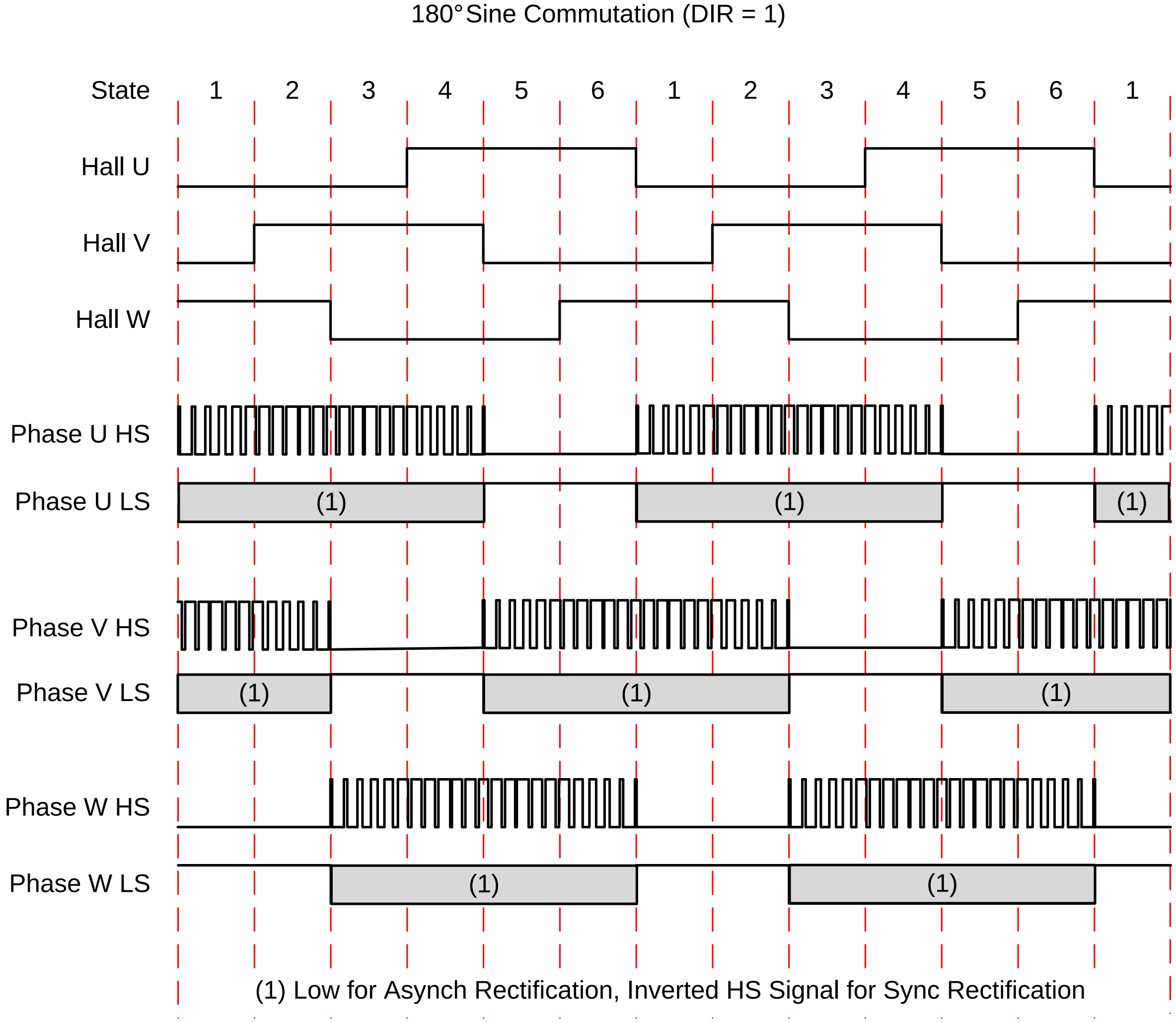


Figure 9. 180° Sine Commutation (DIR = 1)

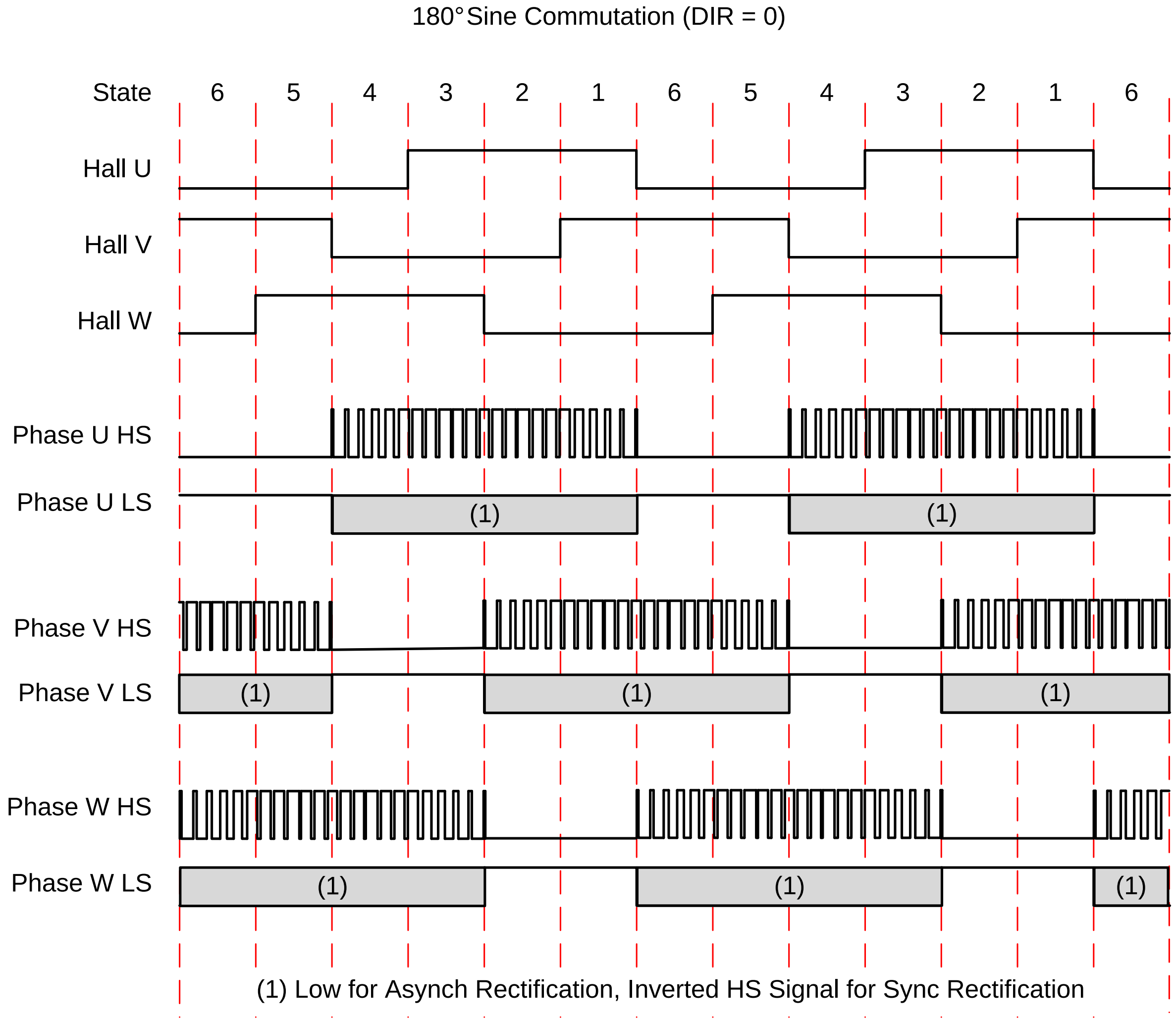


Figure 10. 180° Sine Commutation (DIR = 0)

8.3.5 Commutation Logic Block Diagram

A block diagram of the commutation logic is shown in Figure 11.

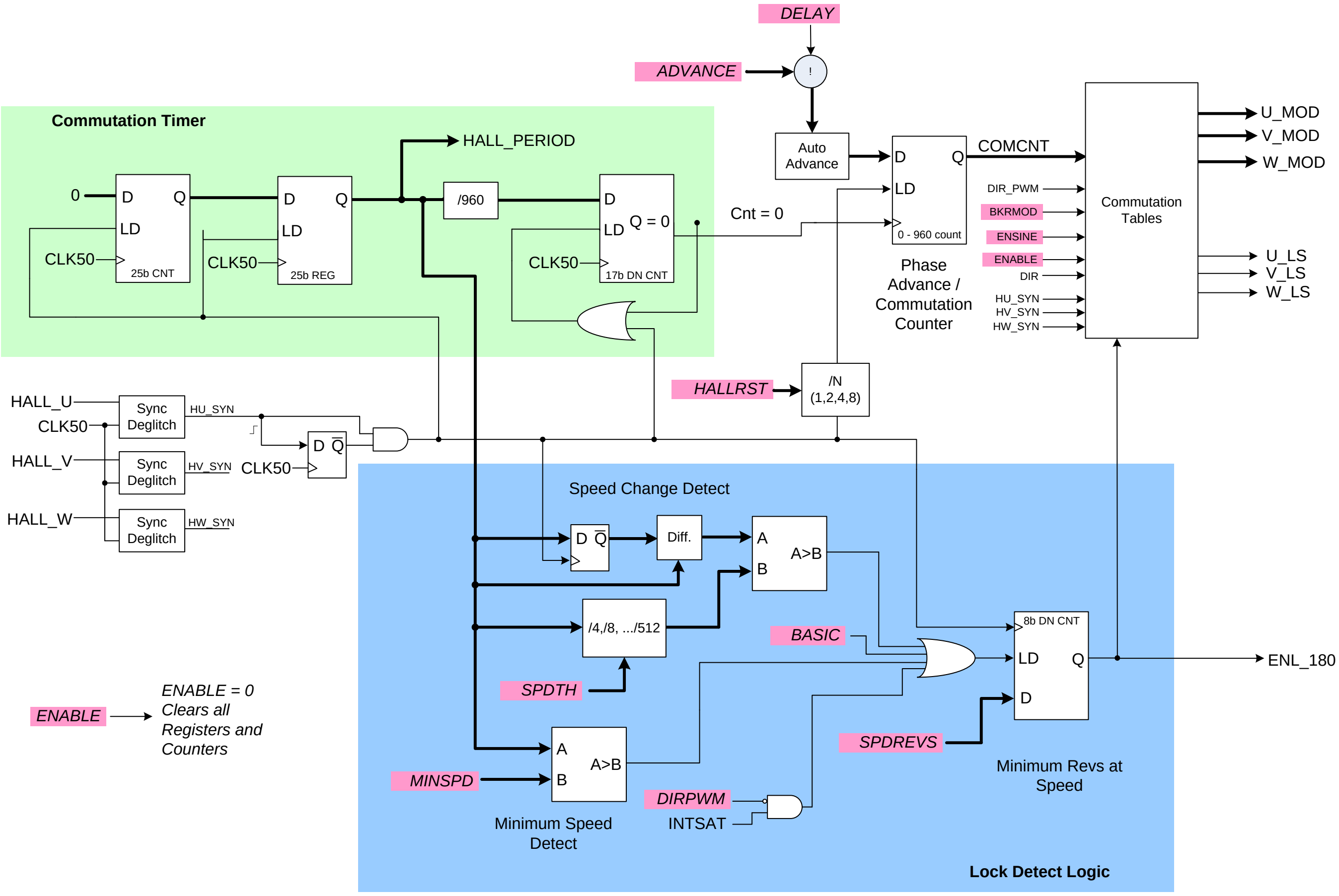


Figure 11. Commutation Logic

8.3.6 Commutation Parameters

A number of commutation parameters are programmable through registers accessed through the serial interface, including:

- ADVANCE — The phase of commutation is advanced (or delayed) relative to the Hall sensor transition by this 8-bit amount. Units are in commutation clocks, which is 1 / 960 of the HALL_U period. Note that phase advance is only applicable in single-Hall commutation modes. An automatic phase advance compensation mode can also be enabled by the AUTOADV bit (see Auto Gain and Advance Compensation for details).
- DELAY — if set, commutation is delayed relative to Hall transitions; if cleared, commutation is advanced relative to Hall transitions.
- BASIC — The BASIC bit, when set, prevents single-Hall or 180° commutation from being entered regardless of the above parameters, forces conventional 120° commutation, and disables ADVANCE functionality.
- ENSINE — The ENSINE bit, when set, selects 180° sinusoidal commutation. The BASIC bit must also be 0.
- HALLRST — HALLRST sets how many HALL_U cycles pass for each commutation counter reset. In other words, the commutation counter is reset every N HALL_U edges. Selections available are 1, 2, 4, and 8.
- MINSPD — Sets the minimum Hall_U period that LOCK can be set. The 8-bit field represents 2.56 ms/count, with a max value of 652.8 ms.
- SPDREVS — After the MINSPD and SPEEDTH criteria are met, SPDREVS adds a minimum number of Hall_U periods that must occur for LOCK to be set.
- SPEEDTH — Sets how much speed variation is allowed across Hall_U periods while keeping LOCK set. This 3-bit field sets the percentage variation allowed by changing a programmable divider. Divisions of 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, and 1/512 are supported. These divisors correspond to 25%, 12.5%, 6.25%,

3.13%, 1.56%, 0.78%, 0.39%, and 0.20% variation per revolution.

The diagram below shows how the lock parameters (MINSPD, SPEEDTH, and SPDREV) affect commutation mode.

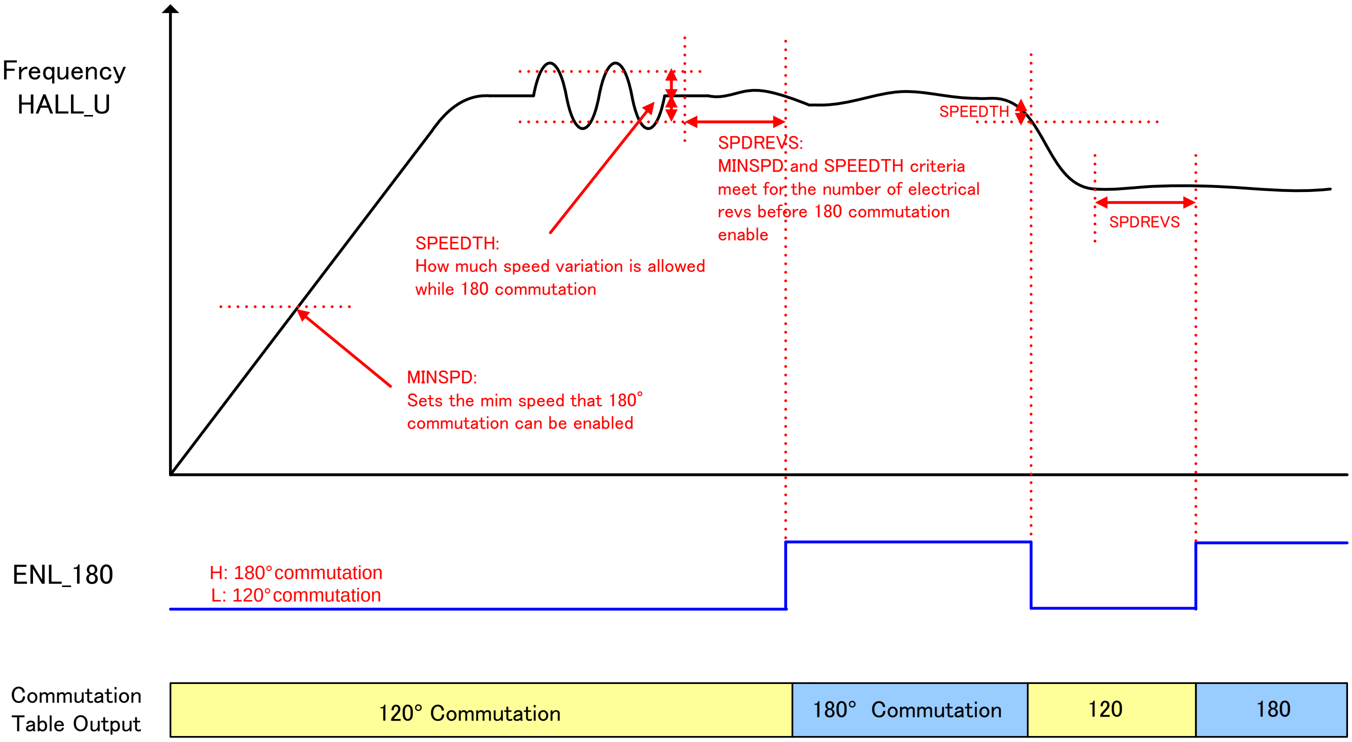


Figure 12.

8.3.7 Braking

Motor braking can be initiated by the BRKPOL register bit as well as the BRAKE terminal. The BRKPOL register bit can also be used to program the polarity of the BRAKE terminal, as it is combined with the terminal with an exclusive-OR function as follows:

Table 4. Brake Behavior

BRAKE Terminal	BRKPOL Register Bit	Resulting Function
0	0	Not brake
0	1	Brake
1	0	Brake
1	1	Not brake

When the motor is braking, all low-side drivers are held in an on state, causing all low-side FETs to turn on, and the integrator is reset to 0.

In addition, braking can be entered when the ENABLE terminal is made inactive. BRKMOD controls the behavior of the outputs when ENABLE is inactive. If BRKMOD= 0, the outputs are 3-stated, resulting in the motor coasting; if BRKMOD = 1, all low-side FETs are turned on, causing the motor to brake.

Table 5. BRKMOD

	BRKMOD = 0 COAST	BRKMOD = 1 BRAKE
RESET = 1	Coast	Brake
BRAKE = active	Brake	Brake
ENABLE = inactive	Coast	Brake

Table 5. BRKMOD (continued)

	BRKMOD = 0 COAST	BRKMOD = 1 BRAKE
DIR	Coast	Brake
Clock off	Brake	Brake
Power down	Coast	Brake

8.3.8 Output Pre-Drivers

The output drivers for each phase consist of N-channel and P-channel MOSFET devices arranged as a CMOS buffer. They are designed to directly drive the gate of external N-channel power MOSFETs.

The outputs can provide synchronous or asynchronous rectification. In asynchronous rectification, only the high-side FET is turned on and off with the PWM signal; current is recirculated using external diodes, or the body diodes of the external FETs. In synchronous rectification, the low side FET is turned on when the high side is turned off.

Synchronous rectification is enabled or disabled using the SYNRECT control bit. When set to 1, synchronous rectification is used. In general, synchronous rectification results in better speed control and higher efficiency.

The high-side gate drive output UHSG is driven to VCP whenever the duty cycle output U_PD from the PWM generator is high, the enable signal U_HS from the commutation logic is active, and the current limit ($V_{LIMITER}$) is not active. If the high-side FET is on and a current limit event occurs, the high-side FET is immediately turned off until the next PWM cycle.

The low-side gate drive ULSG is driven to VM whenever the internal signal U_LS is high, or whenever synchronous rectification is active and UHSG is low.

Phases V and W operate in an identical fashion.

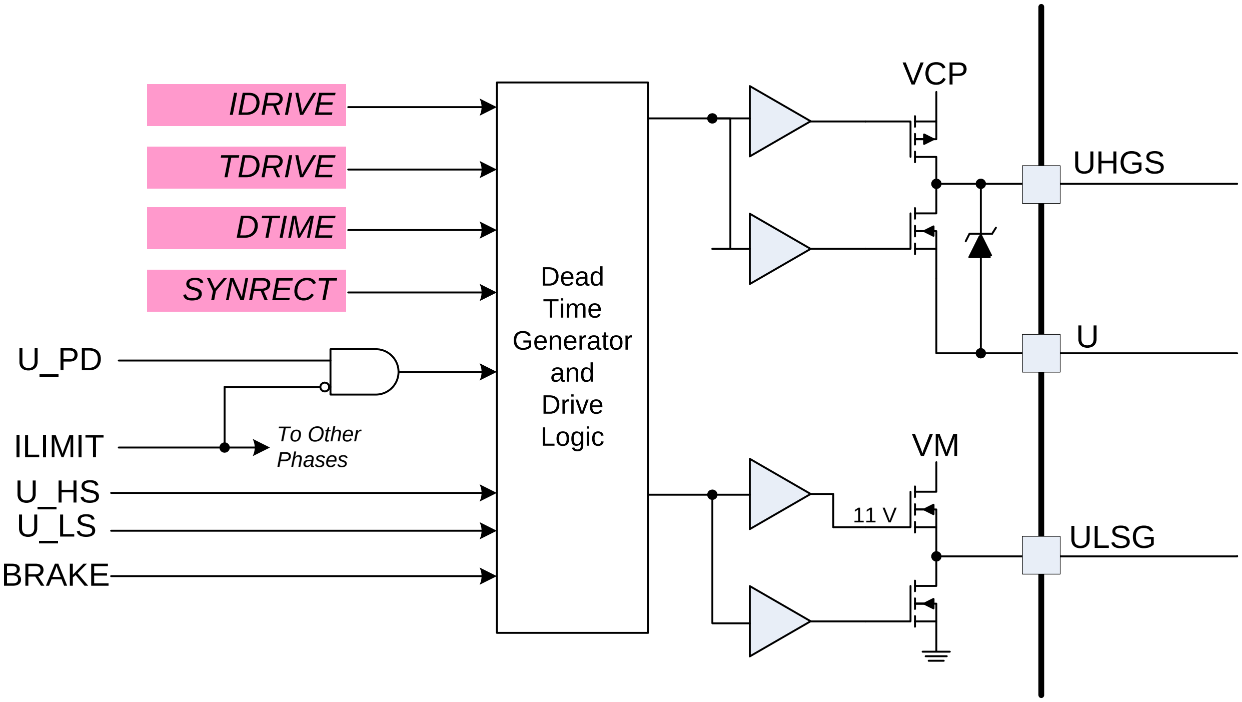


Figure 13.

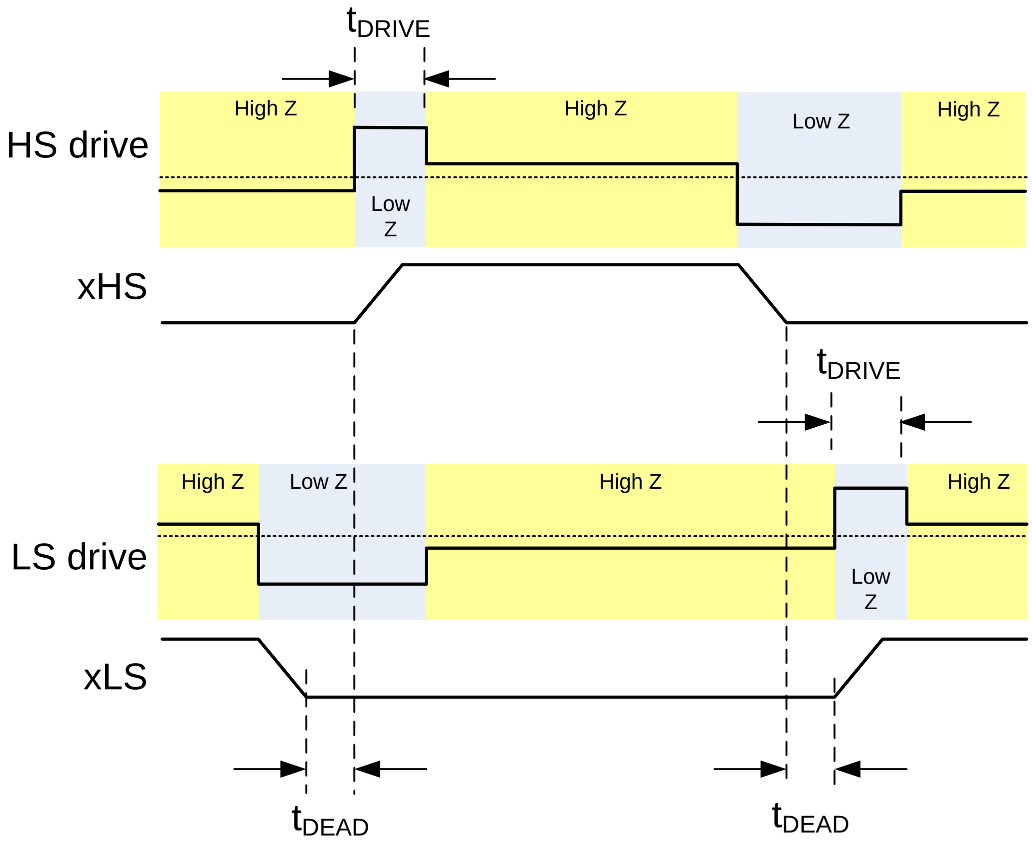


Figure 14.

The peak drive current of the pre-drivers is adjustable by setting the IDRIVE register bits. Peak drive currents may be set between 10 and 130 mA. Adjusting the peak current changes the output slew rate, which also depends on the FET input capacitance and gate charge.

When changing the state of the output, the peak current is applied for a short period of time (t_{DRIVE}), to charge the gate capacitance. This time is selected by setting the TDRIVE register bits. Times of 1, 5, 10, or 15 µs may be selected. After this time, a weak current source is used to keep the gate at the desired state. When selecting the gate drive strength for a given external FET, the selected current must be high enough to fully charge and discharge the gate during the time when driven at full current, or excessive power is dissipated in the FET.

During high-side turn-on, the low-side gate is held low with a low impedance. This prevents the gate-source capacitance of the low-side FET from inducing turn-on. Similarly, during low-side turn-on, the high-side gate is held off with a low impedance.

The pre-driver circuits include enforcement of a dead time in analog circuitry, which prevents the high-side and low-side FETs from conducting at the same time. Additional dead time can be added (in digital logic) by setting the DTIME register bits.

8.3.9 Current Limit

The current limit circuit activates if the voltage detected across the low-side sense resistor exceeds $V_{LIMITER}$. Note that the current limit circuit is ignored immediately after the PWM signal goes active for a short blanking time, to prevent false trips of the current limit circuit.

If current limit activates, the high-side FET is disabled until the beginning of the next PWM cycle. If synchronous rectification is enabled when the current limit activates, the low-side FET is activated while the high-side FET is disabled.

8.3.10 Charge Pump

Since the output stages use N-channel FETs, a gate drive voltage higher than the VM power supply is needed to fully enhance the high-side FETs. The DRV8308 device integrates a charge pump circuit that generates a voltage approximately 10 V more than the VM supply for this purpose.

The charge pump requires two external capacitors for operation. For details on these capacitors (value, connection, and so forth), refer to the Figure 2 and .

The charge pump is shutdown when in standby mode (ENABLE inactive).

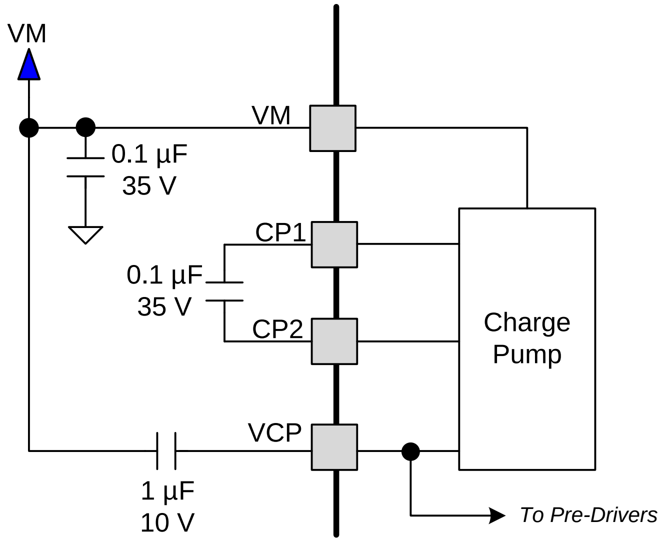


Figure 15.

8.3.11 5-V Linear Regulator

A 5-V linear regulator (VREG) is provided to power internal logic and external circuitry, such as the Hall effect sensors.

A capacitor must be connected from the VREG output to ground, even if the output is not used for external circuitry. The recommended capacitor value is a 0.1-µF, 10-V ceramic capacitor.

The VREG output is designed to provide up to 30-mA output current, but power dissipation and thermal conditions must be considered. As an example, with 24 V in and 20 mA out, power dissipated in the linear regulator is 19 V × 20 mA = 380 mW.

The VREG regulator is shutdown in standby mode (when ENABLE is inactive).

8.3.12 Power Switch

A low-current switch is provided in the DRV8308 device that can be used to power the Hall sensors or other external circuitry through the VSW terminal. When ENABLE is active the switch is turned on, connecting the VSW terminal to VM. When ENABLE is inactive the switch is turned off (standby mode).

8.3.13 Protection Circuits

A number of protection circuits are included in the DRV8308 device. Faults are reported by asserting the FAULTn terminal (an active-low, open-drain output signal), as well as setting the appropriate bit or bits in the FAULT register. Note that bits in the FAULT register remain set until either a 0 is written to them, RESET is asserted, or the device power is cycled.

8.3.13.1 VM Undervoltage Lockout (UVLO)

If the VM power supply drops, there may not be enough voltage to fully turn on the output FETs. Operation in this condition causes excessive heating in the output FETs. To protect against this, the DRV8308 device contains an undervoltage lockout circuit.

In the event that the VM supply voltage drops below the undervoltage lockout threshold (V_{UVLO}), the FAULTn terminal is driven active and the motor driver is disabled. After VM returns to a voltage above the undervoltage lockout threshold, the FAULTn terminal is high impedance and operation of the motor driver automatically resumes.

The UVLO bit in the FAULT register is set. This bit remains set until a 0 is written to the UVLO bit.

At power-up, the UVLO bit is set.

Note that register reads and writes are still possible during the UVLO condition, as long as VM stays above the VM reset threshold. If VM drops below the VM reset threshold, all registers are reset and register read or write is not functional.

8.3.13.2 VM Overvoltage (VMOV)

In some cases, if synchronous rectification is used, energy from the mechanical system can be forced back into the VM power supply. This can result in the VM power supply being boosted by the energy in the mechanical system, causing breakdown of the output FETs, or damaging the DRV8308 device. To protect against this, the DRV8308 device has overvoltage protection.

There are two overvoltage thresholds, selectable by the OVTH bit. An overvoltage event is recognized if the VM voltage exceeds the selected overvoltage threshold (VM_{OVLO}). Note that for the output FETs to be protected, they must be rated for a voltage greater than the selected overvoltage threshold.

In the event of an overvoltage, the FAULTn terminal is pulled low. If synchronous rectification is enabled, the output stage is forced into asynchronous rectification. After VM returns to a voltage below the overvoltage threshold, the FAULTn terminal is high impedance. If synchronous rectification was enabled prior to the overvoltage event, after a fixed 60-µs delay, synchronous rectification is re-enabled.

The VMOV bit in the FAULT register is set. This bit remains set until a 0 is written to the VMOV bit.

8.3.13.3 Motor Overcurrent (OCP)

Overcurrent protection (OCP) is provided on each FET in addition to the current limit circuit. The OCP circuit is designed to protect the output FETs from atypical conditions such as a short circuit between the motor outputs and each other, power, or ground.

The OCP circuit is independent from the current limit circuitry. OCP works by monitoring the voltage drop across the external FETs when they are enabled. If the voltage across a driven FET exceeds V_{FETOCP} for more than t_{FETOCP} an OCP event is recognized. V_{FETOCP} is configurable by register OCPTH and t_{FETOCP} is configurable by register OCPDEG.

In addition to monitoring the voltage across the FETs, an OCP event is triggered if the voltage applied to the ISEN terminal exceeds the $V_{SENSEOCP}$ threshold voltage.

In the event of an OCP event, FAULTn is pulled low, and the motor driver is disabled.

After a fixed delay of 5 ms, the FAULTn terminal is driven inactive and the motor driver is re-enabled.

The OCP bit in the FAULT register is set when an OCP event is recognized. This bit remains set until a 0 is written to the OCP bit.

8.3.13.4 Charge Pump Failure (CPFAIL)

If the voltage generated by the high-side charge pump is too low, the high-side output FETs are not fully turned on, and excessive heating results. To protect against this, the DRV8308 device has a circuit that monitors the charge pump voltage.

If the charge pump voltage drops below VCPFAIL, the FAULTn terminal is pulled low and the motor driver is disabled. After the charge pump voltage returns to a voltage above the VCPFAIL threshold, the FAULTn terminal is high impedance and operation of the motor driver automatically resumes.

The CPFAIL bit in the FAULT register is set when the charge pump voltage drops below VCPFAIL. This bit remains set until a 0 is written to the CPFAIL bit.

At power-up, the CPFAIL bit is set.

8.3.13.5 Charge Pump Short (CPSC)

To protect against excessive power dissipation inside the DRV8308 device, a circuit monitors the charge pump and disables it in the event of a short circuit on the PCB.

If a short circuit is detected on the charge pump, the FAULTn terminal is pulled low and the motor driver is disabled. After a fixed period of 5 s, the FAULTn terminal is high impedance and operation of the motor driver automatically resumes. If the short circuit condition is still present, the cycle repeats.

The CPSC bit in the FAULT register is set when a short circuit is detected on the charge pump. This bit remains set until a 0 is written to the CPSC bit.

8.3.13.6 Rotor Lockup (RLOCK)

Circuitry in the DRV8308 device detects a locked or stalled rotor. This can occur in the event of a mechanical jam or excessive torque load that causes the motor to stop rotating while enabled. The rotor lock condition is set if there are no transitions detected on the FGOUT signal for a programmable period of time (set by the LRTIME register bits). RLOCK can also occur if the 3 Hall signals are an invalid state (all High or all Low), which can be caused by a bad wire connection.

If a locked rotor condition is recognized, the FAULTn terminal is pulled low, the motor driver is disabled and the RLOCK bit in the FAULT register is set. The RLOCK bit remains set until a 0 is written to the RLOCK bit.

If the RETRY bit is set, the part re-enables itself after a fixed delay of 5 s.

If the RETRY bit is not set, the part disables the pre-drivers until RESET is asserted, or power has been removed and reapplied to the device.

8.3.13.7 Overtemperature (OTS)

To protect against any number of faults that could result in excessive power dissipation inside the device, the DRV8308 device includes overtemperature protection.

Overtemperature protection activates if the temperature of the die exceeds the OTS threshold temperature (T_{TSD}). If this occurs, the FAULTn terminal is pulled low, the device is disabled and the OTS bit in the FAULT register is set. This OTS bit remains set until a 0 is written to the OTS bit.

If the RETRY bit is set after the temperature has fallen below the OTS threshold, the part re-enables itself after a fixed delay of 5 s.

If the RETRY bit is not set, the part disables the pre-drivers until RESET is asserted, or until power has been removed and re-applied to the device.

8.3.14 Serial Interface

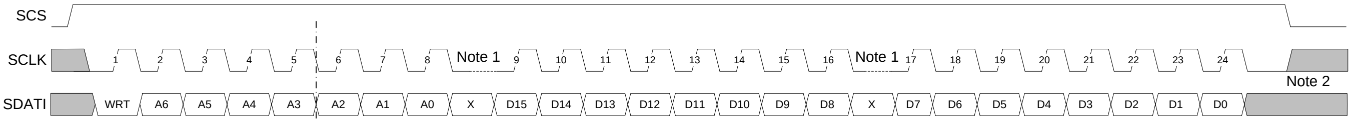
A simple SPI serial interface is used to write to the control registers in the DRV8308 device. Optionally, the interface can be configured to automatically load the registers from an external EEPROM device.

Data is shifted into a holding register when SCS is active high. When SCS is returned to inactive (low), the data received is latched into the addressed register.

8.3.15 Serial Data Format

The serial data consists of a 24-bit serial write, with a read or write bit, 7 address bits, and 16 data bits. The address bits identify one of the registers defined in Table 7.

To write to a register, data is shifted in after the address as shown in Figure 16:

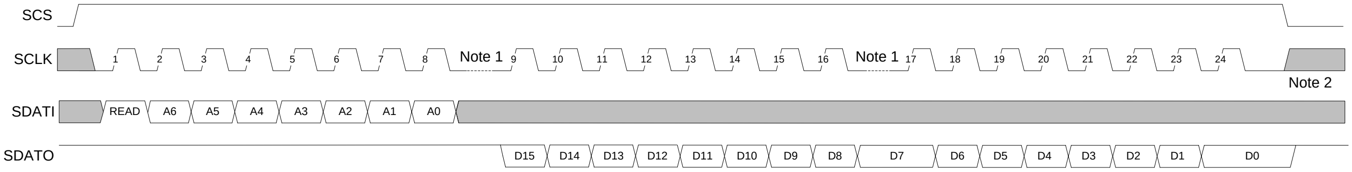


A. Any amount of time may pass between bits, as long as SCS stays active high. This allows 8-bit writes to be used.

B. Any additional clock edges encountered after the 24th edge are ignored.

Figure 16. Timing Diagram

Data may be read from the registers through the SDATO terminal. During a read operation, only the address is used form the SDATI terminal; the data bits following are ignored. Reading is enabled by setting the READ bit at the beginning of the access:



A. Any amount of time may pass between bits, as long as SCS stays active high. This allows 8-bit writes to be used.

B. Any additional clock edges encountered after the 24th edge are ignored.

Figure 17.

8.3.16 Programming the OTP Configuration Memory

To permanently program data in to the internal OTP memory, data is first written into the internal registers described previously.

To write all of the register values into the OTP, follow this sequence:

Table 6.

ADDRESS	DATA	ACTION
0x2Dh	0x1213h	write
0x2Dh	0x1415h	write
0x2Dh	0x1617h	write
0x2Dh	0x1819h	write
0x39h	0x0002h	write
--	--	wait 10 ms minimum
0x2Dh	0EDDh	write

The internal OTP memory can only be programmed once. After programming, the registers can still be overwritten by accesses through the SPI port, or by using an external EEPROM.

8.4 Device Functional Modes

8.4.1 Speed Control

The DRV8308 device is designed to support a wide range of motor speeds and constructions. Speeds of up to approximately 50000 RPM are supported with motor constructions of up to 16 poles, or corresponding lower speeds with more poles. This translates into a Hall sensor speed of up to 6.7 kHz. (The frequency of one Hall sensor can be calculated by RPM × (motor poles) / 120.)

Speed control of the motor is accomplished by varying the duty cycle of the PWM outputs. Three methods of speed control input are possible with the DRV8308 device:

- Clock frequency mode: uses a clock input that is frequency-locked to the FG frequency, for closed-loop speed control.
- Clock PWM mode: uses a clock input with duty cycle information to control the speed of the motor. This is open-loop.
- Internal register PWM mode: uses a programmed register value that represents duty cycle to control the speed of the motor. This is open-loop.

The speed mode is selected by the SPDMODE register.

8.4.1.1 Clock Frequency Mode

In clock frequency mode, the clock signal is deglitched by the 51.2-MHz clock. The deglitched input, along with the FG signal (derived from the FG amplifier, TACH input, or the Hall sensors), are input to a speed differentiator, where the CLKIN signal is compared to the actual speed of the motor (determined by the FG frequency). The speed differentiator outputs are UP and DOWN pulses.

The deglitcher and speed differentiator are shown in Figure 18:

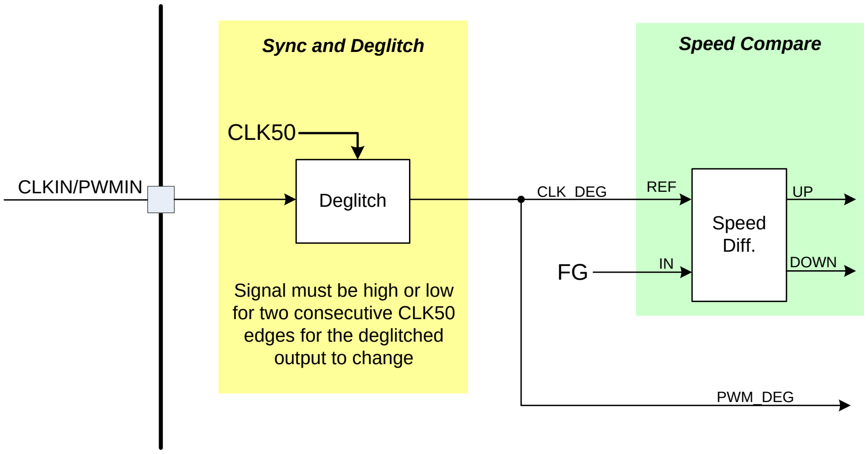


Figure 18. Clock Frequency Mode

The UP and DOWN outputs of the speed differentiator are integrated by accumulating the value set by the SPDGAIN register for each cycle of the integrator clock (CLK50 divided by the value of the INTCLK register) that an UP or DOWN signal is active. If UP is active, the amount is added to the current integrator output; if the DOWN input is active, the value is subtracted. If neither signal is active, the integrator output remains the same. Note that the integrator output is reset to 0 at any time the motor is disabled or in brake, and at reset. The integrator output does not roll over at maximum or minimum count.

At the moment that ENABLE is made active, the integrator and filters are reset to 0. If there are no transitions on the CLKIN terminal, no UP pulses are generated, so the integrator remains at 0, and the motor is not driven.

Once the motor is running, if the signal on CLKIN stops, DOWN pulses are generated until the integrator reaches 0. This actively decelerates the motor (brake) until the motor stops.

Device Functional Modes (continued)

The output of the integrator is applied to a programmable digital filter. The filter has one pole and one zero. The pole location is programmable from approximately 100 to 1600 Hz, and is set via the FILK1 register; the zero location is programmable from 2 to 100 Hz and is set via the FILK2 register. The filter may be bypassed by setting the BYPFILT bit.

For a given pole and zero frequency, FILK1 and FILK2 are calculated as follows:

$$\mathrm{FILK2} = 2^{19}\,\frac{2\pi\frac{f_z}{f_s}}{1+\pi\frac{f_z}{f_s}}, \qquad \mathrm{FILK1} = 2^{16}\,\frac{2\pi\frac{f_p}{f_s}}{1+\pi\frac{f_p}{f_s}}$$

where

- f_z is the desired zero frequency
- f_p is the desired pole frequency
- f_s is the filter sample rate (195000 Hz)
- The result is rounded to the nearest integer (1)

Following the filter is a programmable lead compensator, which also contains one pole and one zero. The compensator characteristics are programmable by the COMPK1 and COMPK2 registers. Center frequency is programmable between 20 and 100 Hz, with a phase lead between 0° and 80°. The compensator may be bypassed by setting the BYPCOMP bit.

For a given pole and zero frequency, COMPK1 and COMPK2 are calculated as follows:

$$\mathrm{COMPK2} = 2^{19}\,\frac{2\pi\frac{f_z}{f_s}}{1+\pi\frac{f_z}{f_s}}, \qquad \mathrm{COMPK1} = 2^{16}\,\frac{2\pi\frac{f_p}{f_s}}{1+\pi\frac{f_p}{f_s}}$$

where

- f_z is the desired zero frequency
- f_p is the desired pole frequency
- f_s is the filter sample rate (195000 Hz)
- The result is rounded to the nearest integer (2)

To calculate the parameters from a center frequency and desired phase lead, a tabular estimation is used. Consult the factory for a spreadsheet to aid in this calculation.

The digital filter and compensator are reset to 0 whenever the motor is disabled.

The integrator, filter, and lead compensator result in a typical open-loop response as shown in Figure 19. Note that the locations of the poles and zeros are not restricted to what is shown.

Device Functional Modes (continued)

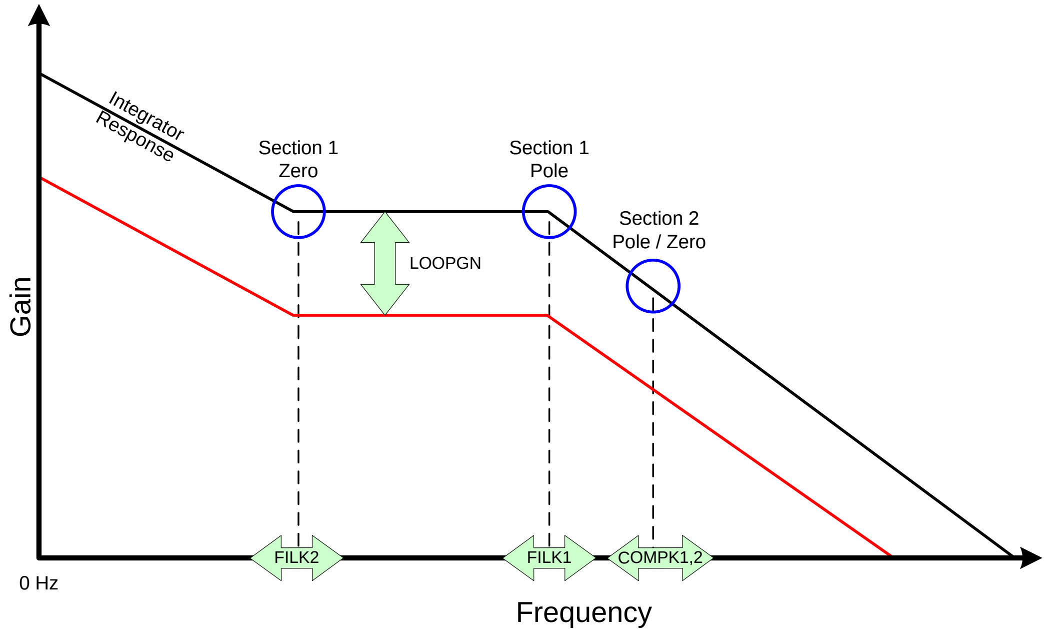


Figure 19. Open-Loop Response

The integrator and filters are shown in Figure 20:

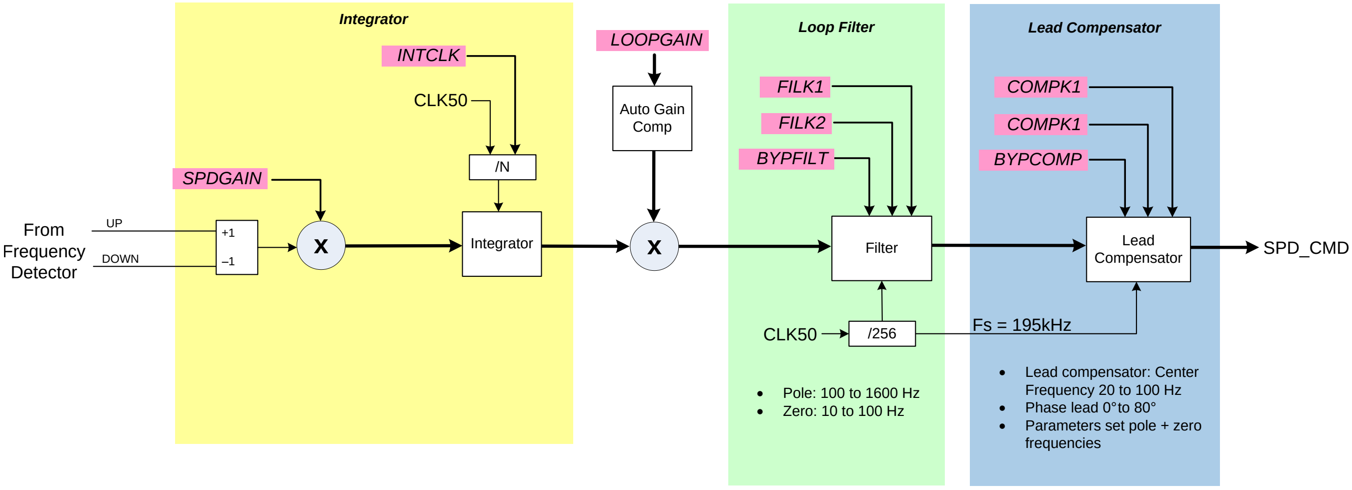


Figure 20. Integrator and Filters

The output of the filters is a speed command, SPD_CMD.

8.4.1.2 Clock PWM and Internal Register PWM Modes

In PWM input modes, the PWM input signal is timed using a 50 MHz clock to generate a 12-bit number that corresponds to the duty cycle of the incoming PWM signal. The input PWM frequency should be between 16 and 50 kHz, higher PWM frequencies work, but resolution is degraded. Note that the gate driver's output PWM frequency is independent of the speed control PWM input frequency; the output PWM frequency is selected by the PWMF register bits.

The measured input duty cycle is scaled by the contents of the MOD120 register. With a full-scale MOD120 register (4095 decimal), the output duty cycle is 2× the input duty cycle. To make the output duty cycle equal to the input, a value of 2048 decimal should be written to MOD120.

Device Functional Modes (continued)

An additional multiplication factor of 2 is introduced when the BYPCOMP bit is set; if BYPCOMP is set, the output duty cycle is 4× the input duty cycle (when MOD120 is 4095).

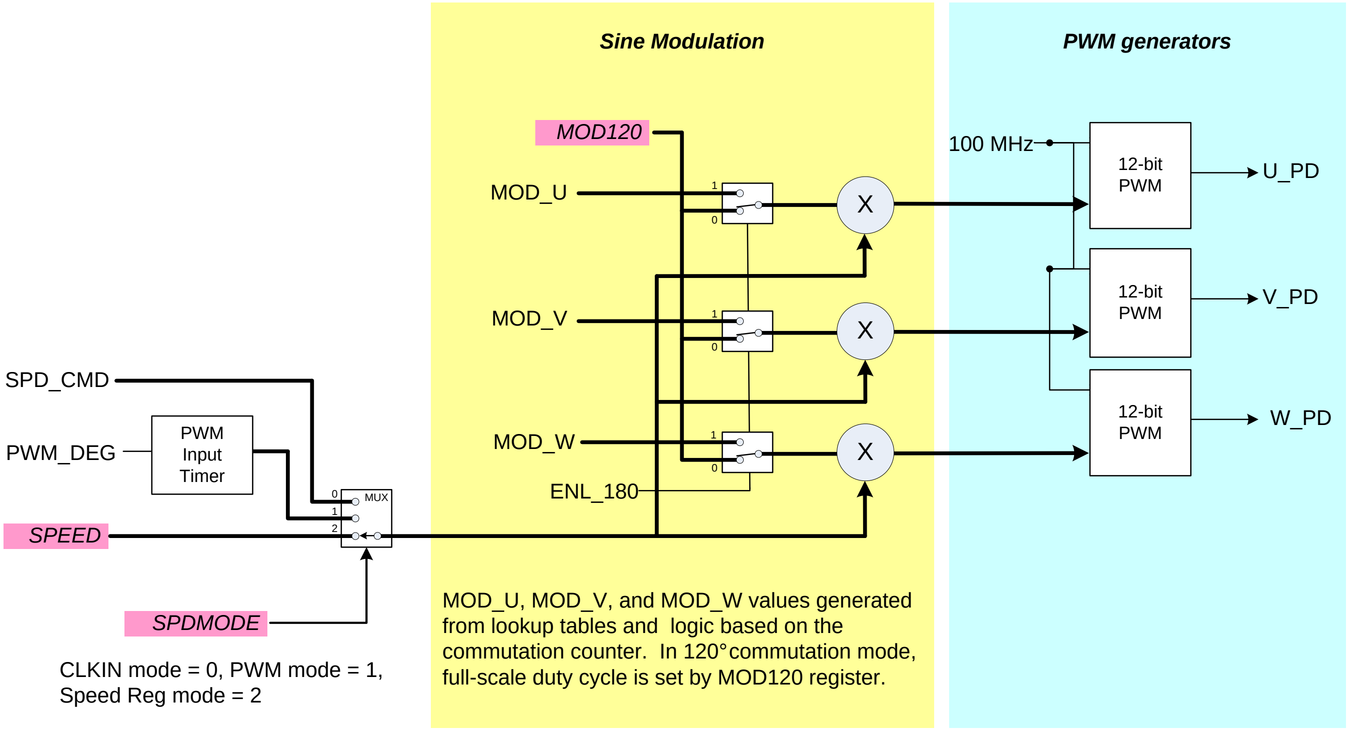
In register speed control mode, a 12-bit register SPEED is used to directly provide the speed command.

During sine commutation, the input duty cycle is multiplied by the modulation values for each phase (MOD_U, MOD_V, and MOD_W) to generate a 12-bit value that determines the output PWM duty cycle of each phase. Note that in 120° commutation, the MOD values are fixed at a duty cycle that is set by the MOD120 register.

The PWM frequency can be set to either 25, 50, 100, or 200 kHz, with register PWMF. Lower PWM frequencies are desirable to minimize switching losses; higher PWM frequencies provide better control resolution, especially at very high motor speeds.

The outputs of the PWM generators are the signals U_PD, V_PD, and W_PD. These contain the duty cycle information for each phase.

Modulation and PWM generation is shown in Figure 21:



CLKIN mode = 0, PWM mode = 1,
Speed Reg mode = 2

MOD_U, MOD_V, and MOD_W values generated from lookup tables and logic based on the commutation counter. In 120° commutation mode, full-scale duty cycle is set by MOD120 register.

Figure 21. Modulation and PWM Generation

8.4.2 Auto Gain and Advance Compensation

The DRV8308 device provides modes to automatically scale the loop gain and the phase advance settings based on motor speed. This helps improve loop stability and motor performance in cases where the motor must operate over a wide speed range with a single set of parameters. For applications that run at only one speed, these functions should be left disabled.

Auto gain compensation is enabled by setting the AUTOGAIN bit. Auto gain will scale the LOOPGAIN of the system using the following equation (the DC gain that FLK2/FILK1 and COMK2/COMK1 are still in effect):

$$\text{Computed Gain} = \text{LOOPGAIN} / \text{AG\_SETPT} \times f_{\text{CLKIN}} \quad (3)$$

Automatic advance is enabled by setting the AUTOADV bit. The advance setting is scaled such that at zero speed, there is no phase advance. As speed increases, the phase advance is increased using the equation below:

$$\text{Computed Advance} = \text{ADVANCE} / \text{AAA\_SETPT} \times f_{\text{Hall\_U}} \quad (4)$$

Device Functional Modes (continued)

Both the gain and advance values are latched when LOCK goes active (when the motor is at constant speed).

The auto gain and advance functions are shown in Figure 22:

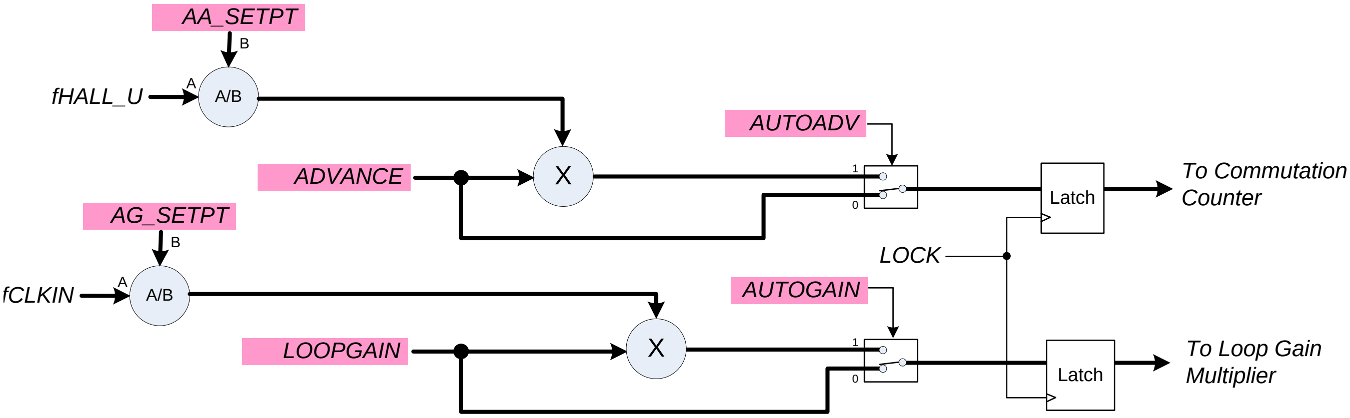


Figure 22. Auto Gain and Advance Functions

8.4.3 External EEPROM Mode

A serial EEPROM can be connected to the serial port to load the register contents. To activate external EEPROM mode, connect the SMODE terminal to logic high. This causes the SPI interface to act as a master, and load data from an external EEPROM. The DRV8308 device latches data on the falling edge of SCLK.

The serial EEPROM should be a microwire-compatible, 16-bit-word device, such as the 93C46B. The VREG power supply can be used to power the EEPROM. Connections are as shown in Figure 23:

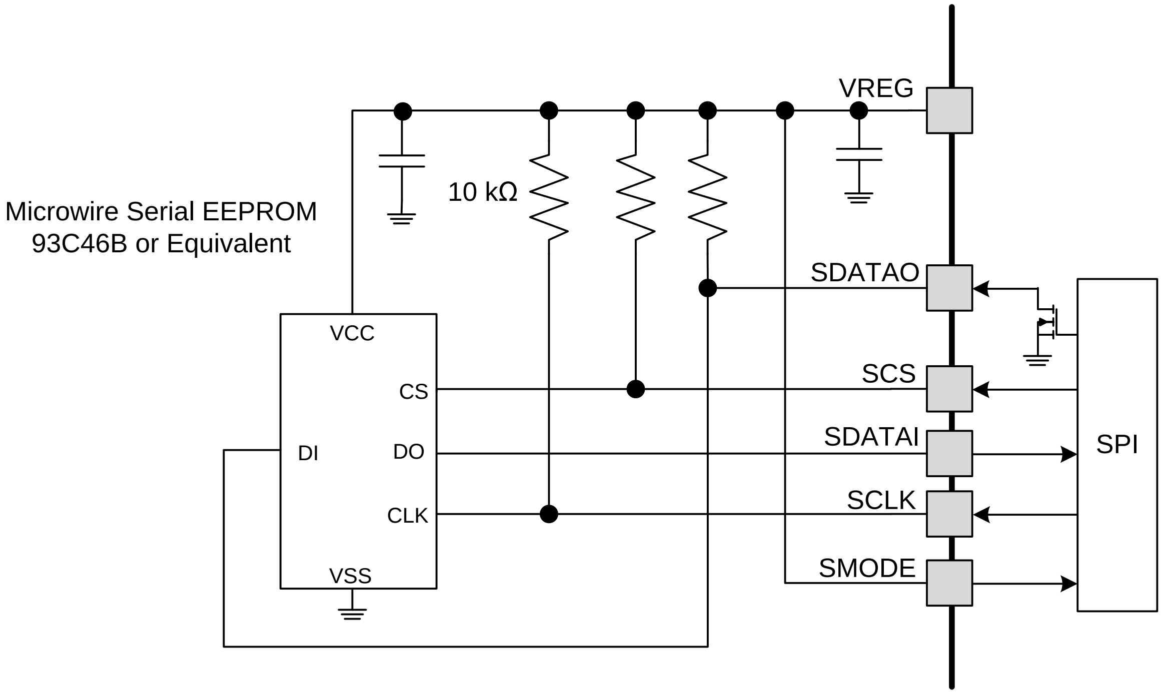


Figure 23.

Data in the EEPROM should be arranged starting at address 0 exactly as shown in Table 6. EEPROM data bits 12 to 15 are unused.

Device Functional Modes (continued)

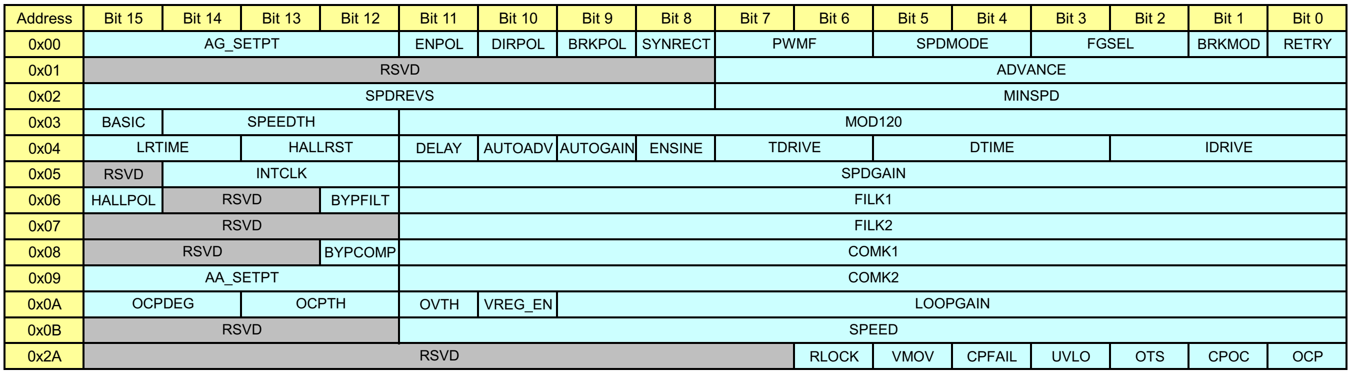
To program the EEPROM device in-circuit while connected to the DRV8308 device, place the DRV8308 device into the reset state by driving RESET high. This 3-states the serial interface terminals and allows them to be overdriven by external programming logic. Alternatively, the EEPROM may be programmed off-board before assembly. The DRV8308 device cannot program an EEPROM.

8.5 Register Map

8.5.1 Control Registers

The DRV8308 device uses internal registers to set operation parameters, including the characteristics of the speed control loop, commutation settings, gate drive current, and so forth. The registers are programmed through a serial SPI communications interface. In addition, the registers can be permanently programmed into non-volatile OTP memory, or loaded from an external serial EEPROM device.

This is the register map:



Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	AG_SETPT				ENPOL	DIRPOL	BRKPOL	SYNRECT	PWMF		SPDMODE		FGSEL		BRKMOD	RETRY
0x01	RSVD								ADVANCE							
0x02	SPDREVS								MINSPD							
0x03	BASIC	SPEEDTH			MOD120											
0x04	LRTIME		HALLRST		DELAY	AUTOADV	AUTOGAIN	ENSINE	TDRIVE		DTIME			IDRIVE		
0x05	RSVD	INTCLK			SPDGAIN											
0x06	HALLPOL	RSVD		BYPFILT	FILK1											
0x07	RSVD				FILK2											
0x08	RSVD			BYPCOMP	COMK1											
0x09	AA_SETPT				COMK2											
0x0A	OCPDEG		OCPTH		OVTH	VREG_EN	LOOPGAIN									
0x0B	RSVD				SPEED											
0x2A	RSVD									RLOCK	VMOV	CPFAIL	UVLO	OTS	CPOC	OCP

Figure 24. Register Map

At power-up, when VM rises above the VM reset threshold, or whenever RESET is toggled, the register contents are loaded from the OTP memory or EEPROM (depending on SMODE). For details on external EEPROM connections, see External EEPROM Mode. If the OTP has not been programmed and the DRV8308 device is powered-up with SMODE low, the default register values are all 0, except for the FAULT register, which defaults to 0x18. FAULT bits can be cleared by writing 0.

At any time, the register contents may be written or overwritten through the SPI interface.

For detailed descriptions for each register, refer to the prior sections.

Register Map (continued)

Table 7. Register Descriptions

ADDRESS	BIT	NAME	DESCRIPTION	TYPE[1]
0x00	15:12	AG_SETPT	Autogain Setpoint 0000 = 3 Hz 0100 = 48 Hz 1000 = 763 Hz 1100 = 12 kHz 0001 = 6 Hz 0101 = 95 Hz 1001 = 1.5 kHz 1101 = 24 kHz 0010 = 12 Hz 0110 = 191 Hz 1010 = 3 kHz 1110 = 49 kHz 0011 = 24 Hz 0111 = 382 Hz 1011 = 6 kHz 1111 = 98 kHz	RW
	11	ENPOL	ENABLE terminal polarity 0 = Device is active when ENABLE is high 1 = Device is active when ENABLE is low	RW
	10	DIRPOL	DIR terminal polarity 0 = Normal direction when DIR is high 1 = Normal direction when DIR is low	RW
	9	BRKPOL	BRAKE terminal polarity 0 = Brake when BRAKE is high 1 = Brake when BRAKE is low	RW
	8	SYNRECT	Synchronous rectification 0 = Disabled 1 = Enabled	RW
	7:6	PWMF	The PWM frequency used on the external FETs 00 = 25 kHz 01 = 50 kHz 10 = 100 kHz 11 = 200 kHz	RW
	5:4	SPDMODE	Speed control mode 00 = Clock frequency mode 01 = Clock PWM mode 10 = Internal register PWM mode 11 = Reserved	RW
	3:2	FGSEL	FG select 00 = Use HALL_U to generate FG 01 = Use XOR of all three Hall sensors 10 = Use FG amplifier input 11 = Use TACH input signal	RW
	1	BRKMOD	Motor brake mode 0 = Coast when ENABLE is inactive (outputs 3-state) 1 = Brake when ENABLE is inactive (all low-side FETs on)	RW
	0	RETRY	Retry mode 0 = Latch off in case of fault 1 = Automatic retry in case of fault	RW
0x01	15:8	RSVD	Reserved	–
	7:0	ADVANCE	Commutation timing advance versus Hall signals; each count is 1 / 960 the Hall_U period	RW
0x02	15:8	SPDREVS	After the MINSPD and SPEEDTH criteria are met, SPDREVS adds a minimum number of Hall_U periods that must occur for LOCK to be set	RW
	7:0	MINSPD	Sets the minimum Hall_U period that LOCK can be set; each count is 2.56 ms	RW
0x03	15	BASIC	Basic operation 0 = Normal device operation 1 = Disables ADVANCE functionality and forces 3-Hall 120° commutation	RW
	14:12	SPEEDTH	Speed change tolerance for LOCK 000 = 1/512 rev (0.20%) 011 = 1/64 rev (1.56%) 110 = 1/8 rev (12.5%) 001 = 1/256 rev (0.39%) 100 = 1/32 rev (3.13%) 111 = 1/4 rev (25%) 010 = 1/128 rev (0.78%) 101 = 1/16 rev (6.25%)	RW
	11:0	MOD120	Scales the input duty cycle in PWM modes	RW

---

(1) R = Read Only; RW = Read or Write. Fault registers can only be written 0.

Register Map (continued)

Table 7. Register Descriptions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	TYPE(1)
0x04	15:14	LRTIME	Locked rotor timeout 00 = RLOCK occurs after 1 s 01 = RLOCK occurs after 3 s 10 = RLOCK occurs after 5 s 11 = RLOCK occurs after 10 s	RW
	13:12	HALLRST	Sets the frequency to reset the Hall commutation counter 00 = Every Hall_U cycle 01 = Every 2nd Hall_U cycle 10 = Every 4th Hall_U cycle 11 = Every 8th Hall_U cycle	RW
	11	DELAY	Controls whether ADVANCE leads or lags Hall signals 0 = Commutate after Hall signals arrive 1 = Commutate before Hall signals arrive	RW
	10	AUTOADV	Enables automatic advance compensation 0 = Disabled 1 = Enabled	RW
	9	AUTOGAIN	Enables automatic gain compensation 0 = Disabled 1 = Enabled	RW
	8	ENSINE	Enables 180° sine wave current drive 0 = Disabled 1 = Enabled	RW
	7:6	TDRIVE	Predriver high-current drive time 00 = 1 µs 01 = 5 µs 10 = 10 µs 11 = 15 µs	RW
	5:3	DTIME	Predriver dead time between high-side and low-side driving (typical) 000 = 60 ns 001 = 120 ns 010 = 240 ns 011 = 500 ns 100 = 740 ns 101 = 1.0 µs 110 = 1.24 µs 111 = 1.5 µs	RW
	2:0	IDRIVE	Predriver output peak current 000 = 10 mA 001 = 20 mA 010 = 30 mA 011 = 50 mA 100 = 90 mA 101 = 100 mA 110 = 110 mA 111 = 130 mA	RW
0x05	15	RSVD	Reserved	–
	14:12	INTCLK	Integrator clock frequency 000 = 50 MHz 001 = 25 MHz 010 = 12.5 MHz 011 = 6.3 MHz 100 = 3.1 MHz 101 = 1.6 MHz 110 = 0.8 MHz 111 = 0.4 MHz	RW
	11:0	SPDGAIN	Speed compensator gain	RW
0x06	15	HALLPOL	Hall polarity 0 = Hall signal logic levels are directly used 1 = Hall signal logic levels are inverted	RW
	14:13	RSVD	Reserved	–
	12	BYPFILT	Bypass the filter that FILK1 and FILK2 configure 0 = Filter is enabled 1 = Filter is disabled (FILK1 and FILK2 are ignored)	RW
	11:0	FILK1	Filter coefficient that sets the pole frequency	RW
0x07	15:12	RSVD	Reserved	–
	11:0	FILK2	Filter coefficient that sets the zero frequency	RW

Register Map (continued)

Table 7. Register Descriptions (continued)

ADDRESS	BIT	NAME	DESCRIPTION	TYPE[1]
0x08	15:13	RSVD	Reserved	–
	12	BYPCOMP	Bypass the compensator (COMK1 and COMK2 are ignored) 0 = Filter is enabled 1 = Filter is disabled (FILK1 and FILK2 are ignored)	RW
	11:0	COMK1	Compensator coefficient that sets the pole frequency	RW
0x09	15:12	AA_SETPT	Autoadvance setpoint 0000 = 3 Hz 0001 = 6 Hz 0010 = 12 Hz 0011 = 24 Hz 0100 = 48 Hz 0101 = 95 Hz 0110 = 191 Hz 0111 = 382 Hz 1000 = 763 Hz 1001 = 1.5 kHz 1010 = 3 kHz 1011 = 6 kHz 1100 = 12 kHz 1101 = 24 kHz 1110 = 49 kHz 1111 = 98 kHz	RW
	11:0	COMK2	Compensator coefficient that sets the zero frequency	RW
0x0A	15:14	OCPDEG	OCP deglitch time to ignore voltage spikes 00 = 1.6 µs 01 = 2.2 µs 10 = 3.0 µs 11 = 5.0 µs	RW
	13:12	OCPTH	Protection threshold for VFETOCP 00 = 250 mV 01 = 500 mV 10 = 750 mV 11 = 1000 mV	RW
	11	OVTH	Protection threshold for VOVLO 0 = 29 V 1 = 34 V	RW
	10	VREG_EN	0 = VREG enabled only when ENABLE is active 1 = VREG always enabled	RW
	9:0	LOOPGAIN	Sets the overall gain for the speed control loop	RW
0x0B	15:12	RSVD	Reserved	–
	11:0	SPEED	Speed command for internal register PWM mode	RW
0x2A	15:7	RSVD	Reserved	–
	6	RLOCK	Fault: rotor lockup 0 = Normal 1 = Fault detected	RW
	5	VMOV	Fault: VM overvoltage 0 = Normal 1 = Fault detected	RW
	4	CPFAIL	Fault: charge pump undervoltage 0 = Normal 1 = Fault detected (default on power up)	RW
	3	UVLO	Fault: VM undervoltage 0 = Normal 1 = Fault detected (default on power up)	RW
	2	OTS	Fault: overtemperature shutdown 0 = Normal 1 = Fault detected	RW
	1	CPOC	Fault: charge pump overcurrent 0 = Normal 1 = Fault detected	RW
	0	OCP	Fault: motor OCP 0 = Normal 1 = Fault detected	RW

9 Application and Implementation

9.1 Application Information

9.1.1 Internal Speed Control Loop Constraints

The DRV8308 device is a versatile speed controller and driver for small, 3-phase brushless motors. However, there are some limitations to its application.

The built-in speed control loop is designed to work optimally with motor electrical speeds from about 50 Hz up to 6.7 kHz. For an 8-pole motor, this translates into about 500 RPM up to more than 100000 RPM. For motors with higher pole counts, these speeds scale down; for lower pole counts, they scale up.

Operation is possible at slower or faster speeds, but speed control becomes less effective, especially if using the Hall sensors for speed feedback (as opposed to the FG input).

Typically, the speed loop is optimized (by setting the filter coefficients and gains) at one desired motor speed. Operation is possible with one set of parameters over a limited speed range (for example, 1000 RPM to 2000 RPM), However, operation over a very wide speed range requires different parameters. The use of the auto gain and auto advance features can extend the dynamic range up to 4×.

When using the SPI interface to program the registers, the parameters can be updated at any time, even while the motor is running. In this manner, a wider range of speeds can be accommodated by the speed loop.

When not using the internal speed loop (when controlling the motor using PWM input or register speed control), the limits imposed by the speed loop do not apply. An external speed control implementation (using a microcontroller, FPGA, or other logic) can essentially control the motor current directly.

However, if using sine commutation, there are limits to the minimum and maximum speed, which are dictated by the timers that are used to generate the commutation sequence. The commutation timer is a 25-bit timer clocked at 50 MHz; therefore, the longest time it can capture is 655 ms. This limits the slowest speed to about 1.5 Hz (or 23 RPM for an 8-pole motor). At the other extreme, there are 960 steps in each sine commutation cycle. To ensure that there is enough time for the steps, the maximum speed is that which generates 960 counts at 50 MHz, or 52 kHz. This corresponds to a maximum speed of 800000 RPM for an 8-pole motor.

When not using the internal speed loop and using 120° commutation (using all three Hall sensors), there are no speed limitations. Commutation is performed with combinational logic.

9.1.2 Hall Sensor Configurations and Connections

The Hall sensor inputs on the DRV8308 device are capable of interfacing with a variety of Hall sensors. Typically, a Hall element is used, which outputs a differential signal on the order of 100 mV. To use this type of sensor, the VREG5 regulator can be used to power the Hall sensor. Connections are as shown in Figure 25:

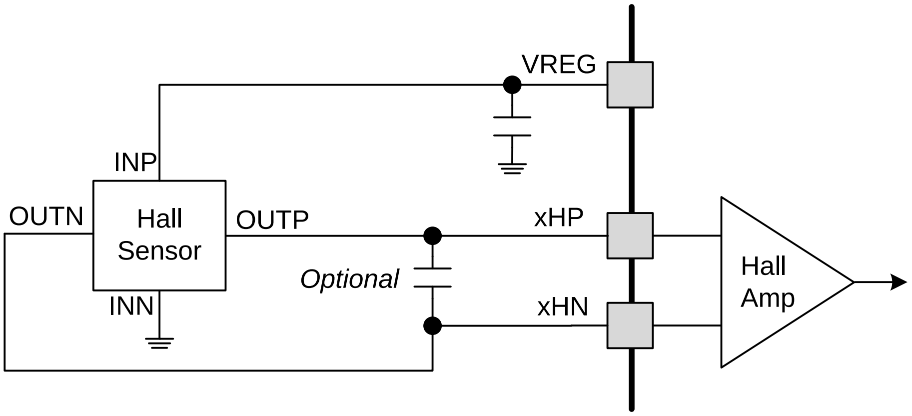


Figure 25.

Since the amplitude of the Hall sensor output signal is very low, often capacitors are placed across the Hall inputs to help reject noise coupled from the motor PWM. Typically capacitors from 1 to 10 nF are used.

Application Information (continued)

Some motors use digital Hall sensors with open-drain outputs. These sensors can also be used with the DRV8308 device, with the addition of a few resistors:

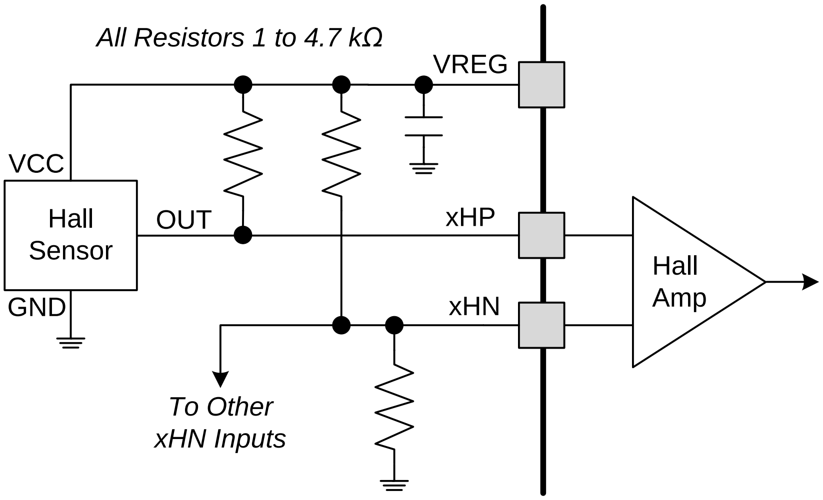


Figure 26.

The negative (xHN) inputs are biased to 2.5 V by a pair of resistors between VREG and ground. For open-collector Hall sensors, an additional pullup resistor to VREG is needed on the positive (xHP) input. Again, the VREG output can usually be used to supply power to the Hall sensors.

9.1.3 FG Amplifier Configurations and Connections

To improve speed control by providing a higher bandwidth speed feedback, often a magnetic pickup coil, commonly referred to as an FG generator, is used. This is typically implemented as a serpentine PCB trace on the motor PCB. This generates a low-level sine wave signal whose amplitude and frequency is proportional to the speed of the motor.

Since the FG trace is in close proximity to the motor coils, it is very susceptible to noise coupling from the PWM of the motor. Noise coupling into the FG circuit causes poor speed regulation, especially at low motor speeds. Startup is a particularly difficult situation, as the motor current is at a maximum, and the FG signal amplitude is low (in fact, 0 at the moment of startup). If noise couples into FG during startup, the speed loop interprets the noise as fast motor rotation, and lowers the PWM duty cycle. The result is slow startup of the motor. If this problem is suspected, looking at the FGOUT signal with an oscilloscope during startup should reveal it.

To address this, in addition to the resistors that set the gain of the FG amplifier (R1 and R2 in Figure 27), usually passive filter components are needed on the FG amplifier circuit.

Application Information (continued)

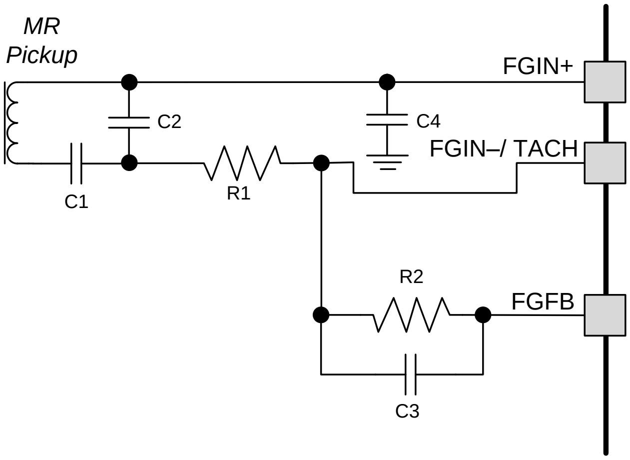


Figure 27.

Ideally, the user desires a large amount of rejection of the PWM frequency. However, the user needs to pass the frequency that corresponds to their fastest motor speed. As an example, a motor may put out 36 FG pulses per revolution. At 5000 RPM, this is a 3-kHz signal. If you operate the PWM at 25 kHz, you can set a single pole at 3 kHz and have significant rejection of the PWM frequency, and the higher harmonics of the PWM (which are typically more easily coupled) are rejected even more.

Because the amplitude of the FG signal also increases with higher motor speed, it is possible to set this pole at a much lower frequency than the maximum speed dictates. The optimal values need to be determined by testing on the actual motor.

This pole is set by C3 in Figure 27.

In addition to rejection of high frequency, the FG winding should be AC-coupled to the amplifier to prevent any issues with DC offsets. This capacitor (C1) must be large enough to allow the motor to start-up reliably, since the FG frequency and amplitude are very low at startup. Typically capacitors on the order of 100 nF to 1 µF are used here. The voltage is low, so a 6.3-V ceramic capacitor can be used.

Occasionally an additional small capacitor is used across the FG trace. This capacitor (C2 above) may not be needed, but it can help reject very high-frequency harmonics of the PWM (glitches). Capacitors between 330 and 2200 pF are typically used.

9.1.4 RESET and ENABLE Considerations

Since the ENABLE function doubles as a sleep (low-power shutdown) function, there are some important considerations when asserting and deasserting ENABLE and RESET.

While the motor driver is enabled, the deassertion of ENABLE initiates a stop-and-power-down sequence. This sequence starts by disabling the motor (either braking or coasting depending on the BRKMOD bit), and waiting for rotation to stop. After rotation is stopped for 1 s (as determined by the absence of transitions on FGOUT), the internal circuitry is powered-down, the V5 regulator and power switch are disabled, and internal clocks are stopped.

In this low-power sleep state, the serial interface may still be used to read or write registers. All other logic is disabled.

After this stop-and-power-down sequence has been initiated (by deasserting the ENABLE terminal for at least 1.2 µs, or by changing the state of the ENPOL bit), the sequence continues to completion, regardless of the state of ENABLE. If ENABLE is immediately returned to the active state, the motor slows and stops for 1 s, at which point it starts again.

If RESET is asserted during power-down (at any time after the deassertion of ENABLE is recognized), it is acted upon when ENABLE is again asserted, and the part powers-up.

Application Information (continued)

If RESET is asserted when ENABLE is active, the motor is stopped similar to the sequence when ENABLE is deasserted. After it is stopped for 1 s, all internal registers are reloaded with the value contained in OTP memory, faults are cleared, and internal states (that is, the speed loop datapath) are initialized. The motor remains disabled until RESET is deasserted.

RESET and ENABLE may be connected together (if the ENPOL bit in OTP memory is programmed so that ENABLE is active low). When both signals are low, the motor is enabled; when both signals are high, the motor is disabled. As soon as the signals are returned to high, all registers are reloaded from OTP memory, faults are cleared, and the motor starts.

10 Power Supply Recommendations

The DRV8308 device is designed to operate from an input voltage supply range between 8.5 and 32 V. This supply should be well regulated. TI recommends to use a 47-µF bulk capacitor to minimize transients on the supply.

11 Layout

11.1 Layout Guidelines

For VM, place 0.1-µF bypass capacitor close to the device. Take care to minimize the loop formed by the bypass capacitor connection from VM to GND.

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8308RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8308	Samples
DRV8308RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8308	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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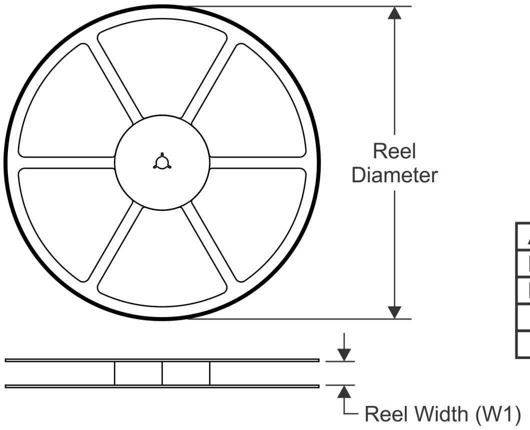
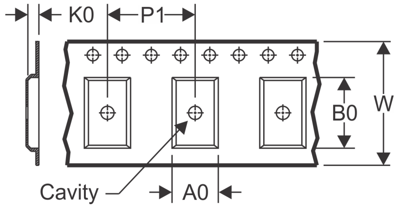
TAPE AND REEL INFORMATION

REEL DIMENSIONS

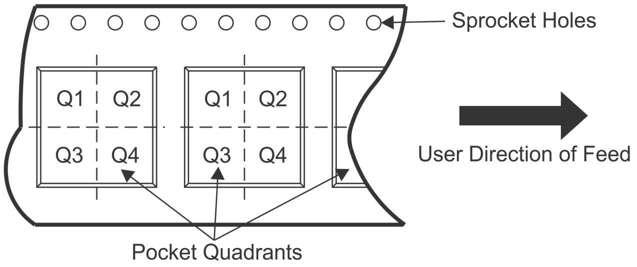


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

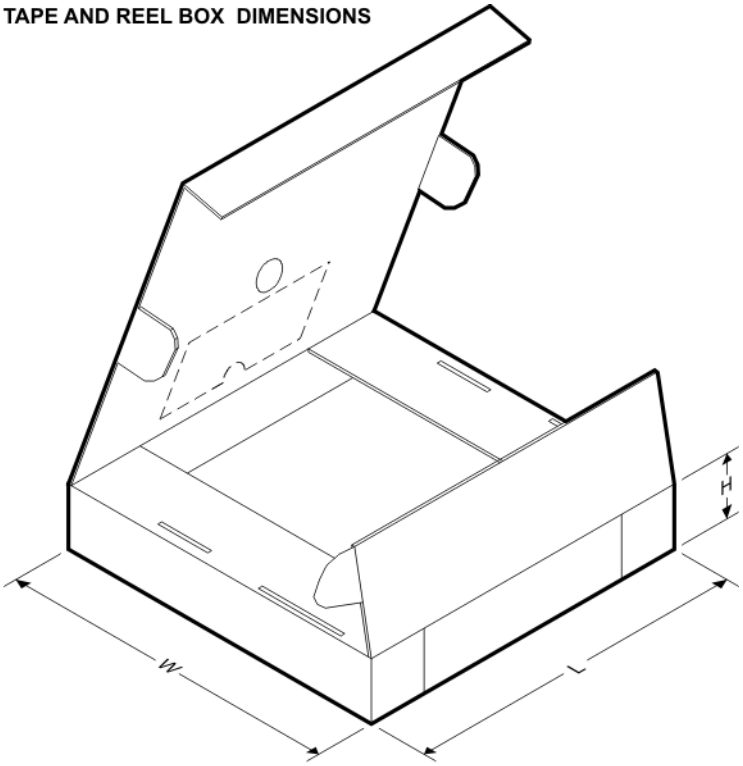
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8308RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
DRV8308RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

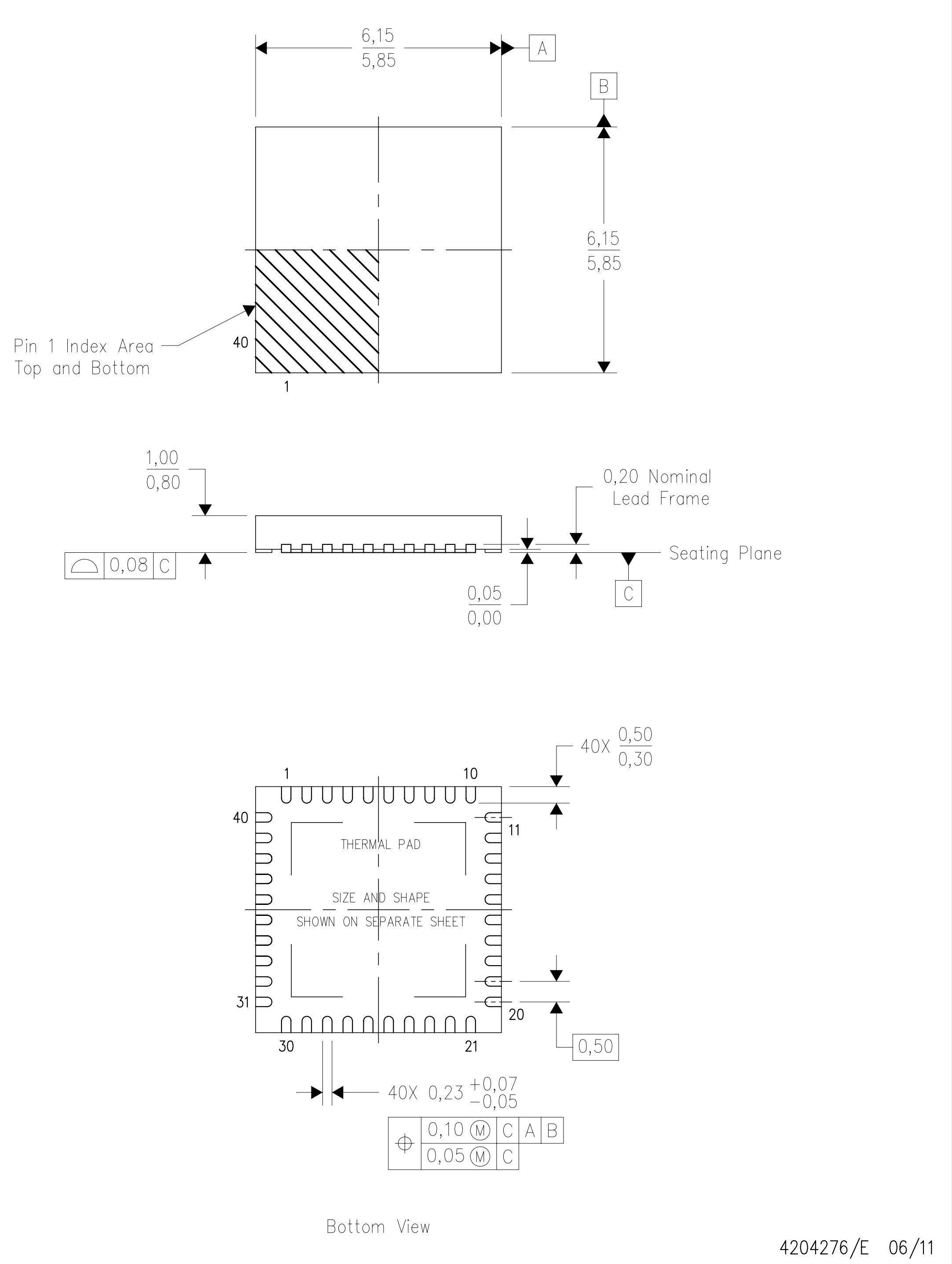
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8308RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DRV8308RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Package complies to JEDEC MO-220 variation VJJD-2.

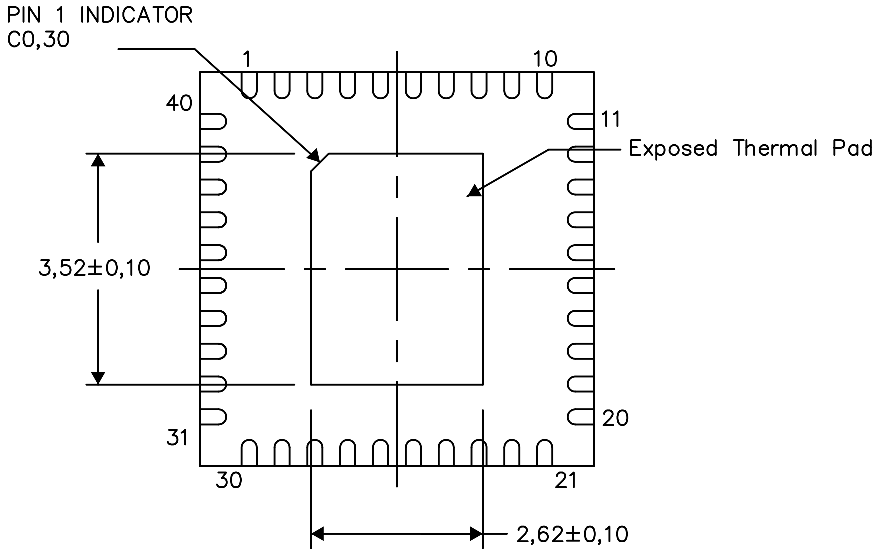
RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



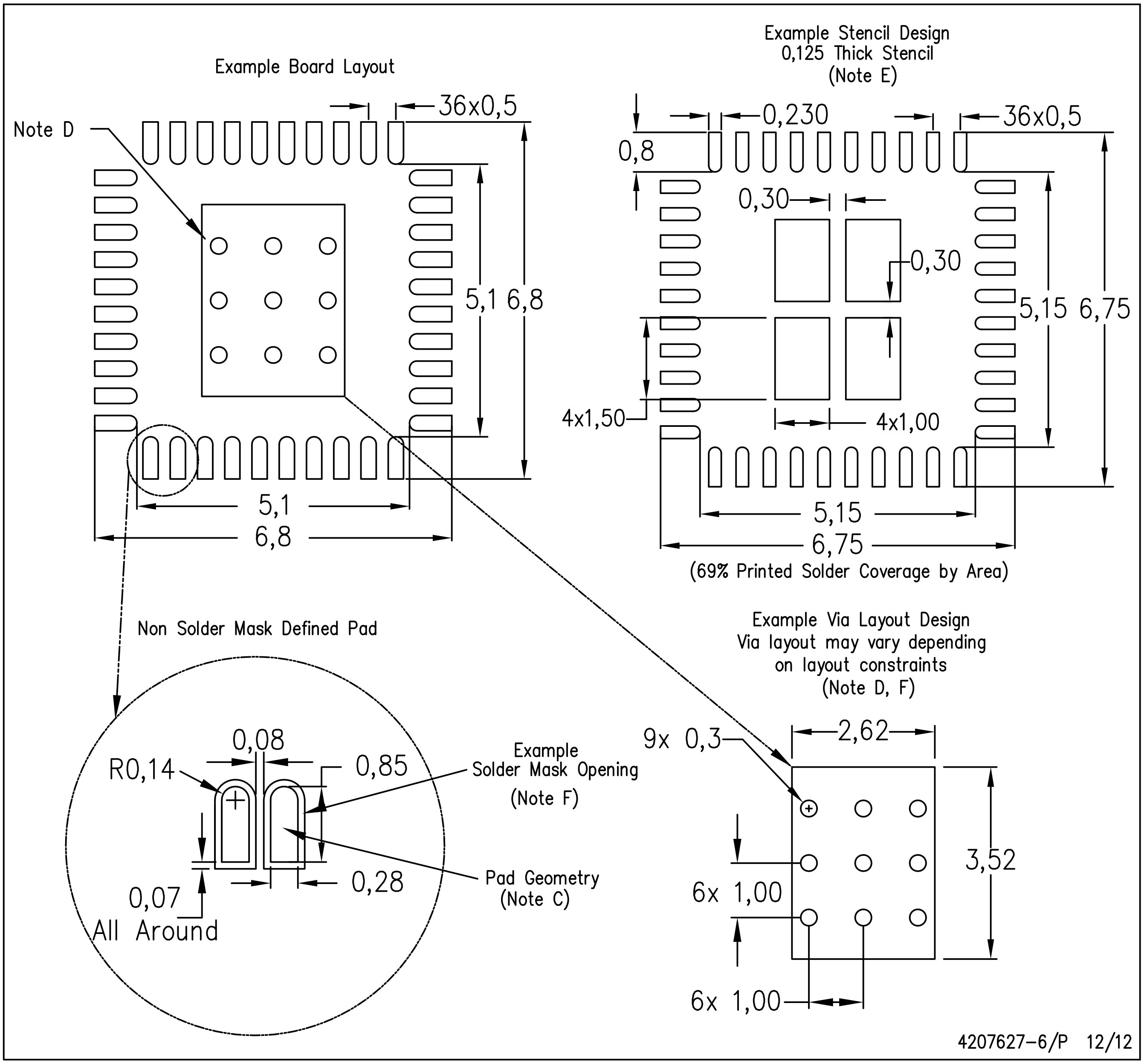
Bottom View

Exposed Thermal Pad Dimensions

4206355-9/V 04/14

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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