PRODUCT BULLETIN
Generic Copy

ISSUE DATE:	05-Jun-2013
NOTIFICATION:	15437
TITLE:	SGTL5000 Internal VDDD No Startup Issue
EFFECTIVE DATE:	06-Jun-2013

DEVICE(S)

MPN
SGTL5000XNAA3
SGTL5000XNAA3R2
SGTL5000XNLA3
SGTL5000XNLA3R2

AFFECTED CHANGE CATEGORIES

- DEVICE SPECIFICATION / ERRATA

DESCRIPTION OF CHANGE

Issue:
On some very rare combinations of parts and application boards, and on a very small percentage of those rare part/board combinations, sometimes the VDDD internal regulator does not start up after IC power-up. This can occur at any VDDIO and VDDA voltage level, and on either the QFN20 or QFN32 part. The failure is a function of board design and the slew rates of the power supplies, VDDIO and VDDA. The failure does not occur if an external regulator is used to supply VDDD.

Result:
The most noticeable symptom is that no IC communication/control occurs, and that the I2C bus lines are held in a low state. Power must be cycled to attempt another power-up, and to attempt to regain IC communication. Please note that the same applies for SPI communication.

Workarounds:

New Designs
Use an external supply in the system or a separate regulator to supply VDDD. This VDDD supply must be between 1.1V and 2.0V, and must source at least 11mA of current. A 0.1uF cap should also be added from VDDD to ground when VDDD is supplied externally. In order to save power, LINREG_D_POWERUP, LINREG_SIMPLE_POWERUP, and STARTUP_POWERUP bits in register 0x0030/CHIP_ANA_POWER should be cleared after IC power-up and after the application of the external VDDD voltage. If power savings is not a

concern, this software change is not required. The preferred supply sequencing is VDDIO/VDDA (doesn't matter which comes first) and then VDDD.

Existing Designs
For existing designs, if you have not experienced the issue to date, you likely will not. As stated previously, the issue requires the right combination of application board and part, and the right combination is very rare. If you are not planning a new board design, you can decrease the likelihood of seeing the issue by ramping both VDDIO and VDDA up in less than 1ms. If VDDIO and VDDA are separate supplies, ramp VDDIO up first. Any "soft-start" supply mechanisms for VDDIO/VDDA should be disabled, and any large caps on VDDIO/VDDA that aren't absolutely necessary should be removed, as long as there's no adverse effect on product performance.

If a new board pass is planned, please follow the steps in the "New Designs" section and use an external VDDD, as the external VDDD fix is the only solution that is guaranteed to solve the issue 100% of the time. Please note that the potential failure rate of an existing design in the field cannot be determined.

The updated SGTL5000 datasheet is attached to this notice and can be found at:
http://www.freescale.com/files/analog/doc/data_sheet/SGTL5000.pdf?fpsp=1

REASON FOR CHANGE

The VDDD internal regulator might not start up on a small percentage of part and board combinations, a small percentage of the time.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

There is some impact to the device function and reliability. The device might not function as expected some of the time if the described workaround is not implemented.

NOTE:
THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a Service Request

For sample inquiries - please go to www.freescale.com

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):

External attachment(s) FOR this notification can be viewed AT:
15437_Freescale_Semiconductor_Technical_Data_SGTL5000_Rev_5.0.pdf

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