PRODUCT BULLETIN
Generic Copy

ISSUE DATE:	25-Nov-2013
NOTIFICATION:	15928
TITLE:	KINETIS K SERIES 50 MHZ - 1N89E ERRATA UPDATE
EFFECTIVE DATE:	26-Nov-2013

DEVICE(S)

MPN
MK11DN512VLK5
MK11DN512VMC5
MK11DX128VLK5
MK11DX128VMC5
MK11DX256VLK5
MK11DX256VMC5
MK12DN512VLH5
MK12DN512VLK5
MK12DN512VMC5
MK12DX128VLF5
MK12DX128VLH5
MK12DX128VLK5
MK12DX128VMC5
MK12DX256VLF5
MK12DX256VLH5
MK12DX256VLK5
MK12DX256VMC5
MK21DN512VLK5
MK21DN512VMC5
MK21DX128VLK5
MK21DX128VMC5
MK21DX256VLK5
MK21DX256VMC5
MK22DN512VLH5
MK22DN512VLK5
MK22DN512VMC5
MK22DX128VLF5
MK22DX128VLH5
MK22DX128VLK5
MK22DX128VMC5
MK22DX256VLF5
MK22DX256VLH5
MK22DX256VLK5
MK22DX256VMC5
PK12DN512VLH5
PK12DX256VLF5

PK21DN512VLK5
PK21DN512VMC5
PK21DX128VMC5
PK21DX256VLK5
PK21DX256VMC5
PK22DN512VLH5
PK22DN512VLK5
PK22DN512VMC5
PK22DX256VLF5
PK22DX256VLH5
PK22DX256VLK5
PK22DX256VMC5

AFFECTED CHANGE CATEGORIES

- ERRATA

DESCRIPTION OF CHANGE

The 1N89E mask set errata documentation has been updated to include additional errata that have been identified.

The updated errata documentation is attached to this notice and can be found at http://cache.freescale.com/files/microcontrollers/doc/errata/KINETIS_1N89E.pdf?fpsp=1&WT_TYPE=Errata&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation

The following errata have been added to this update:

ID Errata Title
6804 CJTAG: Performing a mode change from Standard Protocol to Advanced Protocol may reset the CJTAG.
6939 Core: Interrupted loads to SP can cause erroneous behavior
4710 FTM: FTMx_PWMLOAD register does not support 8-/16-bit accesses
6484 FTM: The process of clearing the FTMx_SC[TOF] bit does not work as expected under a certain condition when the FTM counter reaches FTM_MOD value.
6573 JTAG: JTAG TDO function on the PTA2 disables the pull resistor
7027 UART: During ISO-7816 T=0 initial character detection invalid initial characters are stored in the RxFIFO
7028 UART: During ISO-7816 initial character detection the parity, framing, and noise error flags can set
6472 UART: ETU compensation needed for ISO-7816 wait time (WT) and block wait time (BWT)
7029 UART: In ISO-7816 T=1 mode, CWT interrupts assert at both character and block boundaries
7090 UART: In ISO-7816 mode, timer interrupts flags do not clear
7031 UART: In single wire receive mode UART will attempt to transmit if data is written to UART_D
7091 UART: UART_S1[NF] and UART_S1[PE] can set erroneously while UART_S1[FE] is set
7092 UART: UART_S1[TC] is not cleared by queuing a preamble or break character
6933 eDMA: Possible misbehavior of a preempted channel when using continuous link mode

REASON FOR CHANGE

The errata documentation for 1N89E mask set has been updated.

ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)

No changes have been made to the current production device. The errata describe existing conditions identified on current production devices. There are potential hardware and/or software implications to customers.

NOTE:
THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a Service Request

For sample inquiries - please go to www.freescale.com

QUAL DATA AVAILABILITY DATE: 24-Oct-2013

QUALIFICATION STATUS: N/A

QUALIFICATION PLAN:

N/A

RELIABILITY DATA SUMMARY:

N/A

ELECTRICAL CHARACTERISTIC SUMMARY:

N/A

CHANGED PART IDENTIFICATION:

N/A

ATTACHMENT(S):
External attachment(s) FOR this notification can be viewed AT:
15928_KINETIS_1N89E.pdf
