

**PRODUCT BULLETIN**

Generic Copy

**ISSUE DATE:** 16-Sep-2013  
**NOTIFICATION:** 15838  
**TITLE:** KINETIS K-SERIES 3N96B MASK SET ERRATA UPDATE  
**EFFECTIVE DATE:** 17-Sep-2013

**DEVICE(S)**

MPN
MK10FN1M0VLQ12
MK10FN1M0VMD12
MK10FX512VLQ12
MK10FX512VMD12
MK20FN1M0VLQ12
MK20FN1M0VMD12
MK20FX512VLQ12
MK20FX512VMD12
MK60FN1M0VLQ12
MK60FN1M0VLQ15
MK60FN1M0VMD12
MK60FN1M0VMD12R
MK60FN1M0VMD15
MK60FX512VLQ12
MK60FX512VLQ15
MK60FX512VMD12
MK60FX512VMD15
MK61FN1M0CAA12R
MK61FN1M0CCK12
MK61FN1M0VMD12
MK61FN1M0VMD15
MK61FN1M0VMJ12
MK61FN1M0VMJ15
MK61FX512VMD12
MK61FX512VMD15
MK61FX512VMJ12
MK61FX512VMJ15
MK70FN1M0VMJ12
MK70FN1M0VMJ15
MK70FX512VMJ12
MK70FX512VMJ15

**AFFECTED CHANGE CATEGORIES**

- ERRATA

## **DESCRIPTION OF CHANGE**

The Kinetis 3N96B errata documentation has been updated to include additional errata that have been identified.

The updated errata documentation is attached to this notice and can be found at:

[http://cache.freescale.com/files/microcontrollers/doc/errata/KINETIS\\_3N96B.pdf?fpsp=1&WT\\_TYPE=Errata&WT\\_VENDOR=FREESCALE&WT\\_FILE\\_FORMAT=pdf&WT\\_ASSET=Documentation](http://cache.freescale.com/files/microcontrollers/doc/errata/KINETIS_3N96B.pdf?fpsp=1&WT_TYPE=Errata&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation)

The following errata have been added to the 3N96B errata documentation:

e7166 - SOC: SDHC, NFC, USBOTG, and cache modules are not clocked correctly in low-power modes

e6484 - FTM: The process of clearing the FTMx\_SC[TOF] bit does not work as expected under a certain condition when the FTM counter reaches FTM\_MOD value

e7027 - UART: During ISO-7816 T=0 initial character detection invalid initial characters are stored in the RxFIFO

e7092 - UART: UART\_S1[TC] is not cleared by queuing a preamble or break character

e7028 - UART: During ISO-7816 initial character detection the parity, framing, and noise error flags can set

e7031 - UART: In single wire receive mode UART will attempt to transmit if data is written to UART\_D

e7091 - UART: UART\_S1[NF] and UART\_S1[PE] can set erroneously while UART\_S1[FE] is set

e7029 - UART: In ISO-7816 T=1 mode, CWT interrupts assert at both character and block boundaries

e7090 - UART: In ISO-7816 mode, timer interrupts flags do not clear

e6940 - Core: VDIV or VSQRT instructions might not complete correctly when very short ISRs are used

e6939 - Core: Interrupted loads to SP can cause erroneous behavior

e6934 - SDHC: Issues with card removal/insertion detection

e6933 - eDMA: Possible misbehavior of a preempted channel when using continuous link mode

## **REASON FOR CHANGE**

The errata document for the Kinetis 3N96B mask set has been updated.

## **ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)**

No changes have been made to the current production device. The errata describe existing conditions identified on current production devices. There are potential hardware and/or software implications to customers.

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### **NOTE:**

THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a [Service Request](#)

For sample inquiries - please go to [www.freescale.com](http://www.freescale.com)

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**QUAL DATA AVAILABILITY DATE:** 21-Aug-2013

**QUALIFICATION STATUS:** COMPLETED

**QUALIFICATION PLAN:**

N/A

**RELIABILITY DATA SUMMARY:**

N/A

**ELECTRICAL CHARACTERISTIC SUMMARY:**

N/A

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**CHANGED PART IDENTIFICATION:**

N/A

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**ATTACHMENT(S):**

External attachment(s) FOR this notification can be viewed AT:

[15838\\_KINETIS\\_3N96B\\_08072013.pdf](#)

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