1.35V Automotive DDR3L SDRAM Data Sheet Addendum

MT41K512M4 – 64 Meg x 4 x 8 banks
MT41K256M8 – 32 Meg x 8 x 8 banks
MT41K128M16 – 16 Meg x 16 x 8 banks

Description

The 1.35V DDR3L SDRAM device is a low-voltage version of the 1.5V DDR3 SDRAM device. Unless stated otherwise, the DDR3L SDRAM device meets the functional and timing specifications listed in the equivalent density standard or automotive DDR3 SDRAM data sheet located on www.micron.com.

Features

- $V_{DD} = V_{DDQ}$ = 1.35V (1.283–1.45V)
- Backward-compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of 0°C to +95°C
  - 64ms, 8192-cycle refresh at 0°C to +85°C
  - 32ms at +85°C to +95°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration
- AEC-Q100
- PPAP submission
- 8D response time

Options / Marking

Options	Marking
• Configuration	
– 512 Meg x 4	512M4
– 256 Meg x 8	256M8
– 128 Meg x 16	128M16
• FBGA package (Pb-free) – x4, x8	
– 78-ball (8mm x 10.5mm) Rev. K	DA
• FBGA package (Pb-free) – x16	
– 96-ball FBGA (8mm x 14mm) Rev. K	JT
• Timing – cycle time	
– 1.25ns @ CL = 11 (DDR3-1600)	-125
– 1.5ns @ CL = 9 (DDR3-1333)	-15E
– 1.875ns @ CL = 7 (DDR3-1066)	-187E
• Special Options	
– Product Longevity Program (PLP)	X
– Automotive certification	A
• Operating temperature	
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
– Automotive (–40°C ≤ T_C ≤ +105°C)	AT
• Revision	:K

Table 1: Key Timing Parameters

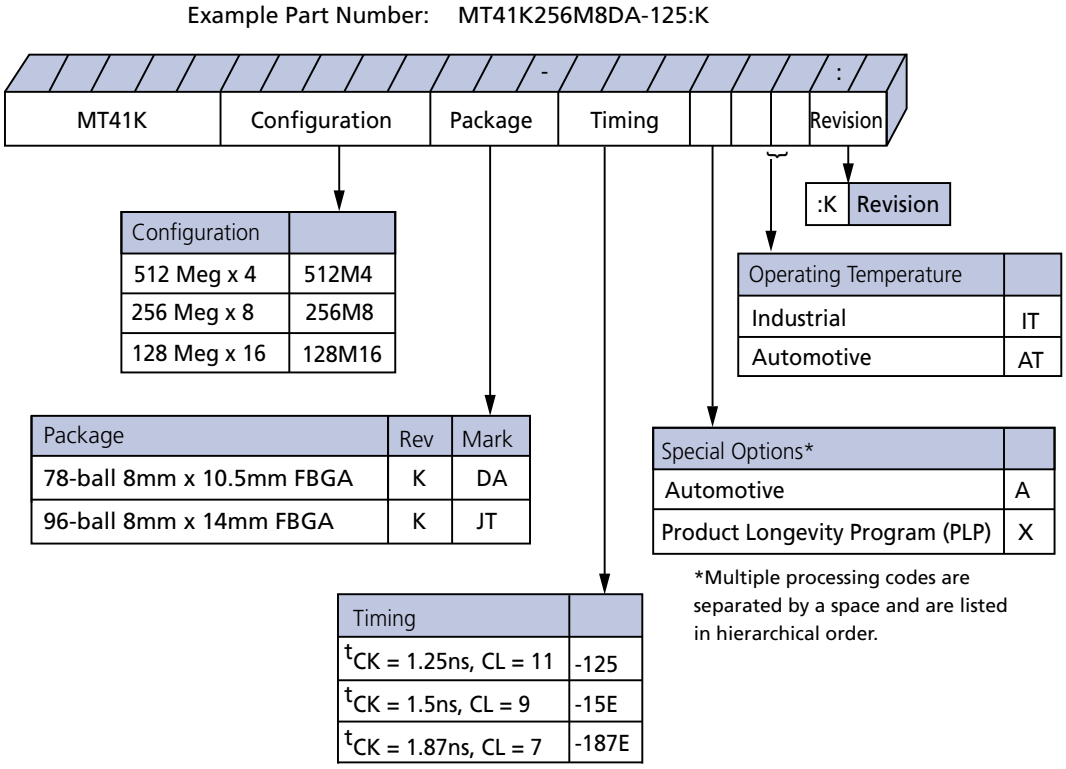
Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-125[1, 2]	1600	11-11-11	13.75	13.75	13.75
-15E[1]	1333	9-9-9	13.5	13.5	13.5
-187E	1066	7-7-7	13.1	13.1	13.1

Notes: 1. Backward compatible to 1066, CL = 7 (-187E).
2. Backward compatible to 1333, CL = 9 (-15E).

Table 2: Addressing

Parameter	512 Meg x 4	256 Meg x 8	128 Meg x 16
Configuration	64 Meg x 4 x 8 banks	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	32K A[14:0]	32K A[14:0]	16K A[13:0]
Bank address	8 BA[2:0]	8 BA[2:0]	8 BA[2:0]
Column address	2K A[11, 9:0]	1K A[9:0]	1K A[9:0]

Figure 1: DDR3L Part Numbers



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Revision History

Rev. A – 03/14

- Initial release based on the 1.35V Automotive DDR3L SDRAM, Rev. A 06/13 data sheet

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.