XR76115

PowerBlox™

15A Synchronous Step Down COT Regulator

General Description

The XR76115 is a synchronous step-down regulator combining the controller, drivers, bootstrap diode and MOSFETs in a single package for point-of-load supplies. The XR76115 has a load current rating of 15A. A wide 5V to 22V input voltage range allows for single supply operation from industry standard 5V, 12V and 19.6V rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR76115 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation, simplifying circuit implementation and reducing overall component count. The control loop also provides 0.25% load and 0.12% line regulation and maintains constant operating frequency. A selectable power saving mode, allows the user to operate in discontinuous mode (DCM) at light current loads thereby significantly increasing the converter efficiency.

A host of protection features, including over-current, over-temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XR76115 is available in a RoHS-compliant, green/halogen-free space-saving QFN 6x6mm package.

FEATURES

- 15A Capable Step Down Regulator
  - 4.5V to 5.5V Low V_{IN} Operation
  - 5V to 22V Wide Single Input Voltage
  - ≥0.6V Adjustable Output Voltage
- Controller, drivers, bootstrap diode and MOSFETs integrated in one package
- Proprietary Constant On-Time Control
  - No Loop Compensation Required
  - Ceramic Output Cap. Stable operation
  - Programmable 200ns-2µs On-Time
  - Quasi Constant 200kHz-800kHz Freq.
  - Selectable CCM or CCM/DCM Operation
- Precision Enable and Power-Good Flag
- Programmable Soft-start
- 6x6mm 37-pin QFN Package

APPLICATIONS

- Distributed Power Architecture
- Point-of-Load Converters
- Power Supply Modules
- FPGA, DSP, and Processor Supplies
- Base Stations, Switches/Routers, and Servers

Typical Application

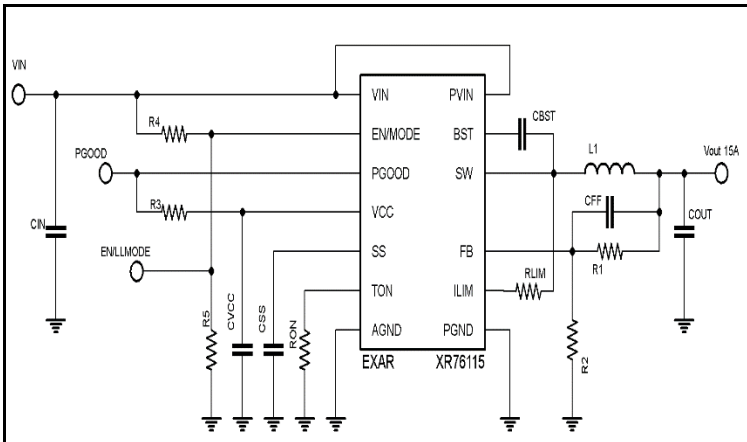


Figure 1: XR76115 Application Diagram

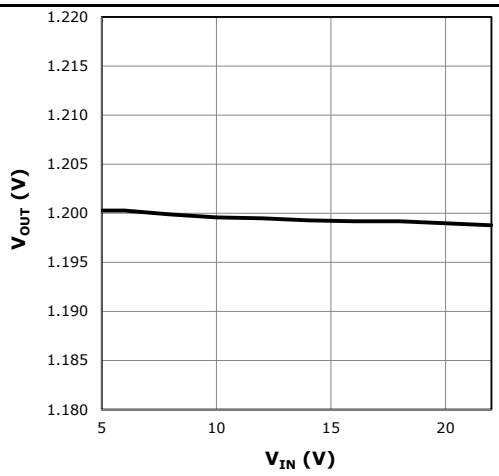


Figure 2: XR76115 line regulation

©2013-2014 Exar Corporation

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN} ..... -0.3V to 25V
V_{CC} ..... -0.3V to 6.0V
BST ..... -0.3V to 31V[1]
BST-SW ..... -0.3V to 6V
SW, I_{LIM} ..... -1V to 25V[1,2]
All other pins..... -0.3V to V_{CC}+0.3V
Storage Temperature ..... -65°C to 150°C
Junction Temperature..... 150°C
Power Dissipation..... Internally Limited
Lead Temperature (Soldering, 10 sec)..... 300°C
ESD Rating (HBM - Human Body Model) 2kV

Operating Ratings

PV_{IN} ..... 3V to 22V
V_{IN} ..... 4.5V to 22V
V_{CC} ..... 4.5V to 5.5V
SW, I_{LIM} ..... -1V to 22V[2]
PGOOD, V_{CC}, T_{ON}, SS, EN..... -0.3V to 5.5V
Switching Frequency ..... 200kHz-800kHz[3]
Junction Temperature Range (T_J)..... -40°C to 125°C
XR76115 Package Power Dissipation max at 25°C 5.2W
XR76115 JEDEC51 Package Thermal Resistance θ_{JA}..... 19°C/W

Note 1: No external voltage applied
Note 2: SW pin's DC range is -1V, transient is -5V for less than 50ns
Note 3: Recommended

Ordering Information

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1
XR76115EL-F	-40°C≤T_J≤+125°C	76115EL YYWW XXXXXXX	6x6mm QFN	Bulk	RoHS Compliant Halogen Free
XR76115ELMTR-F				250/Tape & Reel	
XR76115ELTR-F				3k/Tape & Reel	
XR76115EVB		XR76115 Evaluation Board			

"YY" = Year – "WW" = Work Week – "XXXXXXX" = Lot Number; when applicable.

Electrical Characteristics

Specifications are for Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN}=12V

Parameter	Min.	Typ.	Max.	Units		Conditions
Power Supply Characteristics						
V_{IN}, Input Voltage Range	5	12	22	V	•	V_{CC} regulating
	4.5	5.0	5.5			V_{CC} tied to V_{IN}
I_{VIN}, V_{IN} supply current		0.7	1.3	mA	•	Not switching, V_{IN}=12V, V_{FB}=0.7V
I_{VCC}, V_{CC} Quiescent current		0.7	1.3	mA	•	Not switching, V_{CC}=V_{IN}=5V, V_{FB}=0.7V
I_{VIN}, V_{IN} supply current		11		mA		f=300kHz, R_{ON}=107k, V_{FB}=0.58V
I_{OFF}, Shutdown current		0.5		µA		Enable=0V, V_{IN}=12V, V_{IN}=PV_{IN}
Enable and Under-Voltage Lock-Out UVLO						
V_{IH_EN}, EN Pin Rising Threshold	1.8	1.9	2.0	V	•	
V_{EN_HYS}, EN Pin Hysteresis		50		mV		
V_{IH_EN}, EN Pin Rising Threshold for DCM/CCM operation	2.8	3.0	3.1	V	•	
V_{EN_HYS}, EN Pin Hysteresis		100		mV		
V_{CC} UVLO start threshold, rising edge	4.00	4.25	4.50	V	•	

© 2013-2014 Exar Corporation

Parameter	Min.	Typ.	Max.	Units		Conditions
V_{CC} UVLO Hysteresis		200		mV		
Reference voltage						
V_{REF}, Reference voltage	0.597	0.600	0.603	V		V_{IN}=5V-22V → V_{CC} regulating
	0.596	0.600	0.604	V		V_{IN}=4.5V-5.5V → V_{CC} tied to V_{IN}
	0.594	0.600	0.606	V	•	V_{IN}=5V-22V → V_{CC} regulating, V_{IN}=4.5V-5.5V → V_{CC} tied to V_{IN}
DC load regulation		±0.25		%		CCM operation, closed loop, applies to any C_{OUT}
DC Line regulation		±0.12		%		
Parameter	**Min.**	**Typ.**	**Max.**	**Units**		**Conditions**
Programmable Constant On-Time						
On-Time 1	1.66	1.95	2.24	µs	•	R_{ON}=140kΩ, V_{IN}=22V
f corresponding to On-Time 1	243	280	329	kHz		V_{IN}=22V, V_{OUT}=12V
Minimum Programmable On-Time		109		ns		R_{ON}=6.98kΩ, V_{IN}=22V
On-Time 2	205	245	279	ns	•	R_{ON}=6.98kΩ, V_{IN}=12V
f corresponding to On-Time 2	986	1122	1341	kHz		V_{OUT}=3.3V
f corresponding to On-Time 2	299	340	406	kHz		V_{OUT}=1.0V
On-Time 3	400	470	540	ns	•	R_{ON}=16.2kΩ, V_{IN}=12V
Minimum Off-Time		250	350	ns	•	
Diode Emulation Mode						
Zero crossing threshold		-2		mV		DC value measured during test
Soft-Start						
SS Charge current	-14	-10	-6	µA	•	
SS Discharge current	1	3		mA	•	Fault present
V_{CC} Linear Regulator						
V_{CC} Output Voltage	4.8	5.0	5.2	V	•	V_{IN}=6V to 22V, I_{load}=0 to 30mA
	4.51	4.7			•	V_{IN}=5V, I_{load}=0 to 20mA
Dropout Voltage	100	300	490	mV	•	I_{VCC}=30mA
Power Good Output						
Power Good Threshold	-10	-7.5	-5	%		
Power Good Hysteresis		2	4	%		
Power Good Sink Current	1	15		mA		
Protection: OCP, OTP, Short-Circuit						
Hiccup timeout		110		ms		
I_{LIM} pin source current	45	50	55	µA		
I_{LIM} current temperature coefficient		0.4		%/°C		
I_{LIM} comparator offset	-8	0	+8	mV	•	
Current limit blanking		100		ns		
Thermal shutdown threshold		150		°C		Rising temperature
Thermal Hysteresis		15		°C		
Feedback pin short-circuit threshold	50	60	70	%	•	Percent of V_{REF}, short circuit is active After PGOOD is up
Output Power Stage						
High-side MOSFET R_{DSON}		7	10	mΩ		V_{GS}=4.5V, I_{DS}=2A
Low-side MOSFET R_{DSON}		4	4.6	mΩ		V_{GS}=4.5V, I_{DS}=2A
Maximum Output Current	15			A	•	

© 2013-2014 Exar Corporation

Block Diagram

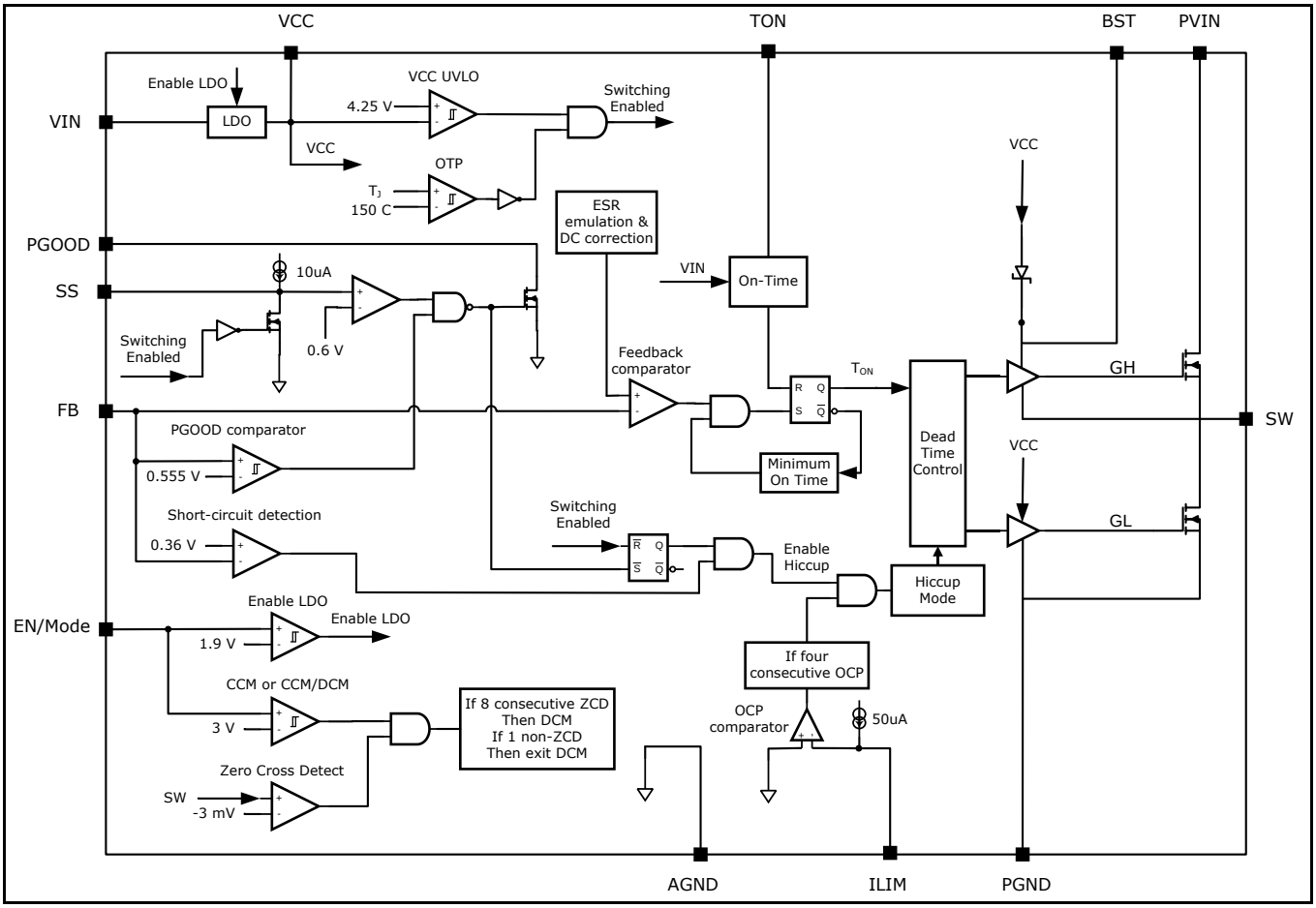


Figure 3: XR76115 Block Diagram

Pin Assignment

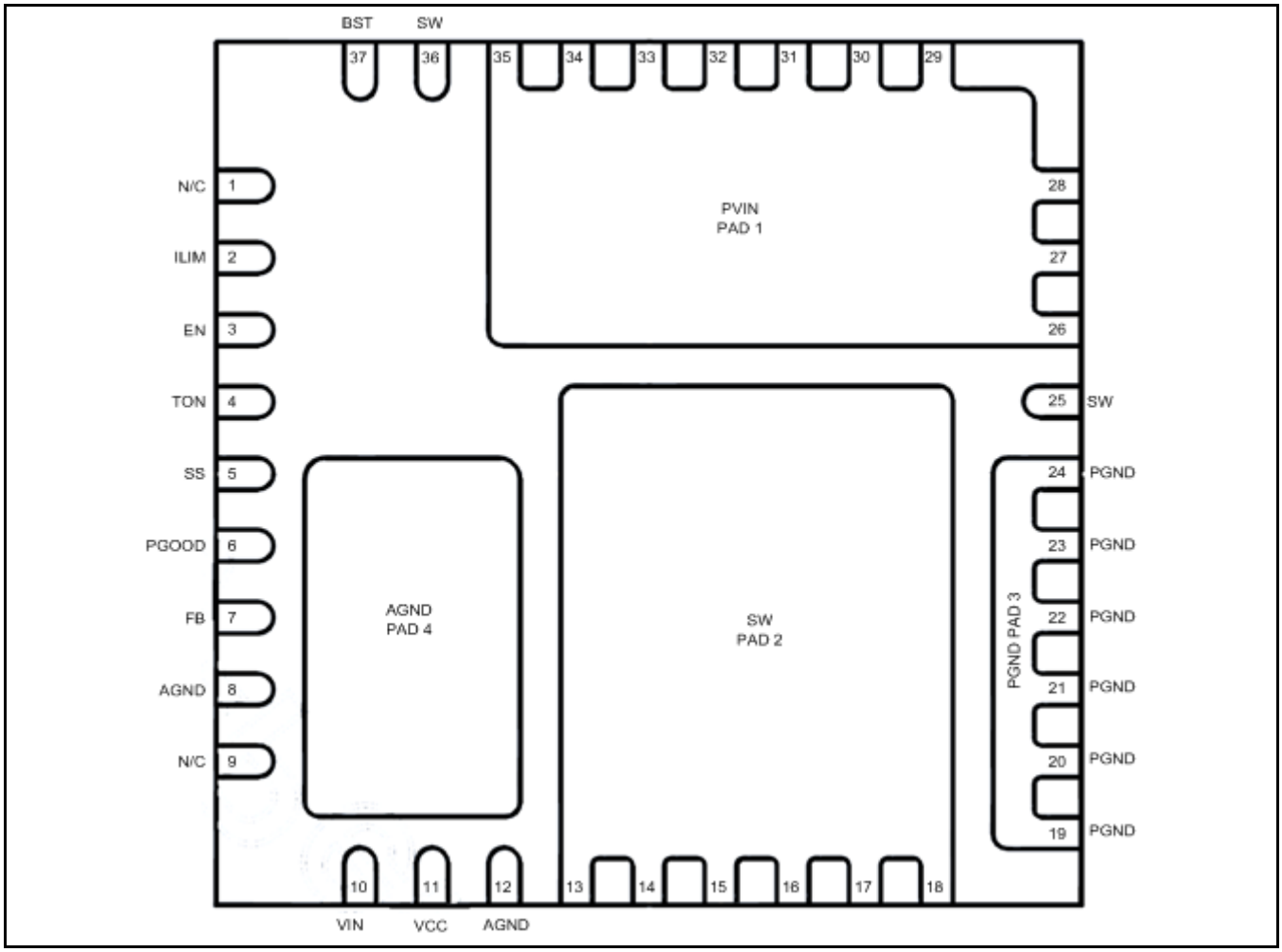


Figure 4: XR76115 Pin Assignment, top view

© 2013-2014 Exar Corporation

Pin Description

Name	Pin Number	Description
NC	1,9	Not connected.
ILIM	2	Over-current protection programming. Connect with a resistor to SW.
EN/MODE	3	Precision enable pin. Pulling this pin above 1.9V will turn the regulator on and it will operate in CCM. If the voltage is raised above 3.0V then the regulator will operate in DCM/CCM depending on load.
TON	4	Constant on-time programming pin. Connect with a resistor to AGND.
SS	5	Soft-Start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10uA internal source current.
PGOOD	6	Power-good output. This open-drain output is pulled low when V_{OUT} is outside the regulation.
FB	7	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and AGND in order to program V_{OUT}.
AGND	8, 12, AGND Pad	Signal ground for control circuitry. Connect AGND Pad with a short trace to pins 8 and 12.
VIN	10	Supply input for the regulator's LDO. Normally it is connected to PVIN.
VCC	11	The output of regulator's LDO. For operation using a 5V rail, VCC should be shorted to VIN.
SW	13-18, 25, 36, SW Pad	Switch node. Drain of the low-side N-channel MOSFET. Source of the high-side MOSFET is wire-bonded to the SW Pad.
PGND	19-24, PGND Pad	Ground of the power stage. Should be connected to the system's power ground plane. Source of the low-side MOSFET is wire-bonded to PGND Pad.
PVIN	26-35, PVIN Pad	Input voltage for power stage. Drain of the high-side N-channel MOSFET.
BST	37	High-side driver supply pin. Connect a 1uF bootstrap capacitor between BST and SW.

© 2013-2014 Exar Corporation

Typical Performance Characteristics

All data taken at V_{IN}=12V, V_{OUT}=1.2V, f=600kHz, T_A=25°C, No Air flow, Forced CCM, unless otherwise specified. Schematic and BOM from Applications Circuit section of this datasheet.

REGULATION

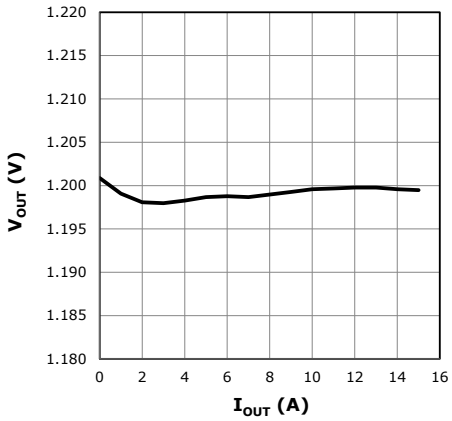


Figure 5: Load regulation, V_{IN}=12V

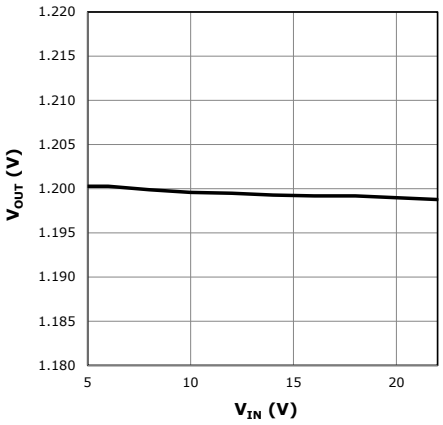


Figure 6: Line regulation, I_{OUT}=15A

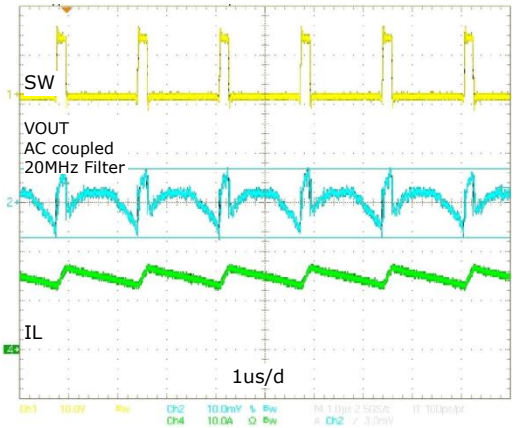


Figure 7: V_{OUT} ripple is 14mV at 15A

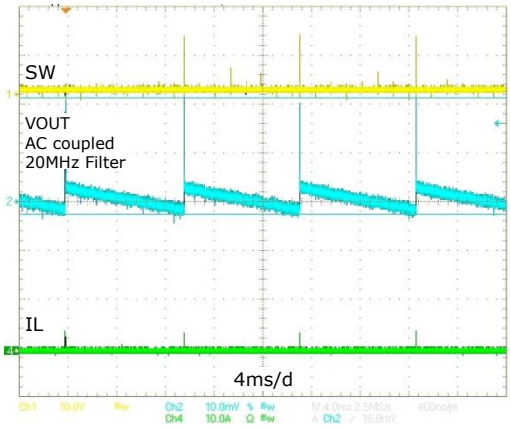


Figure 8: V_{OUT} ripple is 23mV at 0A, DCM

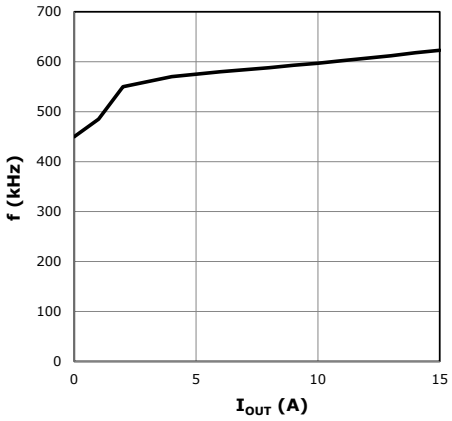


Figure 9: Frequency vs. I_{OUT}, Forced CCM

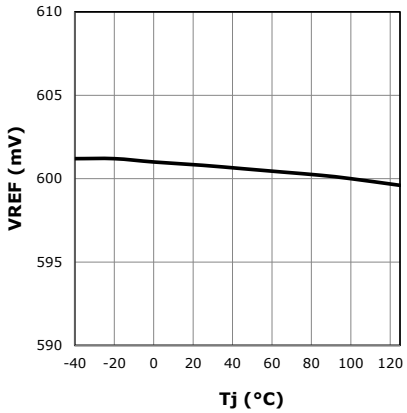


Figure 10: V_{REF} vs. temperature

© 2013-2014 Exar Corporation

Typical Performance Characteristics

All data taken at V_{IN}=12V, V_{OUT}=1.2V, f=600kHz, T_A=25°C, No Air flow, Forced CCM, unless otherwise specified. Schematic and BOM from Applications Circuit section of this datasheet.

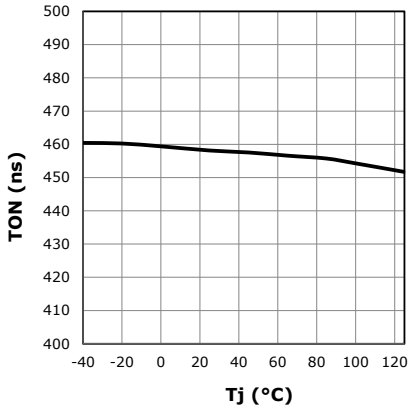


Figure 11: On-Time vs. temperature

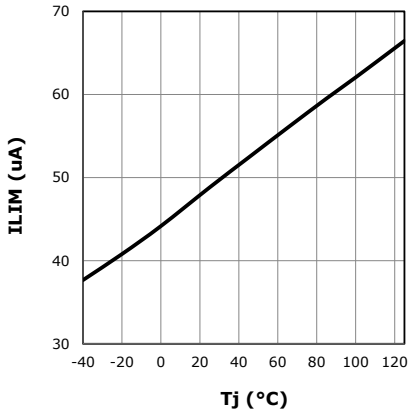


Figure 12: I_{LIM} vs. temperature

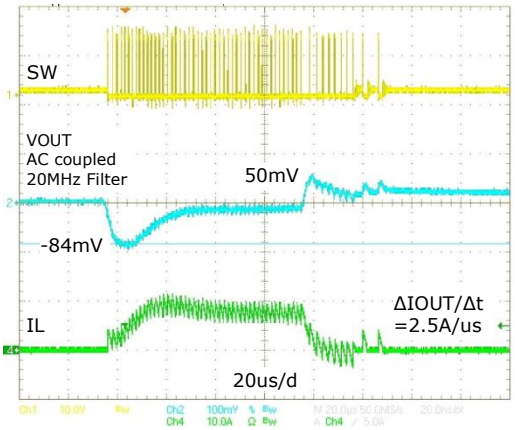


Figure 13: load step, DCM/CCM, 0A-7.5A-0A

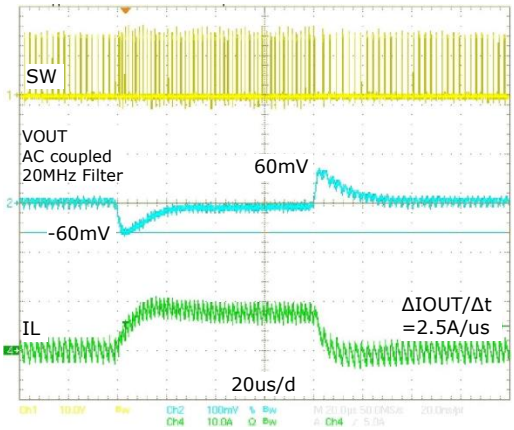


Figure 14: load step, Forced CCM, 0A-7.5-0A

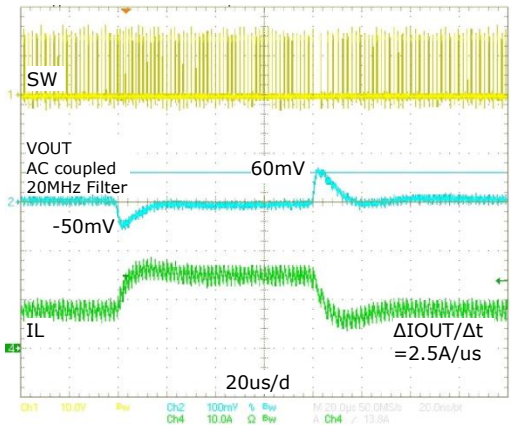


Figure 15: load step, Forced CCM, 7.5A-15A-7.5A

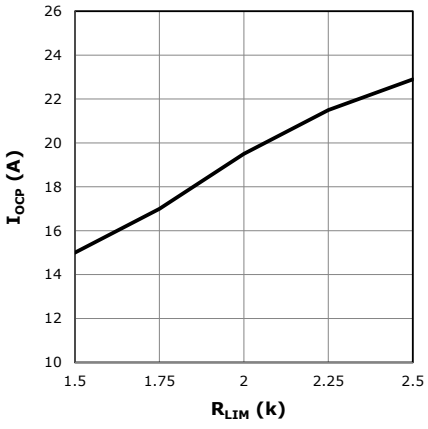


Figure 16: Typical I_{OCP} versus R_{LIM}

© 2013-2014 Exar Corporation

Powerup

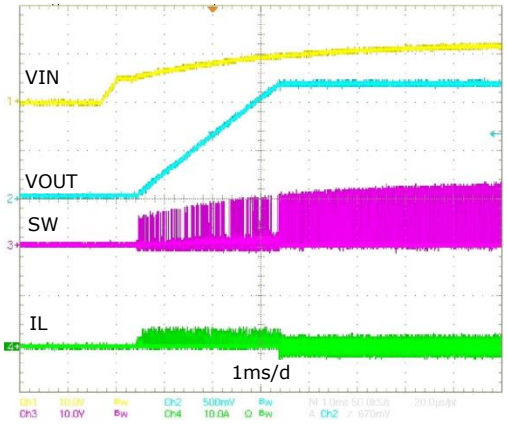


Figure 17: Powerup, Forced CCM, I_{OUT}=0A

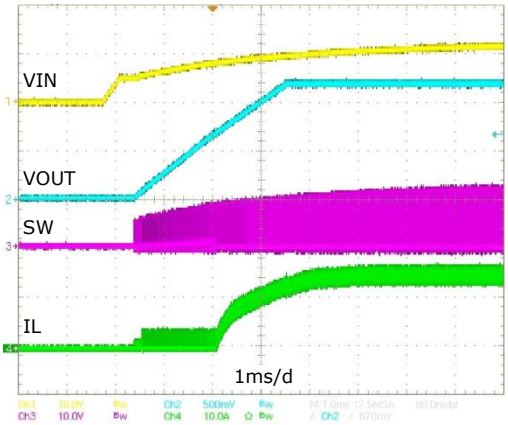


Figure 18: Powerup, Forced CCM, I_{OUT}=15A

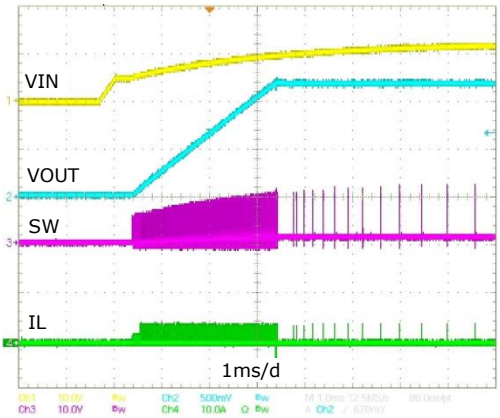


Figure 19: Powerup, DCM/CCM, I_{OUT}=0A

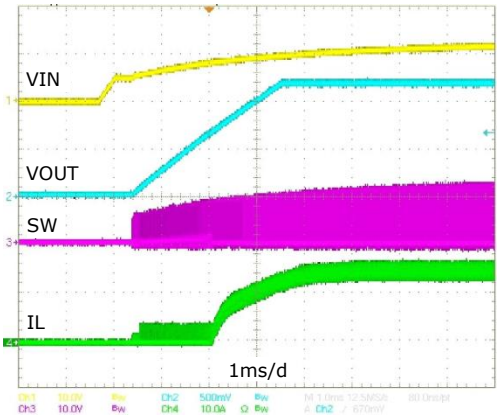


Figure 20: Powerup, DCM/CCM, I_{OUT}=15A

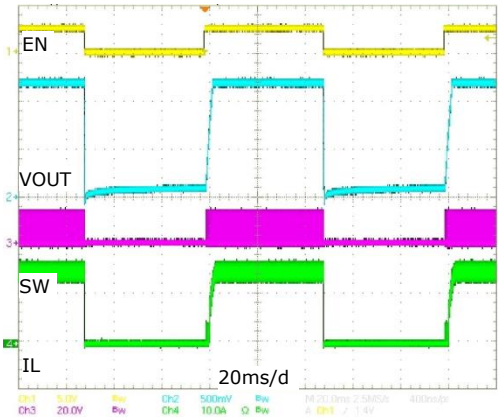


Figure 21: Enable turn on/turn off, 1.2V_{OUT}, 15A

Efficiency and Thermal Characteristics

$T_{AMBIENT}$=25°C, No Air flow, Inductor losses are included.

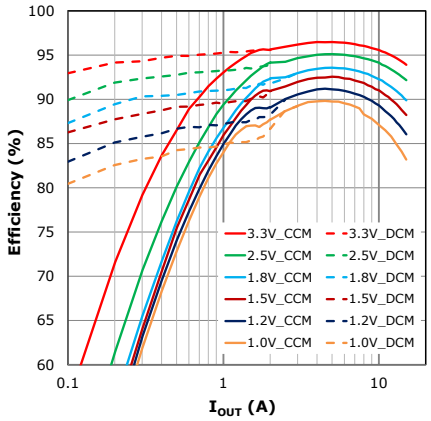


Figure 22: $5V_{IN}$, 600kHz, 0.47uH

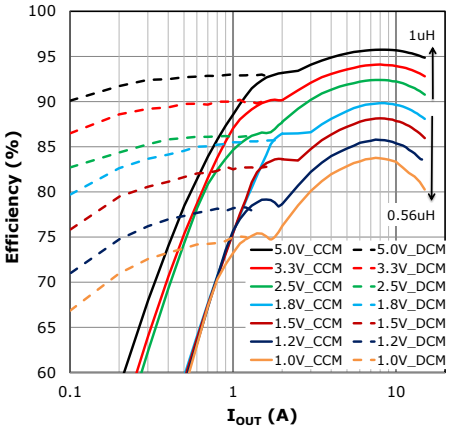


Figure 23: $12V_{IN}$, 600kHz

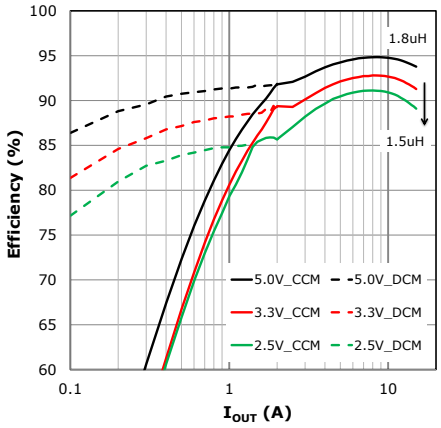


Figure 24: $22V_{IN}$, 400kHz

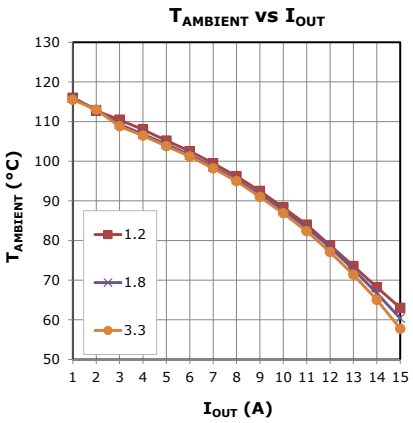


Figure 25: Package Thermal Derating, 12VIN

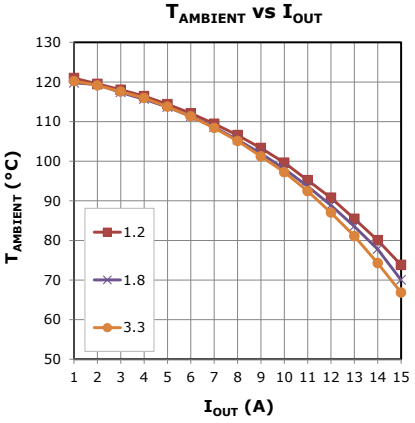


Figure 26: Package Thermal Derating, 5VIN

© 2013-2014 Exar Corporation

Detailed Operation

The XR76115 uses a synchronous step-down proprietary emulated current-mode Constant On-Time (COT) control scheme. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control allows the use of ceramic output capacitors.

Each switching cycle begins with the high-side (switching) FET turning on for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed the Minimum Off-Time. After the minimum off-time the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When VFB drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and allows for the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable/Mode

The EN/MODE pin accepts a tri-level signal that is used to control channel turn-on and turn-off. It also selects between two modes of operation: 'Forced CCM' and 'DCM/CCM'. If EN is pulled below 1.9V the regulator shuts down. A voltage between 1.9V and 3V selects the Forced CCM mode, which will run the converter in continuous conduction for all load currents. A voltage higher than 3V selects the DCM/CCM mode, which will run the converter in discontinuous conduction mode at light loads. DCM/CCM, which is based on diode emulation, is described below.

Diode Emulation Mode (DCM/CCM)

Diode Emulation Mode is designed to increase the converter efficiency at light loads. Light-load efficiency is increased by preventing negative inductor current. This is achieved by monitoring the inductor current valley (bottom) via SW and turning off the synchronous FET as inductor current I_L approaches zero. I_L is monitored indirectly by monitoring V_{SW} during the synchronous FET conduction period (i.e., $V_{SW}=I_L \times R_{DSON}$). If V_{SW} does not drop to -2mV the converter operates in continuous conduction mode as shown in Figure 27. If V_{SW} equals -2mV then a zero-crossing is detected (Figure 28). Eight consecutive zero-crossings activate the diode emulation mode. Then, on every subsequent switching cycle, GL is turned off when V_{SW} reaches -2mV (Figure 28). As I_{OUT} decreases further, discontinuous conduction ensues (Figure 29). The constant on-time delivers a fixed energy at the start of each switching cycle. The synchronous FET is turned off when V_{SW} drops to -2mV. Any remaining inductor energy is discharged through the FET's body diode. Now, because I_{OUT} is low, it takes longer for V_{OUT} to drop below regulation and trigger a new switching cycle. Hence switching frequency f decreases. This increases the efficiency at light loads.

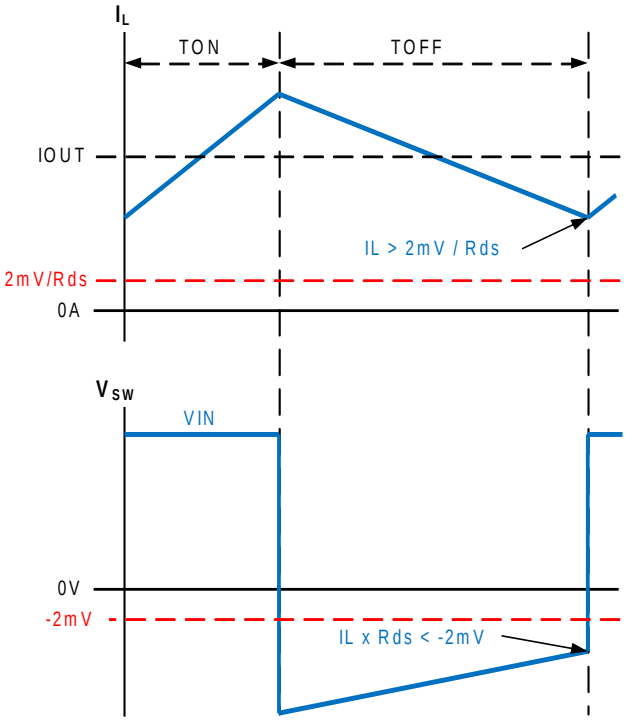


Figure 27: Continuous conduction during diode emulation

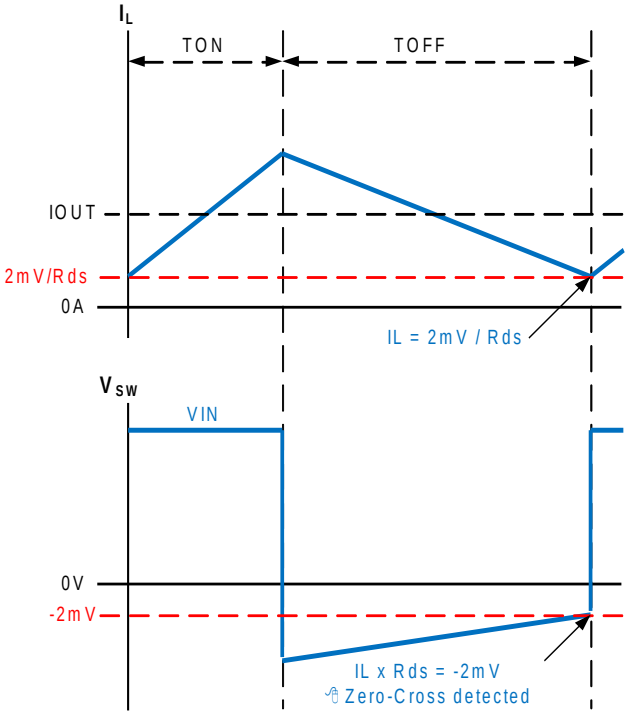


Figure 28: Zero-Crossing detection

© 2013-2014 Exar Corporation

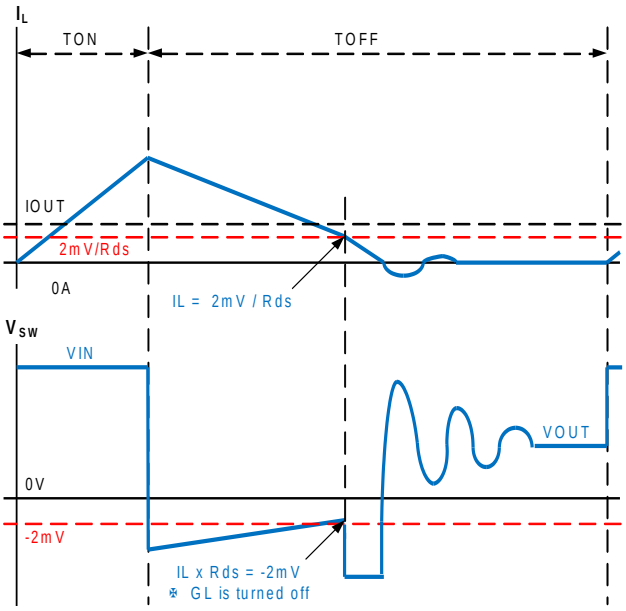


Figure 29: Discontinuous conduction during diode emulation

Programming the On-Time

The on-time T_{ON} is programmed via resistor R_{ON} according to following equation:

$$T_{ON} = \frac{(3.4 \times 10^{-10}) \times R_{ON}}{V_{IN}}$$

The required T_{ON} for a given application is calculated from:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f}$$

Therefore, R_{ON} can be selected based on the output voltage and desired switching frequency as follows:

$$R_{ON} = \frac{V_{OUT}}{(3.4 \times 10^{-10}) \times f}$$

Note that switching frequency f will increase somewhat, as a function of increasing load current and increasing losses (see Figure 9).

Figure 30 suggests resistance values for common output voltages and switching frequencies.

V_{OUT} [V]	R_{ON} [Ω] at 300kHz	R_{ON} [Ω] at 400kHz	R_{ON} [Ω] at 500kHz	R_{ON} [Ω] at 600kHz	R_{ON} [Ω] at 800kHz
3.3	32,353	24,265	19,412	16,176	12,132
2.5	24,510	18,382	14,706	12,255	9,191
1.8	17,647	13,235	10,588	8,824	6,618
1.5	14,706	11,029	8,824	7,353	5,515
1.2	11,765	8,824	7,059	5,882	4,412
1.0	9,804	7,353	5,882	4,902	3,676

Figure 30: R_{ON} resistances for common output voltages and frequencies

Over-Current Protection (OCP)

If the load current exceeds the programmed over-current I_{OCP} for four consecutive switching cycles, then the regulator enters the hiccup mode of operation. In hiccup mode the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The regulator will remain in hiccup mode until load current is reduced below the programmed I_{OCP}. In order to program over-current protection use the following equation:

$$R_{ILIM} = \frac{(I_{OCP} \times R_{DSON}) + 8mV}{I_{LIM}}$$

where:

R_{LIM} is resistor value for programming I_{OCP}

I_{OCP} is the over-current value to be programmed

R_{DSON}=4.6mΩ(maximum specification)

8mV is the OCP comparator offset

I_{LIM} is the internal current that generates the necessary OCP comparator threshold (use 45µA)

Note that I_{LIM} has a positive temperature coefficient of 0.4%/°C. This is meant to approximately match and compensate for positive temperature coefficient of the synchronous FET.

The above equation is for worst-case analysis and safeguards against premature OCP. Actual value of I_{OCP}, for a given R_{LIM}, will be higher than that predicted by the above equation. Typical I_{OCP} versus R_{LIM} is shown in Figure 16.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the regulator will enter hiccup mode. Hiccup mode will persist until the short-circuit is removed. The SCP circuit becomes active after PGOOD asserts high.

Over-Temperature Protection (OTP)

OTP triggers at a nominal controller temperature of 150°C. The gates of the switching FET and the synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in Figure 1 to program the output voltage V_{OUT}.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1\right)$$

The recommended value for R2 is 2kΩ.

© 2013-2014 Exar Corporation

Programming the Softstart

Place a capacitor C_{SS} between the SS and GND pins to program the soft-start. In order to program a soft-start time of T_{SS}, calculate the required capacitance C_{SS} from the following equation:

$$C_{SS} = T_{SS} \times \frac{10uA}{0.6V}$$

Feed-Forward Capacitor CFF

A feed-forward capacitor C_{FF} is required. C_{FF} provides a low-impedance/high-frequency path for the output voltage ripple to be transmitted to FB. It also results in improved load transient response. Calculate C_{FF} from:

$$C_{FF} = \frac{L \times Istep}{\frac{V_{OUT}}{V_{IN}} \times (V_{IN} - V_{OUT}) \times R1}$$

Where I_{step} is load step

Load step transient response should be checked with C_{FF} calculated above. If necessary the value of C_{FF} may be adjusted in order to yield a critically damped transient response.

Feed-Forward Resistor RFF

In order to prevent switching noise from coupling to the feedback pin, it may be necessary to place a resistor R_{FF} in series with C_{FF}. Calculate RFF from:

$$R_{FF} = \frac{10ns}{C_{FF}}$$

Thermal Design

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are a number of factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated.

The thermal resistance of the XR76115 is specified in the "Operating Ratings" section of this datasheet. The JEDEC θ_{JA} thermal resistance provided is based on tests that comply with the JESD51-2A "Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection" standard. JESD51-xx are a group of standards whose intent is to provide comparative data based on a standard test condition which includes a defined board construction. Since the actual board design in the final application will be different from the board defined in the standard, the thermal resistances in the final design may be different from those shown.

The package thermal derating curves for the XR76115 are shown in Figures 25 and 26. These correspond to input voltage of 12V and 5V respectively.

© 2013-2014 Exar Corporation

Applications Circuit

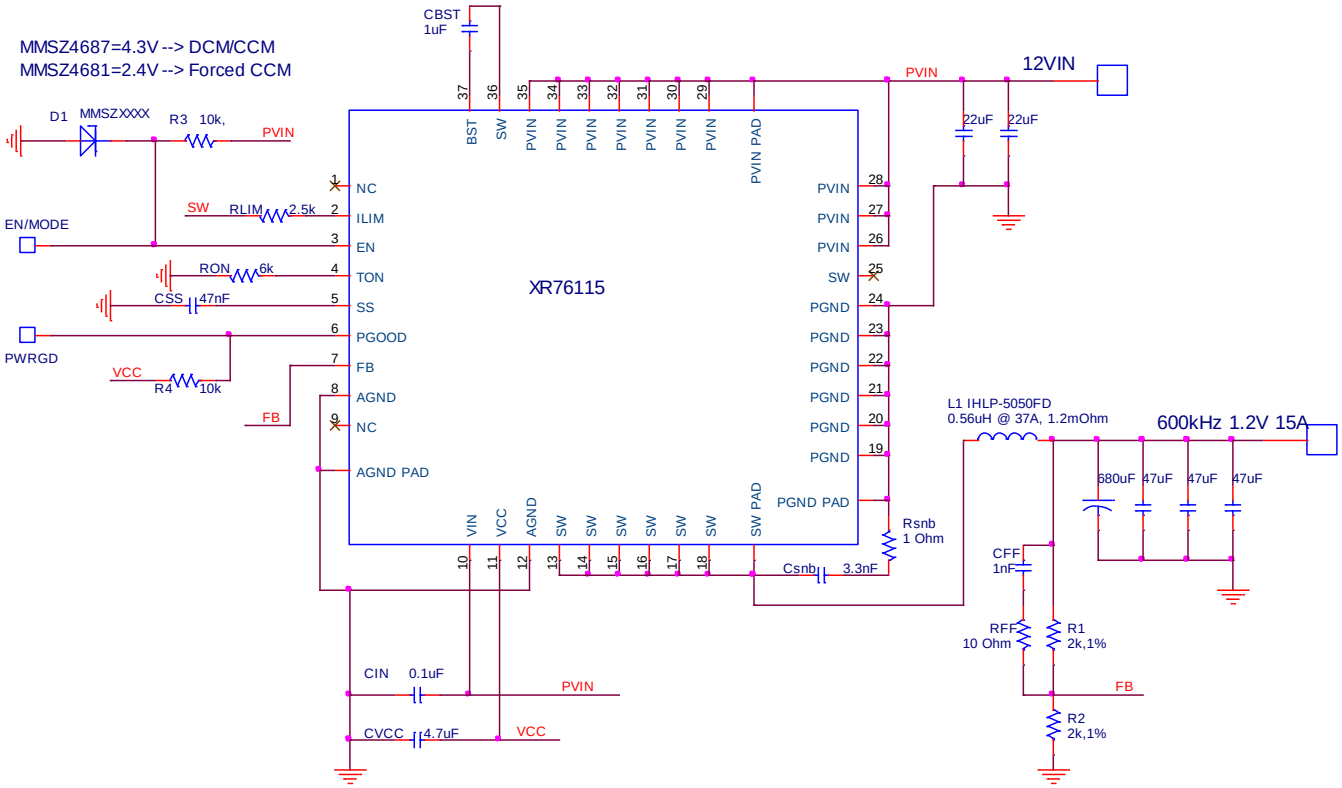
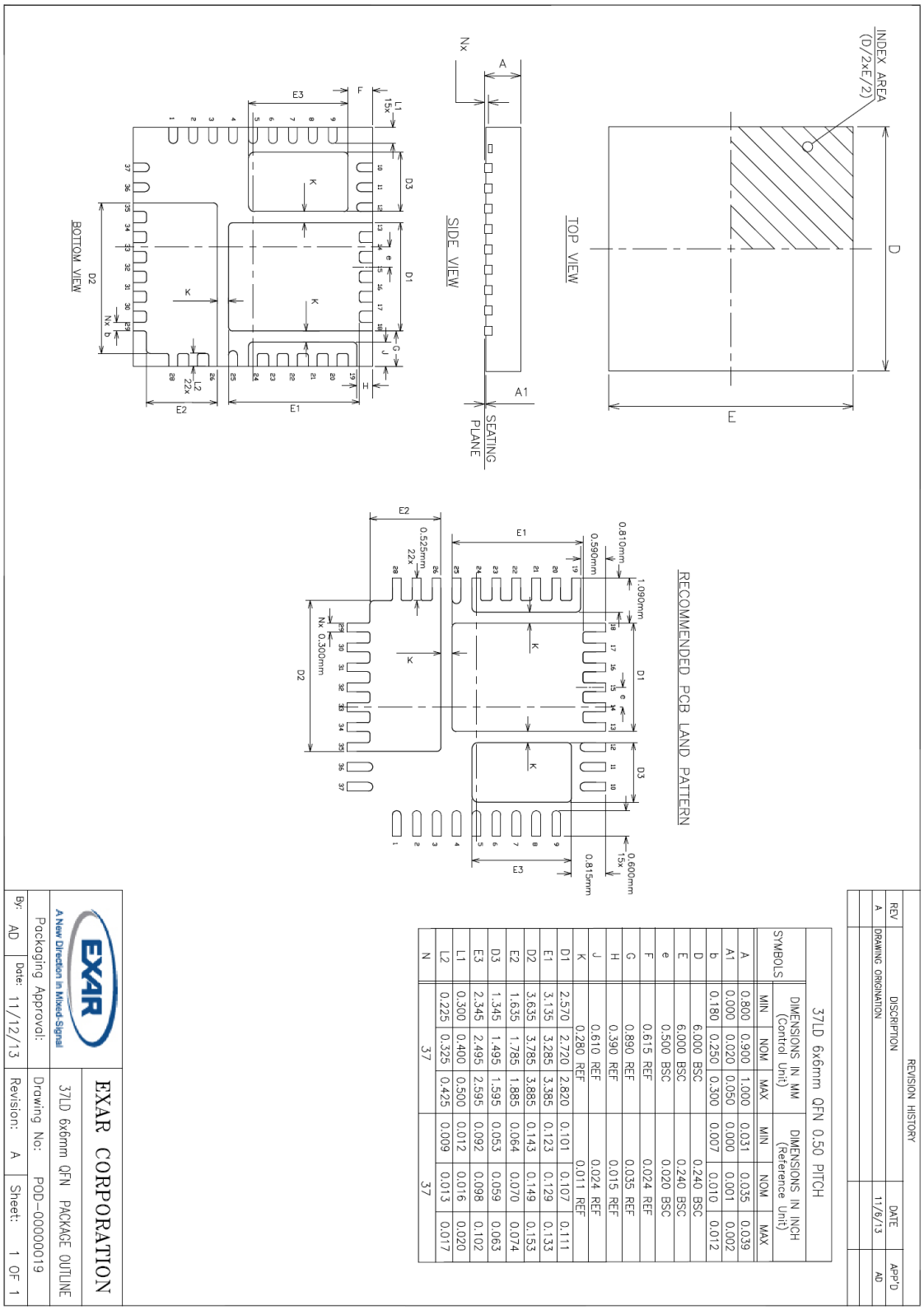


Figure 31: XR76115 Application circuit schematic

Package Specification



37LD 6x6mm QFN 0.50 PITCH

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.800	0.900	1.000	0.031	0.035	0.039
A1	0.000	0.020	0.050	0.000	0.001	0.002
b	0.180	0.250	0.300	0.007	0.010	0.012
D		6.000 BSC			0.240 BSC	
E		6.000 BSC			0.240 BSC	
e		0.500 BSC			0.020 BSC	
F		0.615 REF			0.024 REF	
G		0.890 REF			0.035 REF	
H		0.390 REF			0.015 REF	
J		0.610 REF			0.024 REF	
K		0.280 REF			0.011 REF	
D1	2.570	2.720	2.820	0.101	0.107	0.111
E1	3.135	3.285	3.385	0.123	0.129	0.133
D2	3.635	3.785	3.885	0.143	0.149	0.153
E2	1.635	1.785	1.885	0.064	0.070	0.074
D3	1.345	1.495	1.595	0.053	0.059	0.063
E3	2.345	2.495	2.595	0.092	0.098	0.102
L1	0.300	0.400	0.500	0.012	0.016	0.020
L2	0.225	0.325	0.425	0.009	0.013	0.017
N		37			37	

REV	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	11/6/13	AD

REVISION HISTORY

EXAR CORPORATION

A New Direction in Mixed-Signal

37LD 6x6mm QFN PACKAGE OUTLINE

Packaging Approval:	Drawing No: POD-00000019
By: AD Date: 11/12/13	Revision: A Sheet: 1 OF 1

Revision History

Revision	Date	Description
1A	March 2014	Initial release: ECN 1413-14 03-26-2014

For Further Assistance:

Email: powertechsupport@exar.com

Exar Technical Documentation:http://www.exar.com/TechDoc/

Exar corporation headquarters and Sales Offices

48720 Kato Road
Fremont, CA 94538 – USA

Tel.: +1 (510) 668-7000
Fax: +1 (510) 668-7030

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.