AM335x Industrial Communication Engine EVM Rev2 1 HW User Guide

AM335x Industrial Communication Engine (ICE) EVM Rev. 2.1 Hardware User Guide

Introduction

This document provides the design information on the AM335x processor based ICE EVM (TMDSICE3359) to the users. ICE stands for Industrial Communications Engine. This EVM can be used to evaluate industrial communication protocols based on AM335x.

Description

The low-cost ICE EVM can be used for evaluation and development of industrial communication type applications. It has been equipped with a TI AM3359 processor and a defined set of features to allow the user to experience specifically industrial communication solutions using serial or Ethernet based interfaces. It is not intended as a generic development platform as some of the features and interfaces supplied by the AM335x are not accessible from the ICE board. Using standard interfaces, the ICE board may interface to other processors or systems and act as a communication gateway in this case. In addition it can directly operate as a standard remote I/O system or simple sensor connected to an industrial communication network. The embedded emulation logic allows emulation and debug using standard development tools such as TI's Code Composer Studio by just using the supplied USB cable.

It is not intended for use in end products. All of the design information is freely available and can be used as the basis for the development of an AM335x based product.

EVM System View

The ICE EVM board has dimensions of 3.09” x 4.10 “". The Top Side and the Iso views of the AM335x ICE 2.0 EVM are shown in the pictures provided below.

Top view

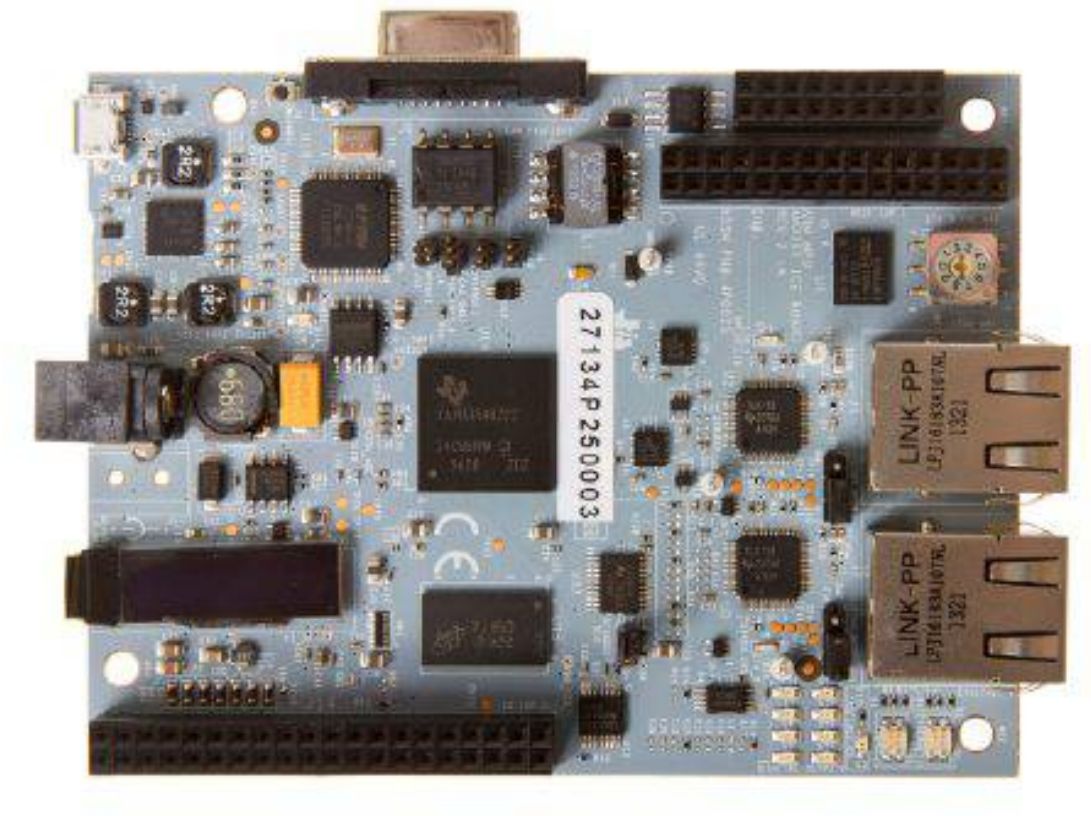

Figure 1: AM3359 ICE 2.1 EVM Top view

Isometric view

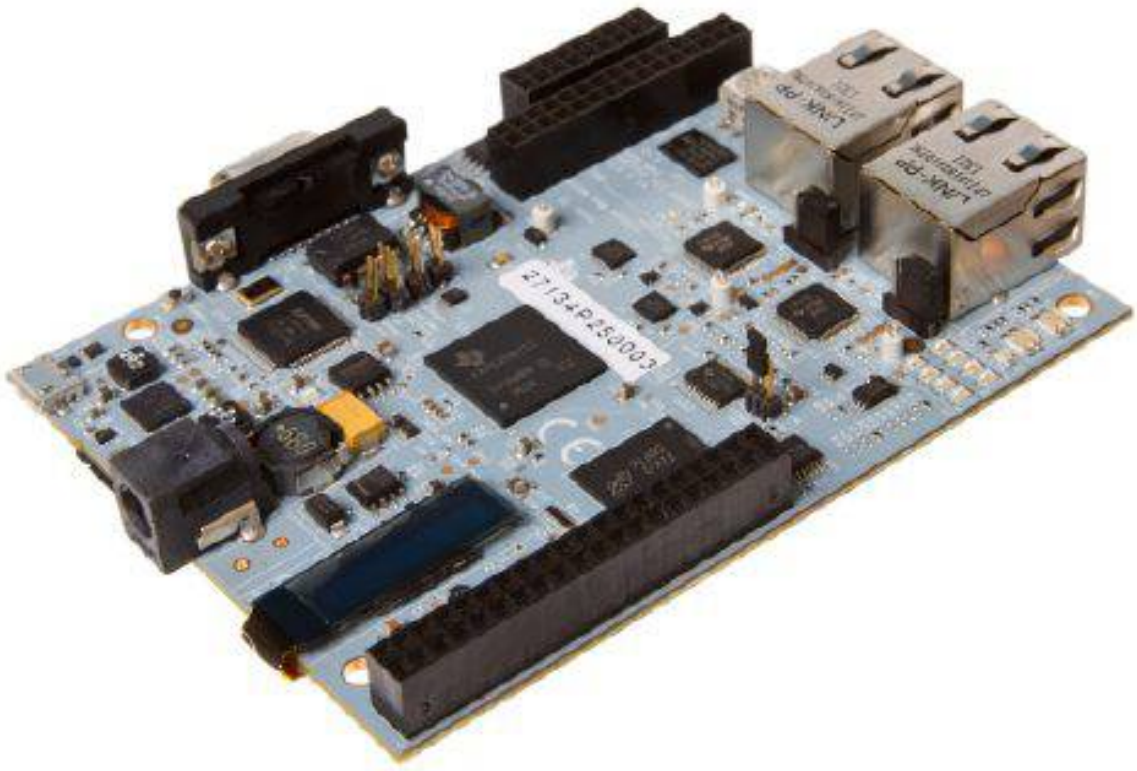

Figure 2: AM3359 ICE 2.1 EVM Iso View

Schematics/Design Files

- HW Documentation [1] - Schematics, Design Files, and other related HW Documentation

Functional Block Diagram of AM335x ICE 2.0 EVM

AM335x ICE Rev. 2.1 EVM Functional Block Descriptions

This section describes about the major functional blocks of the AM335x ICE V2.0 EVM System. The Functional block diagram of the AM335x ICE 2.0 EVM is shown below.

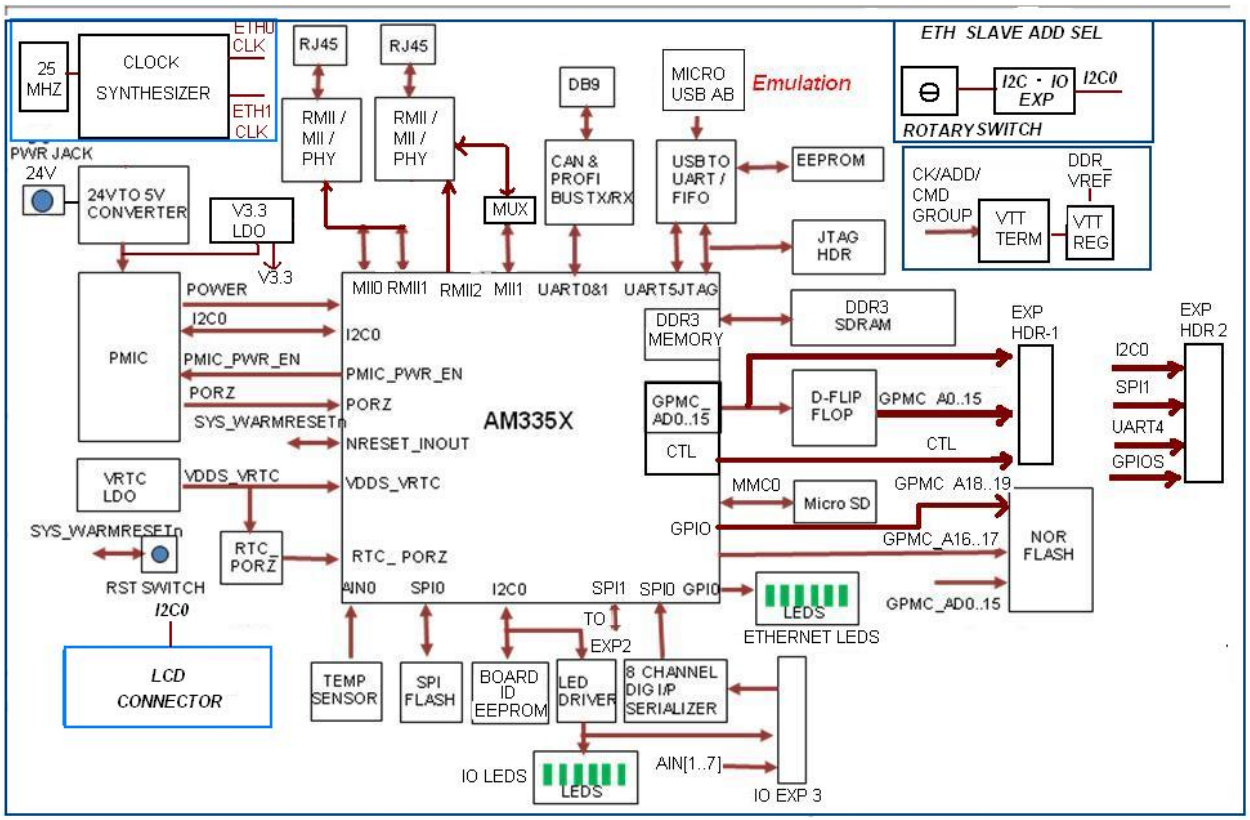

Figure 3: AM335x ICE Rev. 2.1 EVM Block Diagram

Processor

The AM3359ZCZ processor is the central processor for this EVM. All the resources on the board surround the AM3359 processor to provide development capabilities for hardware and software. See the AM3359 datasheet and TRM for the details about the processor.

There are system configuration signals, SYSBOOT, that can be set on the EVM to define some startup parameters on the AM335x processor. See the Configuration/Setup section later for more details.

Clocks

The main clock for the processor is derived from a 24MHz crystal. An on-board oscillator in the AM3359 generates the base clock and subsequent module clocks as needed within the AM3359 processor. A 32kHz clock for the RTC section on the AM3359 processor is derived from a 32kHz crystal on board.

Reset Signals

SYS_RESETn is a signal running to several peripherals and AM335x which performs a reset on those peripherals. SYS_WARMRESETn is asserted by a pushbutton on the board and is used to force a reset of the AM3359. AM3359 can also pulldown on the RESET_INOUTn signal to cause the SYS_RESETn line to go active. The RTC_PORZ reset signal for the RTC section is derived using from an RC delay of the main power supply through VRTC power rail. An AND gate sharpens the edge to meet the AM3359 requirements.

Power

The DC power input to the board is from a 24V DC Power Supply. The 24V power input is converted into 5V to provide power input to the Power Manager TPS65910. The power requirements of the processor are taken care of by the Power Manager IC TPS65910A3. The Power ON LED "D16" is ON if the PMIC is active. The power on sequencing requirements of the AM3359 processor (see the AM3359 datasheet) are handled automatically by the TPS65910A3 PMIC.

Power Management IC

The AM3359 ICE Rev. 2.1 EVM uses the TPS65910A3 power management IC. The I2C0 on AM335x is used to control the TPS65910A3 PMIC. For AM335x, the following power supplies from the TPS65910A are used.

TPS65910A3 Power Supply	AM335x Power Rail	Voltage
VAUX2	VDDSHV1,3,5,6	3.3V (rails that are 3.3V)
VMMC	VDDSHV4 & VDDSHV2	3.3V
VDD2 SMPS	VDD_CORE	1.1V
VDD1 SMPS	VDD_MPU	1.1V
No supply needed	VDD_RTC	1.1V
VRTC	VDDS_RTC	1.8V
VIO_SMPS	VDDS_DDR	1.8V (or 1.5V for DDR3)
VIO_SMPS	DDR_VREF	0.9V
VDAC	VDDS	1.8V
VDIG2	VDDS_SRAM_CORE_BG	1.8V
VDIG2	VDDS_SRAM_MPU_BB	1.8V
VDIG2	VDDS_PLL_DDR	1.8V
VDIG2	VDDS_PLL_CORE_LCD	1.8V
VDIG2	VDDS_PLL_MPU	1.8V
VDIG2	VDDS_OSC	1.8V
VAUX1	VDDA1P8V_USB0/1	1.8V
VAUX33	VDDA3P3V_USB0/1	3.3V
VAUX33	USB_VBUS0/1	3.3V
VPLL	VDDA_ADC	1.8V

VDD3 SMPS	Not Used	-
VIO_SMPS	DDR3 SDRAM	1.8V

Table 1: AM3359 Power supplies from TPS65910A

Configuration/Setup

Boot Configuration

Various boot configurations can be set using the pull up / down resistor combinations provided on the SYS_BOOT pins (LCD_DATA[15..0]).Boot configuration pins are latched upon de-assertion of PORz pin.

SYSBOOT(4..0)	AM3359 Boot Sequence
11010	XIP (MUX2), UART0, SPI0, MMC0
11001	SPI0, MMC0, EMAC1, UART0

I2C Port Address Assignments

Information on I2C address assignments are provided below.

AM335x ICE Rev. 2.1A EVM Function	AM335x I2C Port	Address
ID memory	I2C0	0x50
AM65910A PMIC Control	I2C0	0x2D
CDCE913 Clock Synthesizer	I2C0	0x65
PCA9536DGKR – I2C to IO Expander for Rotary Switch	I2C0	0x41
TPIC2810	I2C0	0x60
LCD Display	I2C0	0x3C

Table 2:I2C Bus Addresses

JTAG

The ICE Rev. 2.1 EVM supports embedded XDS100V2 USB Emulation through the MicroUSB AB connector. It also has an optional 20 pin TI CJTAG connector to support the Emulation. This CJTAG connector is not installed by default.

Memories Supported

The ICE Rev. 2.1 EVM supports on-board memories like DDR3 SDRAM, SPI Flash, NOR Flash and Board ID EEPROM. It also supports an microSD card socket.

DDR3 SDRAM

The ICE design contains a 2Gbit (128M x16) of DDR3 SDRAM memory. The Part number for the DDR3 SDRAM memory used is MT41J128M16JT-125. The package used is an 84 ball FBGA package. See the AM335x TRM for memory locations for this memory.

SPI Flash

A 64Mbit, W25Q64 SPI Flash is used in this design. SPI Flash Boot is enabled through this Flash. This flash is connected to the SPI0 port of the processor.

NOR Flash

A 16Mbit, M29W160EB NOR Parallel Flash memory is used in this design. This NOR flash is connected to the GPMC interface of the processor and is connected as a halfword (16bit) data width only.

Board Identity Memory

The board contains a 256 Kb serial EEPROM that contains board specific data which allows the processor to automatically detect which board is connected and the version of that board. Other hardware specific data can be stored on this memory device as well. The part number of the memory device is CAT24C256WI-GT3. See the Configuration/Setup section for details on the data in this memory.

SDMMC0

The SDMMC0 connector is a card socket SCHA5B0200 (J16). This is a standard SD/MMC Card type of connector. It is connected to the MMC0 port of the AM335x processor. Check the AM335x data sheet and TRM for supported card types/densities. The Pin assignment is as given below.

Pin No	Memory Card PIN No.
uSD#1	DAT2
uSD#2	CD/DAT3
uSD #3	CMD
uSD #4	VCC
uSD #5	CLK
uSD #6	GND
uSD #7	DAT0
uSD #8	DAT1
uSD #9	GND
uSD #10	CD
uSD #11	GND_SD
uSD #12	GND_SD
uSD #13	GND_SD
uSD #14	GND_SD
uSD #15	GND_SD
uSD #16	GND_SD

Table 3: SDMMC0 Connector Pin Details

Ethernet

The ICE Rev. 2.1 EVM has two 10/100 Ethernet transceivers (TLK110) interfaced to connectors J1 & J2 . These Ethernet ports are connected from the Gig Switch and the PRUSS units of the AM335x to the transceivers through a muxing /ORing logic. The reset for the transceivers are driven by the board system reset SYS_RESETn and a GPIO control.The various protocols supported in the design are SERCOS III,SERCOS III S, ETHERNET / IP, POWERLINK, ETHERCAT and PROFINET. The signal MUX_MII_CTL1 is used to switch the muxing logic between the Gb Switch and the PRUSS unit control of the Ethernet PHY's.

The XI clock input pins of both the PHYs are driven from the clock synthesizer CDCE913, (Synthesizer inputs connected to a 25Mhz crystal). The PHYAD pins are left unconnected for setting the PHY's address on the PRU1_MII0 Ethernet so it is by default 0x01. The PHYAD pins on the PRU1_MII1 Ethernet are set to 0x02 using pull up / pull down resistors on the PHYAD pins.

Pin No	Signal Name	Description
1	ETHER0_RDP	Ethernet Data Rx Positive
2	ETHER0_RDN	Ethernet Data Rx Negative
3	V3_3D_PRUETH0JCK	Power
4	V3_3D_PRUETH0JCK	Power
5	ETHER0_TDP	Ethernet Data Tx Positive
6	ETHER0_TDN	Ethernet Data Tx Negative
7	NC	No Connect
8	GND	Ground
D1	LINK LED Power	Power
D2	LINKLED	Link LED Signal
D3	Active LED Power	Power
D4	ACTLED	Active LED Signal

Table 4: Ethernet Jack Pinout

USB

Micro USB-AB connector (J13) is connected to the upstream port of the USB to UART converter IC (FT2232L) . This is used for USB to JTAG and USB to UART conversion applications. This USB port can also be used for XDS100V2 JTAG emulation .

Pin No	Signal Name	Description
1	USB_DC	USB BUS VOLTAGE
2	USB_DM	USB DATA MINUS
3	USB_DP	USB DATA PLUS
4	USB_ID	USB IDENTIFICATION (NC)
5	DGND	Ground

Table 5: USB

CAN/PROFIBUS

The ICE Rev. 2.1 EVM has a DB9 female connector J9 for the PROFI/CAN Bus Interfaces . PR1_UART0 port of AM335x is used for interfacing with the PROFIBUS transceiver ISO1176T & DCAN0 port of the AM335x is used for interfacing with the CAN bus transceiver ISO1050. The Profi signals and CAN signals are on different pins of the connector.

Pin No	Signal Name	Description
1	Reserved	Upgrade Path
2	CAN_L	Dominant Low
3	CAN_GND	Ground
4	Reserved	Upgrade Path
5	PROFI_GND	PROFIBUS Ground
6	VPROFI_DB	PROFIBUS voltage
7	CAN_H	Dominant High
8	Profi BusB	PROFIBUS B
9	CAN_V+	Power, Optional

Table 6: CAN/PROFIBUS Connector Pin Details

CAN /PROFIBUS Selection Jumpers

The Jumpers J6,J7,J8 and J10 are used to select between the CAN / PROFI bus. Description of the selection is provided below.

Jumper	Selection
J6	Pins 1 & 2 Short for CAN bus Voltage select
J10	Pins 1 & 2 Short for PROFIBUS Voltage select
J8	Pins 1 & 2 Short for PROFIBUSA select,Pins 2 & 3 Short for CAN Ground select
J7	Pins 1 & 2 Short for PROFIBUS Ground select

Industrial Inputs

For industrial 24v digital inputs, a SN65HVS882 serializer is used to accept standard signals in and allow the AM335x to read them. The Serialized output from the serializer is fed to the SPI0 port of the processor.

Ethernet LEDs

The Ethernet Protocol LEDs are used to indicate the status of the various protocols supported in the design like SERCOS III,SERCOS III S, ETHERNET / IP, POWERLINK, ETHERCAT, PROFINET.

Protocol	Status	Colour of LED
'SERCOS-III S		RED, GREEN, YELLOW
'ETHERNET/IP	MODULE STATE	RED, GREEN
'POWERLINK	S/E	RED, GREEN
'ETHERCAT	ERROR	RED
'PROFINET	BF	RED

Table 7: Tri-Color LED D1 Mapping

Protocol	Status	Colour of LED
'SERCOS-III SD1		RED, GREEN, YELLOW
'ETHERNET/IP	NETWORK	RED, GREEN
'ETHERCAT	RUN	GREEN
'PROFINET	SF	RED

Table 8: Tri-Color LED D2 Mapping

Industrial Output LEDs

I2C to 8 bit LED driver TPIC2810 is used to drive the eight Industrial output LEDs D6 to D10 AND D12 , D14 and D15. The I2C interface is connected to the I2C0 port of the AM335x processor. By communicating over the I2C bus, these outputs can be set to arbitrary values. The 8 LED driver outputs are also driven to the IO Expansion header. All the LEDs are green in color.

Temperature Sensor

The ICE design has a temperature sensor LM94022 on board which outputs analog ambient temperature data. The output data from the temperature sensor is fed to the Analog input pin AIN0 of the processor.

Rotary Encoded Switch

The EVM has a rotary switch that allows a slave address to be selected. This switch selects a 4bit (hex) value and a I2C converter allows this encoded value to be read by the AM335x through the I2C0 port.

Pin Use Description

GPIO Definitions

See the updated pinmux document which shows the use case columns for GPIOs.

Board Expansion Connectors

There are two expansion connectors provided in the ICE board. They are used for HOST and I/O signals Expansion. The J4 (15 x2 , Female) and J3 (9x2, Female) connectors are used for HOST expansion is a 25x2 header. The Description of the signals are provided below.

Pin No	Signal	Description
1	GPMC_A0	Address 0
1	GPMC_AD0	Data 0
3	GPMC_A1	Address 1
4	GPMC_AD1	Data 1
5	GPMC_A2	Address 2
6	GPMC_AD2	Data 2
7	GPMC_A3	Address 3
8	GPMC_AD3	Data 3
9	GPMC_A4	Address 4
10	GPMC_AD4	Data 4
11	GPMC_A5	Address 5
12	GPMC_AD5	Data 5
13	GPMC_A6	Address 6
14	GPMC_AD6	Data 6
15	GPMC_A6	Address 6
16	GPMC_AD7	Data 7
17	GPMC_A8	Address 8
18	GPMC_AD8	Data 8
19	GPMC_A9	Address 9
20	GPMC_AD9	Data 9
21	GPMC_CSn2	Chip Select 2
22	GPMC_AD10	Data 10
23	GPMC_WEn	Write Enable
24	GPMC_AD11	Data 11
25	GPMC_OEn_REn	Output Enable/ Read Enable
26	GPMC_AD12	Data 12
27	GPMC_ADVn_ALE	Address Latch Enable
28	GPMC_AD13	Data 13
29	GPMC_AD15	Data 15
30	GPMC_AD14	Data 14

Table 9: AM335x Host Expansion Connector 1- J4

Pin No	Signal	Description
1	V3_3D	3.3V Power
2	DGND	Ground
3	LATCH0_IN	Latch 0 Input
4	I2C0_SDA	I2C0 Data
5	LATCH1_IN	Latch 1 Input
6	I2C0_SCL	I2C0 Clock
7	UART4_RXD_SYNC0_OUT	Uart 4 Receive / Sync0 Output
8	UART4_TXD_SYNC1_OUT	Uart 4 Transmit / Sync1 Output
9	GPIO3_18	General Purpose IO
10	EMU4	JTAG EMU4
11	GPIO3_19	General Purpose IO
12	SPI1_SCLK	SPI1 Port Clock
13	GPIO3_20	General Purpose IO
14	SPI1_D0	SPI1 Data0
15	DGND	Ground
16	SPI1_D1	SPI1 Data1
17	V24_IN	24V Power
18	SPI1_CS0	SPI1 Chip Select 0

Table 10: AM335x Host Expansion Connector 2- J3

Pin No	Signal	Description
1	INDUS INPUT0	Digital Input 0
2	V24_0HVS	24V Power
3	INDUS INPUT1	Digital Input 1
4	V24_0HVS	24V Power
5	INDUS INPUT2	Digital Input 2
6	V24_0HVS	24V Power
7	INDUS INPUT3	Digital Input 3
8	V24_0HVS	24V Power
9	INDUS INPUT4	Digital Input 4
10	V24_0HVS	24V Power
11	INDUS INPUT5	Digital Input 5
12	V24_0HVS	24V Power
13	INDUS INPUT6	Digital Input 6
14	V24_0HVS	24V Power
15	INDUS INPUT7	Digital Input 7
16	V24_0HVS	24V Power
17	DGND	Ground

18	DGND	Ground
19	DRAIN0	Digital Output 0
20	DRAIN1	Digital Output 1
21	DRAIN2	Digital Output 2
22	DRAIN3	Digital Output 3
23	DRAIN4	Digital Output 4
24	DRAIN5	Digital Output 5
25	DRAIN6	Digital Output 6
26	DRAIN7	Digital Output 7
27	V5_0D	5V Power
28	V5_0D	5V Power
29	DGND	Ground
30	DGND	Ground
31	AIN1	Analog Input 1
32	AIN5	Analog Input 1
33	AIN2	Analog Input 2
34	AIN6	Analog Input 6
35	AIN3	Analog Input 3
36	AIN7	Analog Input7
37	AIN4	Analog Input 4
38	GNDA_ADC	Analog Ground
39	GNDA_ADC	Analog Ground
40	GNDA_ADC	Analog Ground

Table 11: AM335x I/O Expansion Connector – J14

LCD

The LCD used in this design is a Passive Matrix , Monochrome (light blue) display with 96 × 16 pixels and has a panel size of 29.10 × 9.20 × 1.60 mm. The J17 connector is provided on board to connect with the LCD assembly. The 13V required for the LCD is generated on board using the TPS61041 Boost converter with power input from the 5V power available in the board.

Pin No	Signal	Description
1	V13	Power 13.0V rail
2	VCOMH	Voltage output High
3	IRREF	Current Reference
4	I2C0_SDA	I2C0 Data
5	I2C0_SCL	I2C0 Clock
6	RESn	Power Reset
7	VDD_3V3	Power Supply 3.3V
8	DGND	Ground
9	VBREF	Voltage Reference
10	VBAT_LCD	Power Supply for DC-DC converter
11	C1N	Charge Pump Capacitor1 negative
12	C1P	Charge Pump Capacitor1 positive
13	C2N	Charge Pump Capacitor2 negative
14	C2P	Charge Pump Capacitor2 positive

Table 12:LCD Connector

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Important Notice for Users of EVMs Considered "Radio Frequency Products" in Japan

Note: You can download these EVM terms and conditions in PDF format

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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ANNEX

This Hardware User's Guide is prepared by using the following documents as references.

1. AM335x Sitara ARM Microprocessors TRM (SPRUH73)

References

[1] http://processors.wiki.ti.com/index.php/AM335xBoards#Industrial_Communications_Engine_.28ICE.29_.28AM3359_-_TMDSICE3359.29

[2] http://www.ti.com/esh

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8. Miscellaneous

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