

# ESDR7534

## Low Capacitance TVS for LVDS Interfaces

The ESDR7534 transient voltage suppressor is designed to protect high speed data lines from ESD, EFT, and lightning.

### Features

- Low Capacitance (3 pF Maximum Between I/O Lines and GND)
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (ESD) Level 4 – ±8 kV (Contact); ±15 kV (Air)
- This is a Pb-Free Device

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation (Note 1)	P <sub>pk</sub>	300	W
Maximum Peak Pulse Current 2 x 10 μS @ T <sub>A</sub> = 25°C	I <sub>pp</sub>	10	A
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	8	kV
IEC 61000-4-2 Air (ESD)	ESD	15	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. P<sub>pk</sub> calculated. P<sub>pk</sub> = V<sub>C</sub> × I<sub>pp</sub>.

Table 1. PIN DESCRIPTIONS

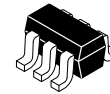
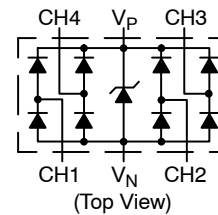
4-Channel, 6-Lead SC70-6			
Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	V <sub>N</sub>	GND	Negative Voltage Supply Rail
3	CH2	I/O	ESD Channel
4	CH3	I/O	ESD Channel
5	V <sub>P</sub>	PWR	Positive Voltage Supply Rail
6	CH4	I/O	ESD Channel



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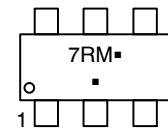
<http://onsemi.com>

### PIN CONFIGURATION AND SCHEMATIC



SC-88  
S7 SUFFIX  
CASE 419B

### MARKING DIAGRAM



7R = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(\*Note: Microdot may be in either location)

### ORDERING INFORMATION

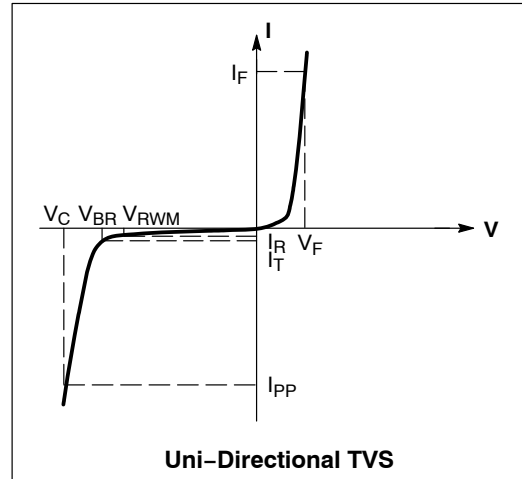
Device	Package	Shipping†
ESDR7534W1T2G	SC-88 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$
$P_{pk}$	Peak Power Dissipation
C	Capacitance @ $V_R = 0$ and $f = 1.0$ MHz

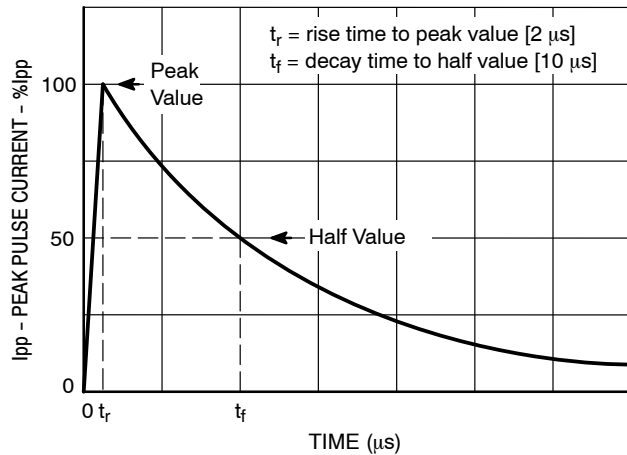


\*See Application Note AND8308/D for detailed explanations of datasheet parameters.

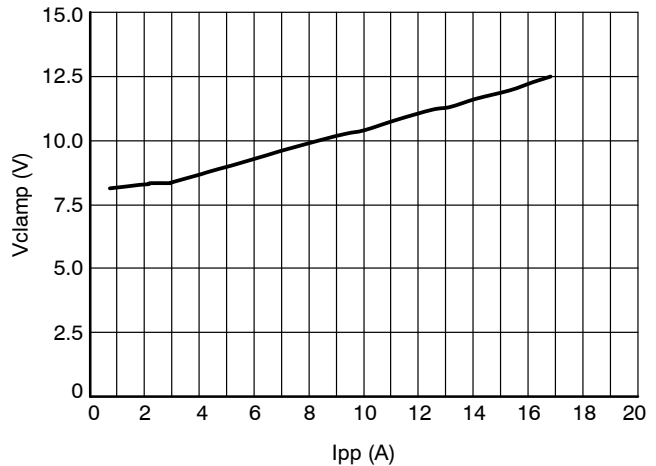
**ELECTRICAL CHARACTERISTICS** ( $T_A=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	(Note 1)			5.0	V
Breakdown Voltage	$V_{BR}$	$I_T = 1$ mA, (Note 2)	6.0	8.0	9.5	V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5$ V			3.0	$\mu\text{A}$
Forward Voltage	$V_F$	$I_F = 100$ mA			1.6	V
Clamping Voltage	$V_C$	$I_{PP} = 10$ A (2 x 10 $\mu\text{s}$ Waveform)			30	V
Maximum Peak Pulse Current	$I_{PP}$	2 x 10 $\mu\text{s}$ Waveform			10	A
Junction Capacitance	$C_J$	$V_R = 0$ V, $f = 1$ MHz between I/O Pins and GND		1.9	3.0	pF
Junction Capacitance	$C_J$	$V_R = 0$ V, $f = 1$ MHz between I/O Pins		0.8	1.0	pF

1. TVS devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
2.  $V_{BR}$  is measured at pulse test current  $I_T$ .



**Figure 1. Exponential Decay Pulse Waveform**



**Figure 2. Clamping Voltage vs. Peak Pulse Current ( $t_p = 2 \times 10 \mu\text{s}$ ,  $R = 8 \Omega$ )**

# ESDR7534

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

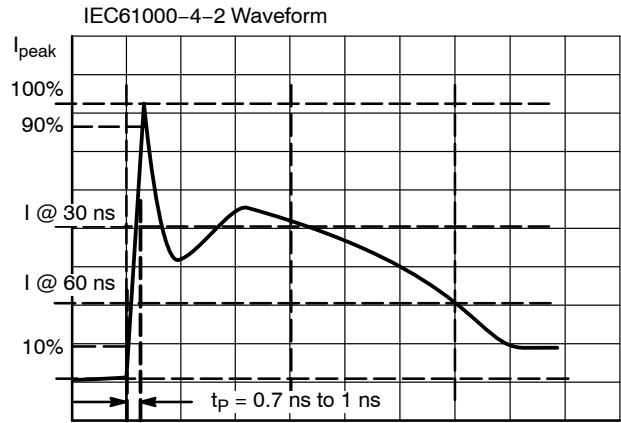


Figure 3. IEC61000-4-2 Spec

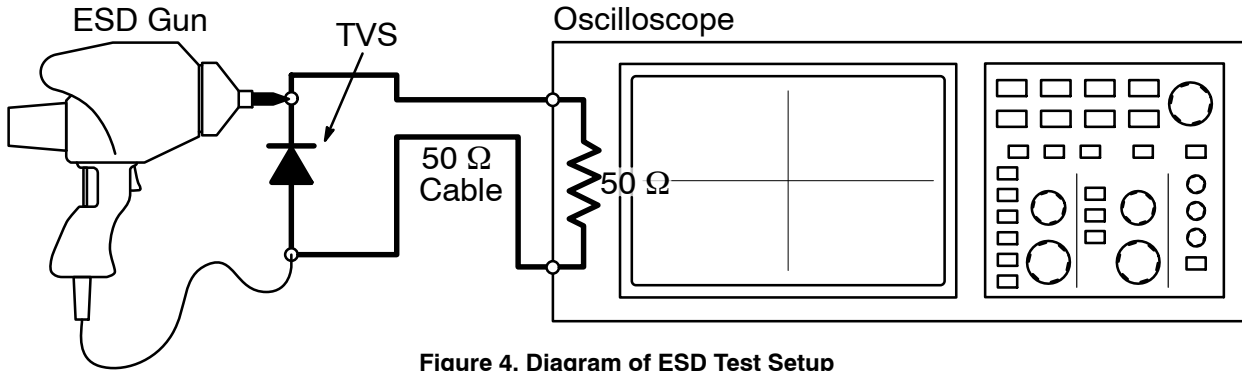


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D - Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

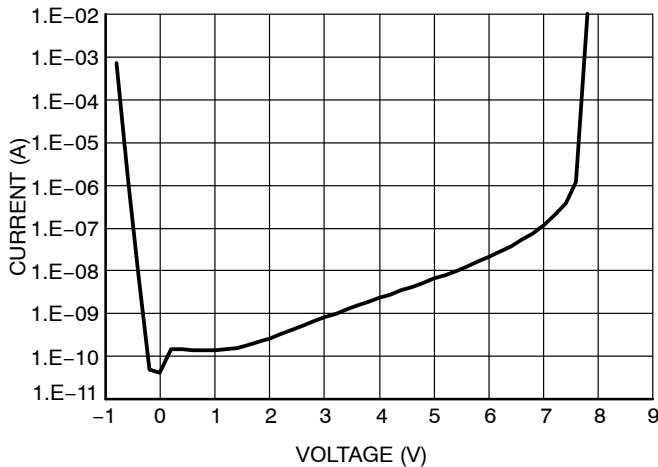


Figure 5. IV Characteristic Curve

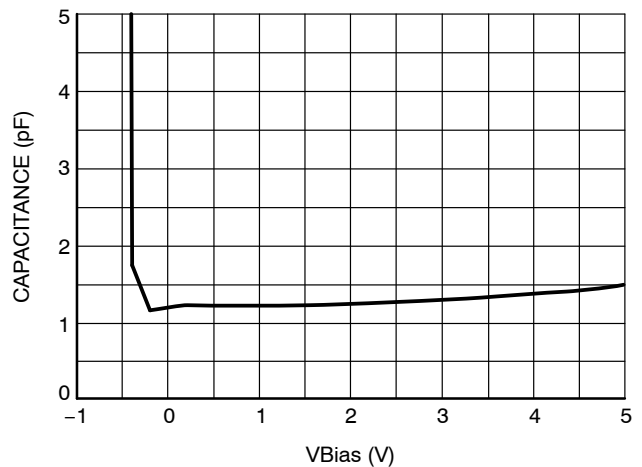


Figure 6. CV Characteristic Curve

## APPLICATIONS INFORMATION

The new ESDR7534 is a low capacitance TVS diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the ESDR7534 offers low capacitance steering diodes and an internal TVS diode ( $V_P$  diode) integrated in a single package. If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The TVS device protects the power line against overvoltage conditions to avoid damage to the power supply and any downstream components.

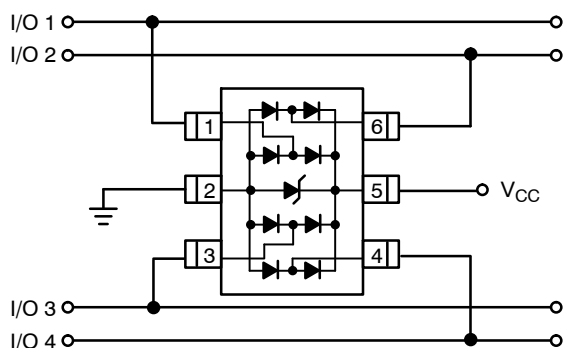
### ESDR7534 Configuration Options

The ESDR7534 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage ( $V_f$  or  $V_{CC} + V_f$ ). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 2. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

#### Option 1

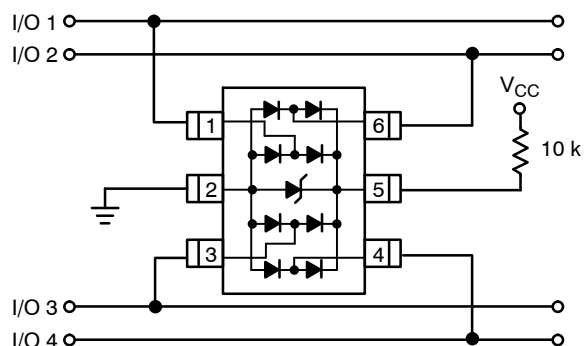
Protection of four data lines and the power supply using  $V_{CC}$  as reference.



For this configuration, connect pin 5 directly to the positive supply rail ( $V_{CC}$ ), the data lines are referenced to the supply voltage. The  $V_P$  diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

#### Option 2

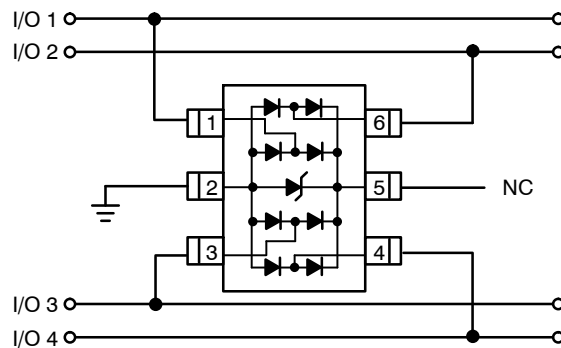
Protection of four data lines with bias and power supply isolation resistor.



The ESDR7534 can be isolated from the power supply by connecting a series resistor between pin 5 and  $V_{CC}$ . A 10 kΩ resistor is recommended for this application. This will maintain a bias on the  $V_P$  and steering diodes, reducing their capacitance.

#### Option 3

Protection of four data lines using the  $V_P$  diode as reference.

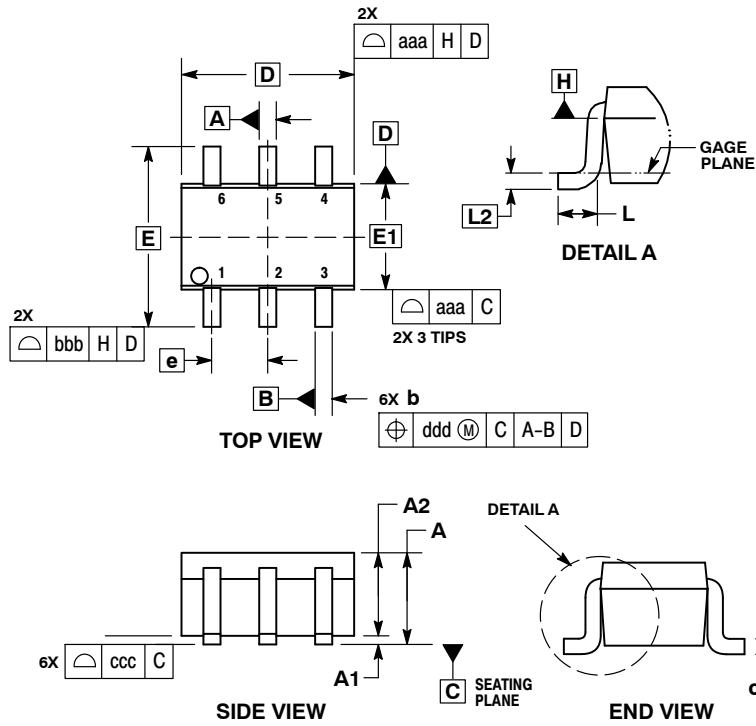


In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the  $V_P$  can be used as the reference. For these applications, pin 5 is not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the  $V_{BR}$  of the I/O (CHX) pin.

# ESDR7534

## PACKAGE DIMENSIONS

SC-88/SC-70-6/SOT-363  
CASE 419B-02  
ISSUE Y

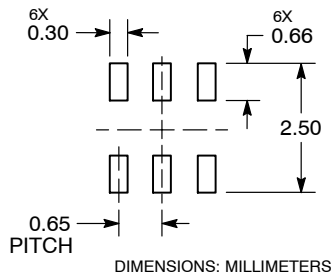


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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