TPS60140, TPS60141
LOW POWER DC-DC CONVERTER
REGULATED 5 V, 100-mA CHARGE PUMP VOLTAGE TRIPLER

features

- Regulated 5 V ± 4% Output Voltage With up to 100 mA Output Current From a 1.8 V to 3.6 V Input Voltage Range
- 65-μA Quiescent Supply Current
- 0.05-μA Shutdown Current, Battery Is Isolated From Load in Shutdown
- Integrated Low-Battery or Power-Good Indicator
- Low Output Voltage Ripple Over Complete Output Current Range
- Easy-To-Design With Low-EMI Power Supply Since no Inductors Are Required
- Evaluation Module Available (TPS60140EVM-144)

applications

- Replaces DC/DC Converters With Inductors in Battery-Powered Applications:
  - Two Battery Cells to 5 V Conversion
  - Portable Instruments
  - Miniature Equipment
  - Backup-Battery Boost Converters
  - Medical Instruments
  - 5-V Smart Card Supply
  - Organizers, PDAs

typical operating circuit

description

The TPS6014x step-up, regulated charge pumps generate a 5-V ±4% output voltage from a 1.8 V to 3.6 V input voltage range. The devices are typically powered by two alkaline, NiCd, or NiMH battery cells and provide an output current of minimum 100 mA from a 2-V input. Only four external capacitors are needed to build a complete voltage tripler charge pump.

The devices regulate the output by using the pulse-skip topology. The controller is optimized for lowest output voltage ripple over the complete output current range. The output peak current and therefore the output voltage ripple are drastically reduced compared to a conventional pulse-skip topology by regulating the charge pump output resistance. At light loads the maximum output resistance is limited to assure a low quiescent current.

The TPS60140 includes a low-battery comparator that issues a warning if the battery voltage drops below a user-adjustable threshold voltage. The TPS60141 features a power-good output that goes active when the output voltage reaches 90% of its nominal value.

The logic shutdown function disables the converter, reduces the supply current to a maximum of 1 μA and disconnects the output from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This dc-dc converter requires no inductors, therefore, EMI is of little concern. It is available in the small, thermally enhanced 20-pin TSSOP package (PWP).
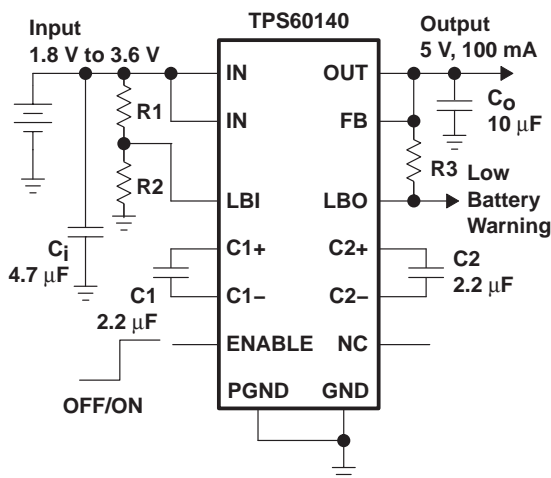
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

![Texas Instruments logo]

AVAILABLE OPTIONS

T_A	PART NUMBER†	PACKAGE		DEVICE FEATURES	
−40°C to 85°C	TPS60140PWP	PWP	20-pin thermally enhanced TSSOP	2-cell to 5 V, 100 mA	Low-battery detector
	TPS60141PWP				Power-good detector

† The PWP package is available taped and reeled. Add an R suffix to the device type (e.g. TPS60140PWPR) to order quantities of 2000 devices per reel.

PWP PACKAGE (TPS60140)
(TOP VIEW)

GND	1	20	GND
GND	2	19	GND
ENABLE	3	18	LBI
FB	4	17	LBO
OUT	5	16	NC
C1+	6	15	C2+
IN	7	14	IN
C1−	8	13	C2−
PGND	9	12	PGND
PGND	10	11	PGND

PWP PACKAGE (TPS60141)
(TOP VIEW)

GND	1	20	GND
GND	2	19	GND
ENABLE	3	18	NC
FB	4	17	PG
OUT	5	16	NC
C1+	6	15	C2+
IN	7	14	IN
C1−	8	13	C2−
PGND	9	12	PGND
PGND	10	11	PGND

functional block diagrams

TPS60140

TPS60141

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
C1+	6		Positive terminal of the flying capacitor C1
C1–	8		Negative terminal of the flying capacitor C1
C2+	15		Positive terminal of the flying capacitor C2
C2–	13		Negative terminal of the flying capacitor C2
ENABLE	3	I	ENABLE input. Connect ENABLE to IN for normal operation. When ENABLE is a logic low, the device turns off and the supply current decreases to 0.05 µA. The output is disconnected from the input when the device is placed in shutdown.
FB	4	I	Feedback input. Connect FB to OUT as close to the load as possible to achieve best regulation. A resistive divider is on the chip to match the output voltage to the internal reference voltage of 1.21 V.
GND	1, 2, 19, 20		Ground. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.
IN	7,14	I	Supply input. Bypass IN to PGND with capacitor C_i. Connect both IN terminals through a short trace.
LBO/PG	17	O	Low battery detector output (TPS60140) or power good output (TPS60141). Open drain output of the low-battery indicator or power-good comparator. It can sink 1 mA. A 100-kΩ to 1-MΩ pullup is recommended. Leave the terminal unconnected if the low-battery or power-good detector function is not used.
LBI/NC	18	I	Low battery detector input (TPS60140 only). The voltage applied to this terminal is compared to the internal 1.21-V reference voltage. Connect the terminal to ground if the low-battery comparator is not used. On the TPS60141, this terminal is not connected to the chip and should remain unconnected.
NC	16		Not connected
OUT	5	O	Regulated 5-V power output. Bypass OUT to PGND with the output filter capacitor C_O.
PGND	9–12		Power ground. The charge-pump current flows through this terminal. Connect all PGND terminals together.

detailed description

The TPS6014x charge pumps provide a regulated 5-V output from a 1.8-V to 3.6-V input voltage range. They can deliver a maximum continuous load current of at least 100 mA at V_I = 2 V minimum. Designed specifically for space-critical battery-powered applications, the complete charge pump circuit requires only four external capacitors.

The TPS6014x consist of an oscillator, a 1.21-V voltage reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, a low-battery or power-good comparator and a control circuit (see the functional block diagrams).

operating principle

The TPS6014x devices regulate the output voltage using an improved pulse-skip topology. In pulse-skip mode the error amplifier disables switching of the power stages when it detects an output voltage higher than 5 V. The oscillator halts and the controller skips switching cycles. The error amplifier reactivates the oscillator and starts switching of the power stages again when the output voltage drops below 5 V. The output resistance of the charge pump is controlled to improve the ripple performance. This limits the output current to the minimum that is necessary to sustain a regulated output voltage. The benefit is that the ripple performance is nearly as good as with a linear-regulation topology.

At light loads a conventional pulse-skip regulation mode is used, but the charge pump output resistance is held at a high level. The pulse-skip regulation minimizes the operating current because the charge pump does not switch continuously and hence the gate-charge losses of the MOSFETs are reduced. Additionally, all functions except voltage reference, error amplifier, and low-battery or power-good comparator are deactivated when the output is higher than 5 V. When switching is disabled by the error amplifier, the load is also isolated from the input. This improved pulse-skip control topology is also referred to as *active-cycle* control.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

detailed description (continued)

start-up procedure and shutdown

During start-up, i.e., when ENABLE is set from logic low to logic high, the output capacitor is charged up with a limited current until the output voltage(V_O) reaches 0.8 x V_I. When the start-up comparator detects this voltage limit, the IC begins switching. This pre-charging of the output capacitor ensures a short start-up time. In addition, the inrush current into an empty output capacitor is limited because the current through the switches is limited before the charge pump starts switching.

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05 μA of supply current in this mode. Leakage current drawn from the output is as low as 1 μA max. The device exits shutdown once ENABLE is set to a high level. When the device is in shutdown, the load is isolated from the input.

undervoltage lockout and short-circuit protection

The TPS6014x devices have an undervoltage lockout feature that deactivates the device and places it in shutdown mode when the input voltage falls below 1.6 V. The devices are also short-circuit protected. The output current is limited to typically 100 mA during a hard short circuit condition at the output, i.e., when V_O is GND. In this case the condition to enter the start-up mode is met, the device stops switching and controls the on-resistance of the appropriate MOSFET switches to limit the current.

low-battery detector (TPS60140 only)

The internal low-battery comparator trips at 1.21 V $\pm$ 5% when the voltage on pin LBI ramps down. The voltage $V_{(TRIP)}$ at which the low battery warning is issued can be adjusted with a resistive divider as shown in Figure 1. The sum of resistors R1 and R2 is recommended to be in the 100 kΩ to 1 MΩ range. When choosing R1 and R2, be aware of the input leakage current into the LBI terminal.

LBO is an open drain output. An external pullup resistor to OUT, in the 100 kΩ to 1 MΩ range, is recommended. During start-up, the LBO output signal is invalid for the first 500 μs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected.

$$V_{(TRIP)} = 1.21\,V \times \left(1 + \frac{R1}{R2}\right)$$
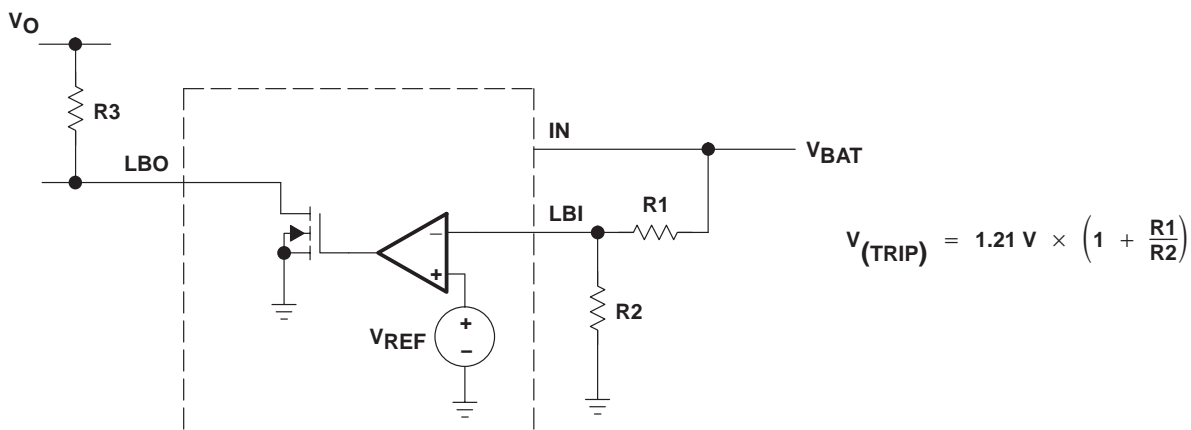
Figure 1. Programming of the Low-Battery Comparator Trip Voltage

A 100 nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

low-battery detector (TPS60140 only) (continued)

Formulas to calculate the resistive divider for low battery detection, with $V_{(LBI)}$ = 1.15 V to 1.27 V:

$$R2 \ = \ 1 \ M\Omega \ x \ \frac{V_{LBI}}{V_{Bat}} \tag{1}$$

$$R1 \ = \ 1 \ M\Omega - R2 \tag{2}$$

Formulas to calculate the minimum and maximum trip voltage:

$$V_{trip(min)} \ = \ V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}} \tag{3}$$

$$V_{trip(max)} \ = \ V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}} \tag{4}$$

Table 1. Recommended Values for the Resistive Divider From the E96 Series ($\pm$1%)

V_I/V	R1/kΩ	R2/kΩ	$V_{(TRIP)}$MIN/V	$V_{(TRIP)}$MAX/V
1.8	357	732	1.700	1.902
1.9	365	634	1.799	2.016
2.0	412	634	1.883	2.112
2.1	432	590	1.975	2.219
2.2	442	536	2.080	2.338

power-good detector (TPS60141)

The PG terminal is an open-drain output that is pulled low when the output is out of regulation. When the output rises to typically 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation an external pullup resistor must be connected between PG and OUT. The resistor should be in the 100 kΩ to 1 MΩ range. If the power-good function is not used, the PG terminal should remain unconnected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Supply voltage range at IN to GND and PGND . . . . −0.3 V to 3.6 V
Voltage range, at OUT, ENABLE, LBI, LBO, PG, FB to GND and PGND . . . . −0.3 V to 5.4 V
Voltage range at C1+ TO GND . . . . −0.3 V to (V_O + 0.3 V)
Voltage range at C1− TO GND . . . . −0.3 V to (V_I + 0.3 V)
Voltage range at C2+ TO GND . . . . −0.3 V to (V_O + 0.3 V)
Voltage range at C2− TO GND . . . . −0.3 V to (V_I + 0.3 V)
Continuous output current . . . . 150 mA
Storage temperature range, T_{stg} . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Maximum junction temperature, T_J . . . . 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ $V_{(ENABLE)}$, $V_{(LBI)}$, $V_{(LBO)}$, and $V_{(PG)}$ can exceed V_I up to the maximum rated voltage without increasing the leakage current drawn by these inputs.

![Texas Instruments logo]

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	1.8	3.6	V
Continuous output current, $I_O$max		100	mA
Operating junction temperature, T_J		125	°C

electrical characteristics at C_i = 4.7 μF, C1 = C2 = 2.2 μF, C_o = 10 μF† at T_C = –40°C to 85°C, V_I = 2 V, FB = V_O and ENABLE = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(UVLO)}$	Undervoltage lockout threshold	T_C = 25°C		1.6	1.8	V
$I_O$max	Maximum continuous output current		100			mA
V_O	Output voltage	1.8 V < V_I < 2 V, V_O Start-up = 5 V, 0 < I_O < $I_O$max/2 T_C = 0°C to 70°C	4.8		5.2	V
		2 V < V_I < 3.6 V, 0 < I_O < $I_O$max	4.8		5.2	
$I_{lkg(OUT)}$	Output leakage current	V_I = 2.4 V, $V_{(ENABLE)}$ = GND			1	μA
I_Q	Quiescent current (no-load input current)	V_I = 2.4 V		65	90	μA
$I_{(SD)}$	Shutdown current	V_I = 2.4 V, $V_{(ENABLE)}$ = GND		0.05	1	μA
$f_{(OSC)}$	Oscillator frequency		210	320	450	kHz
V_{IL}	ENABLE input voltage low	V_I = 1.8 V			$0.3 \times V_I$	V
V_{IH}	ENABLE input voltage high	V_I = 3.6 V	$0.7 \times V_I$			V
$I_{lkg(ENABLE)}$	ENABLE input leakage current	$V_{(ENABLE)}$ = GND or V_I		0.01	0.1	μA
	Output load regulation	V_I = 2.4 V, 1 mA < I_O < $I_O$max, T_C = 25°C		0.003		%/mA
	Output line regulation	2 V < V_I < 3.6 V, V_O = 5 V: I_O = 75 mA, T_C = 25°C		0.08		%/V
$I_{(SC)}$	Short circuit current limit	V_I < 2.4 V, V_O = 0 V, T_C = 25°C		100		mA
$V_{(TRIP,LBI)}$	LBI trip voltage	TPS60140	V_I = 1.8 V to 2.2 V, Hysteresis 0.8% for rising LBI voltage, T_C = 0°C to 70°C	1.15	1.21	1.27	V
$I_{I(LBI)}$	LBI input current	TPS60140	LBI = 1.3 V		20	100	nA
$V_{O(LBO)}$	LBO output voltage low‡	TPS60140	$V_{(LBI)}$ = 0 V, $I_{(LBO,SINK)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO output leakage current	TPS60140	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 5 V		0.01	0.1	μA
$V_{(TRIP,PG)}$	Power-good trip voltage	TPS60141	T_C = 0°C to 70°C	$0.86 \times V_O$	$0.90 \times V_O$	$0.94 \times V_O$	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	TPS60141	V_O ramping down, T_C = 0°C to 70°C		0.8%		
$V_{O(PG)}$	Power-good output voltage low	TPS60141	V_O = 0 V, $I_{(PG,SINK)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	TPS60141	V_O = 5 V, $V_{(PG)}$ = 5 V		0.01	0.1	μA

† All capacitors are ceramic capacitors of the type X5R or X7R.
‡ During start-up the LBO signal is invalid for the first 500 μs.

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

Used Capacitor Types:
C_i, C_O: Ceramic, X7R, Size 1206
C1, C2: Ceramic, X7R, Size 1206
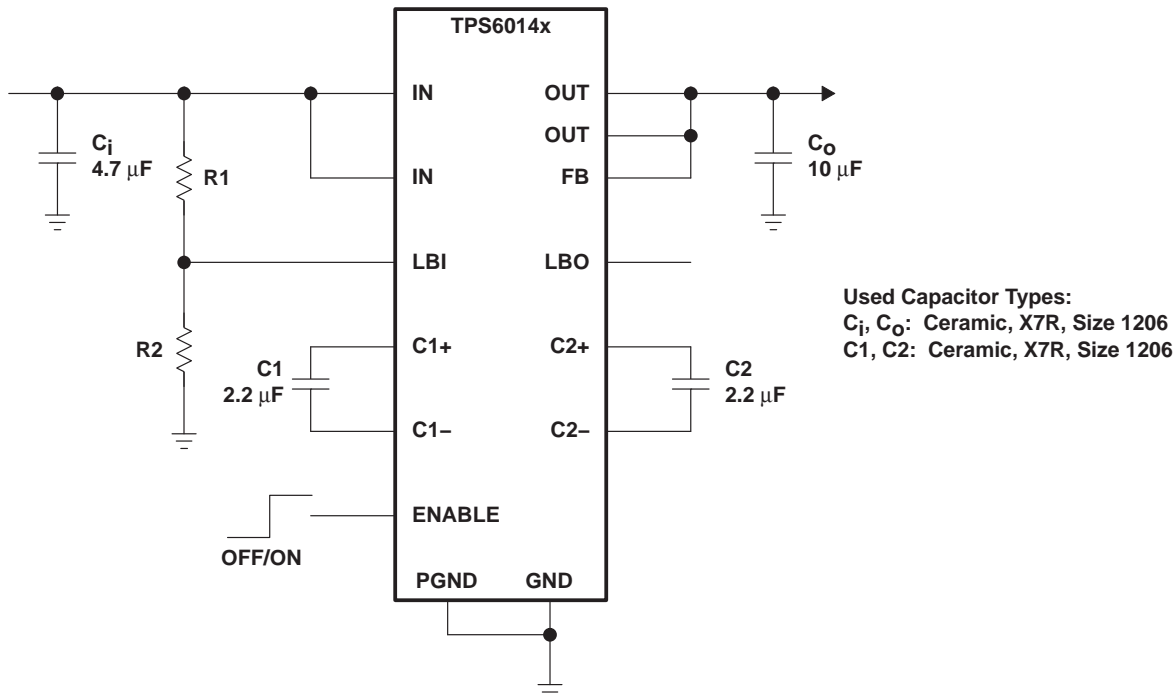
Figure 2. Circuit Used For Typical Characteristics Measurements

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Output Current	3
		vs Input Voltage	4
I_Q	Quiescent Supply Current	vs Input Voltage	5
V_O	Output Voltage	vs Output Current	6
		vs Input Voltage	7
V_O	Output Voltage Ripple		8,9,10
V_{PP}	Output Voltage Ripple Amplitude	vs Input Voltage	11
		vs Output Current	12
$f_{(OSC)}$	Oscillator Frequency	vs Input Voltage	13
	Load Transient Response		14
	Line Transient Response		15
V_O	Output Voltage	vs Time (Start-up Timing)	16

TEXAS INSTRUMENTS
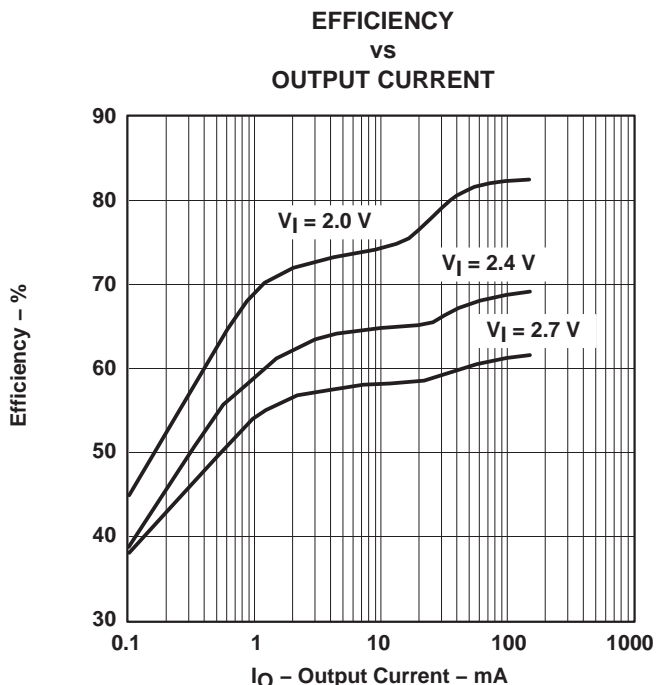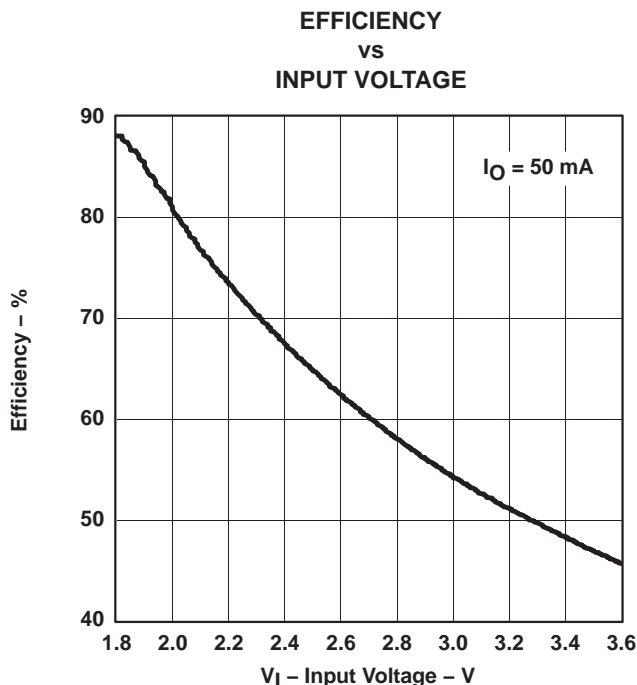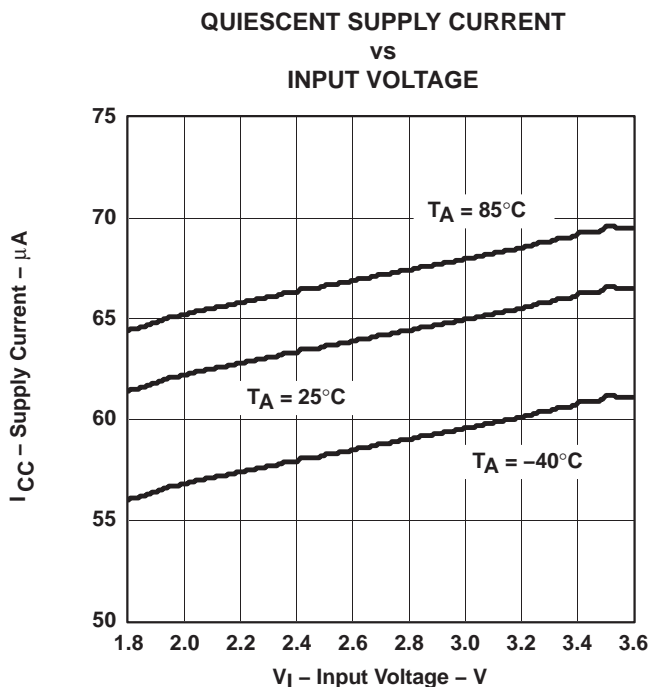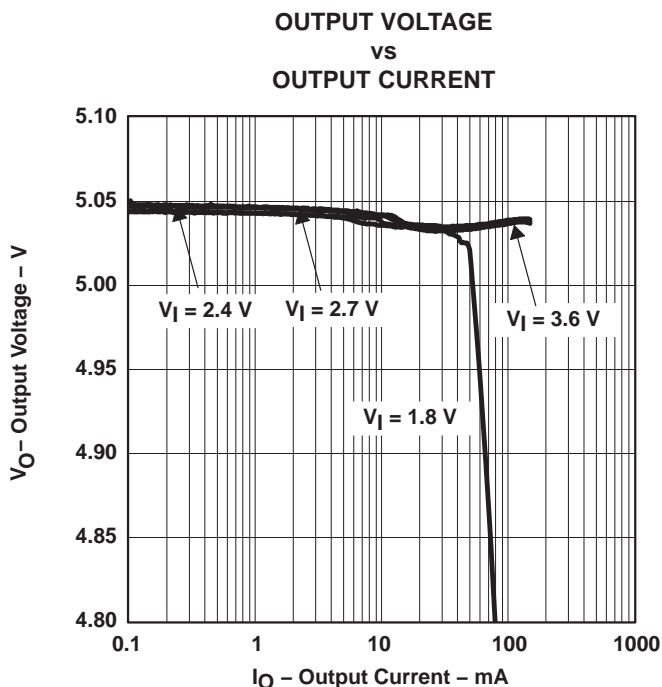
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

**EFFICIENCY
vs
OUTPUT CURRENT**

Figure 3

**EFFICIENCY
vs
INPUT VOLTAGE**

Figure 4

**QUIESCENT SUPPLY CURRENT
vs
INPUT VOLTAGE**

Figure 5

**OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

Figure 6

![Texas Instruments logo] TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE
vs
INPUT VOLTAGE**
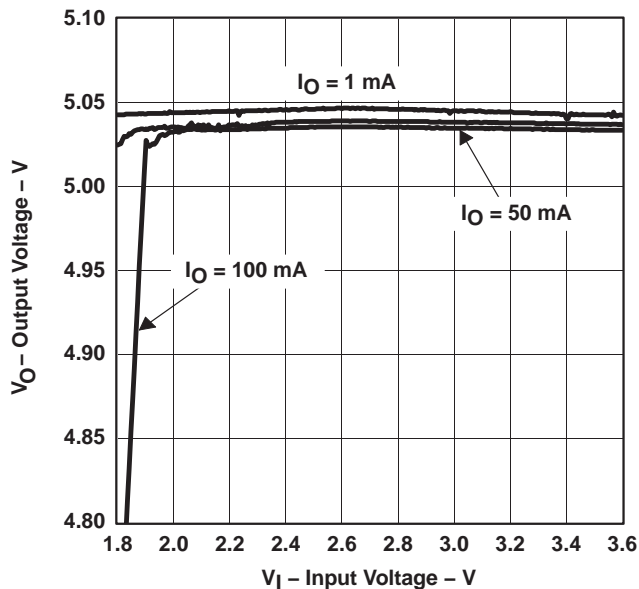
Figure 7

OUTPUT VOLTAGE RIPPLE

Figure 8

OUTPUT VOLTAGE RIPPLE

Figure 9

OUTPUT VOLTAGE RIPPLE
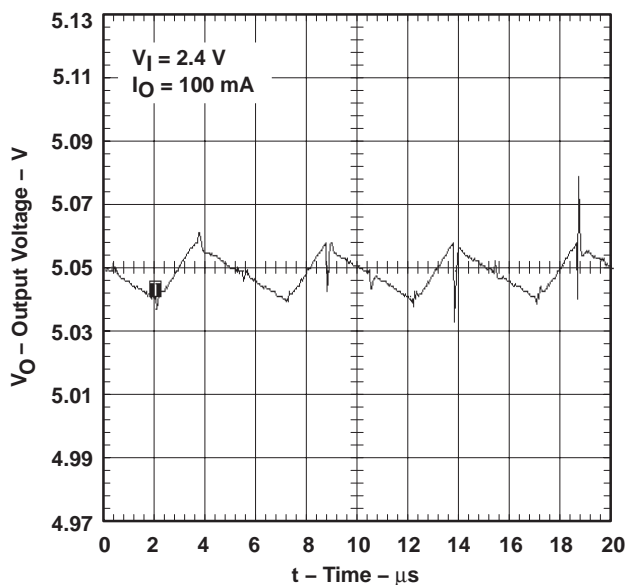
Figure 10

TYPICAL CHARACTERISTICS
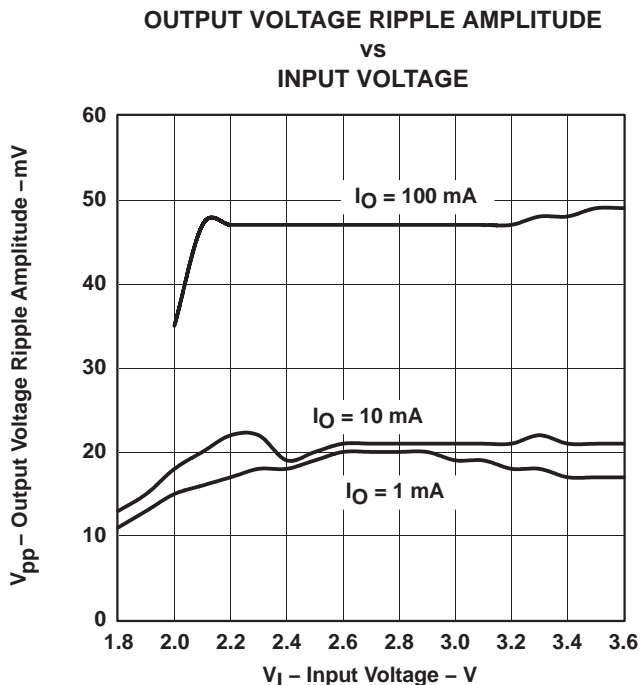
**OUTPUT VOLTAGE RIPPLE AMPLITUDE
vs
INPUT VOLTAGE**

Figure 11

**OUTPUT VOLTAGE RIPPLE AMPLITUDE
vs
OUTPUT CURRENT**

Figure 12

**OSCILLATOR FREQUENCY
vs
INPUT VOLTAGE**

Figure 13

LOAD TRANSIENT RESPONSE

Figure 14

TEXAS
INSTRUMENTS

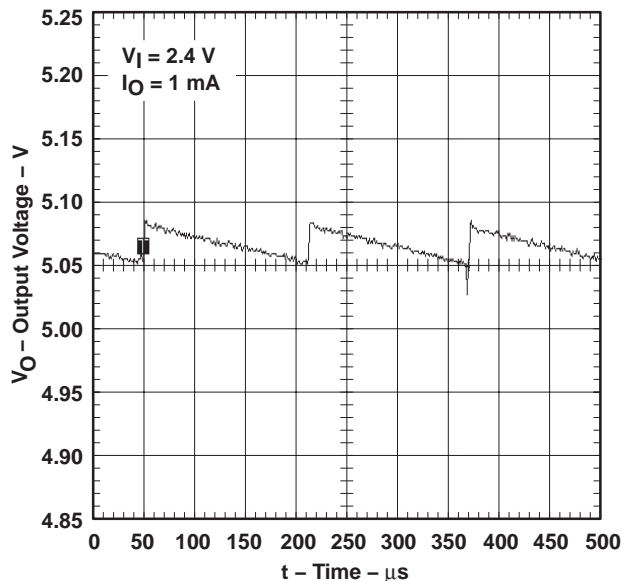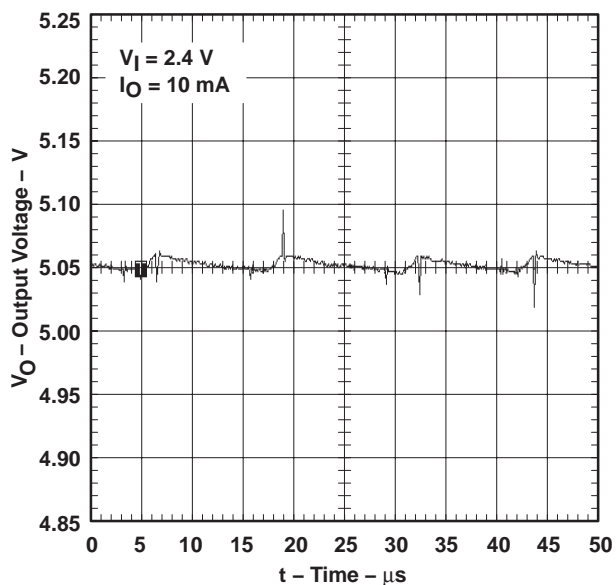POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

11

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

Figure 15

OUTPUT VOLTAGE vs TIME (START-UP TIMING)
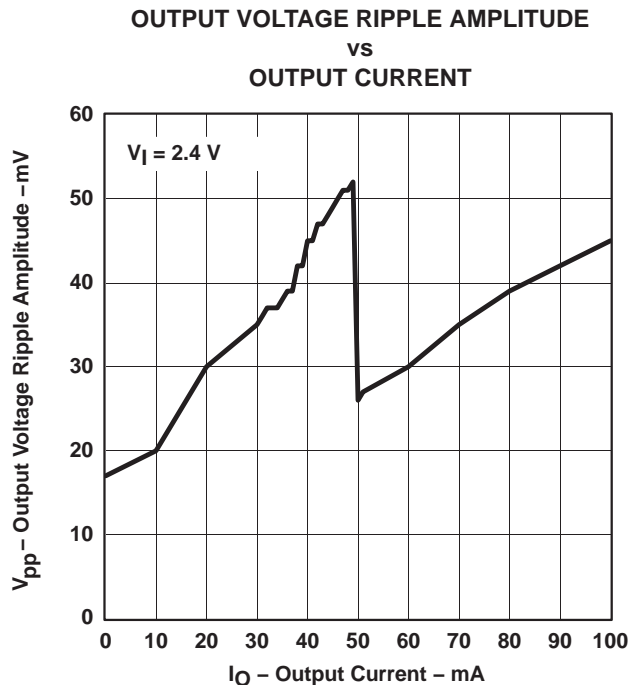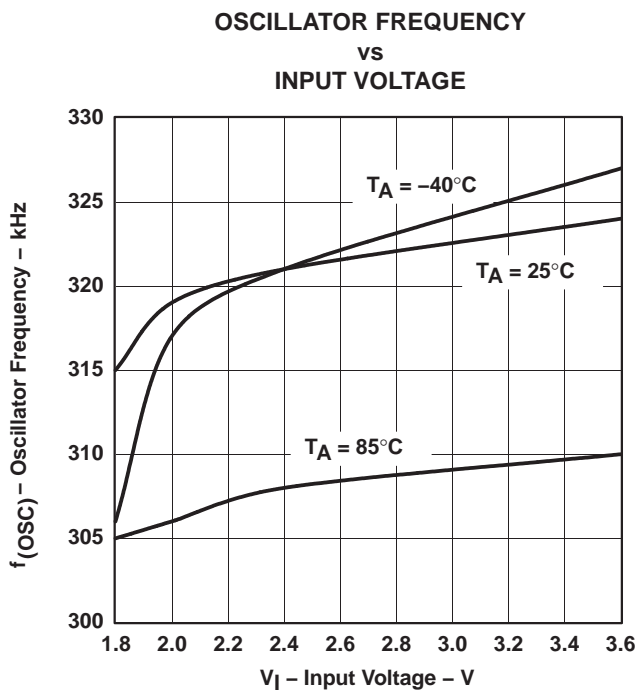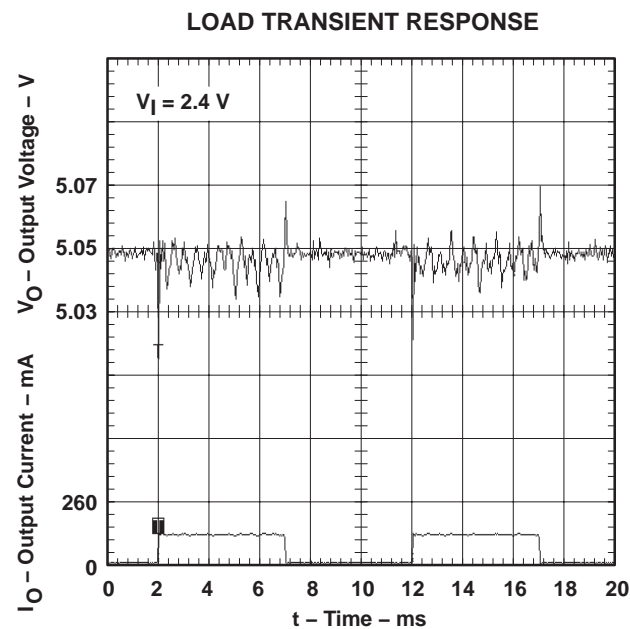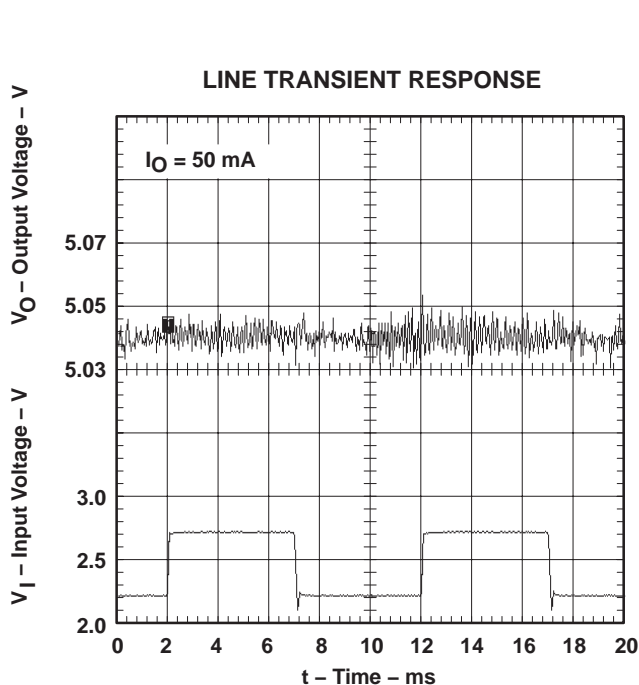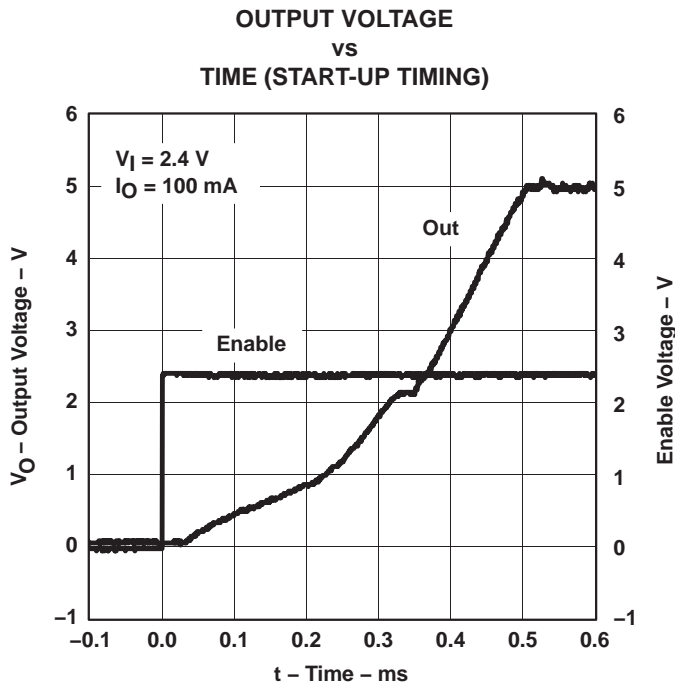
Figure 16

APPLICATION INFORMATION

capacitor selection

The TPS6014x requires only four external capacitors as shown in the basic application circuit. Their capacitance values are closely linked to the output current and output ripple requirements. For lowest ripple, low ESR (<0.1 Ω) capacitors should be used at the input and output of the charge pump.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. The input capacitor selection also depends on the output ripple requirements. C_i is recommended to be about two to four times as large as the flying capacitors. The lower the ESR of the input capacitor C_i, the lower is the output ripple.

The output capacitor C_O can be selected from 2-times to 50-times larger than the flying capacitor, depending on the ripple tolerance. The larger C_O and the lower its ESR, the lower will be the output voltage ripple.

Generally, the flying capacitors will be the smallest. Only ceramic capacitors are recommended because of their low ESR and because they retain their capacitance at the switching frequency. Please be aware that, depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U or Y5V-type capacitors will decrease in capacitance. Table 2 lists recommended capacitor values.

![Texas Instruments logo]

APPLICATION INFORMATION

capacitor selection (continued)

Table 2. Recommended Capacitor Values

I_O (mA)	C_i (μF)	$C_{(xF)}$ (μF)	C_O (μF)	V_{PP}TYP (mV)
0 – 50	4.7	2.2	4.7	40
0 – 100	4.7	2.2	10	40
0 – 100	4.7	2.2	22	18

If the measured output voltage ripple is too high for the application, improvements can be made. The first step is to increase the capacitance at the output. If the ripple is still too high, the second step would be to increase the capacitance at the input. For lower output currents, lower value flying capacitors can be used. Tables 3 and 4 lists the manufacturers of recommended capacitors.

Table 3. Recommended Capacitors

MANUFACTURER	PART NUMBER	CAPACITANCE	CASE SIZE	TYPE
Taiyo Yuden	LMK212BJ105KG–T	1 μF	0805	Ceramic
	LMK212BJ225MG–T	2.2 μF	0805	Ceramic
	LMK316BJ475KL–T	4.7 μF	1206	Ceramic
	LMK325BJ106MN–T	10 μF	1210	Ceramic
	LMK432226MM–T	22 μF	1812	Ceramic
AVX	0805ZC105KAT2A	1 μF	0805	Ceramic
	1206ZC225KAT2A	2.2 μF	1206	Ceramic

NOTE: Case code compatibility with EIA 535BAAC and CECC30801 molded chips.

Table 4. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	http://www.t–yuden.com/
AVX	X7R/X5R ceramic	http://www.avxcorp.com/

TEXAS INSTRUMENTS

APPLICATION INFORMATION

power dissipation

The power dissipated in the TPS6014x depends mainly on input voltage and output current and is described by the following:

$$P_{(DISS)} = I_O \times \left(3 \times V_I - V_O\right)$$

(5)

By observation of the above equation, it can be seen that the power dissipation is worse for the highest input voltage V_I and the highest output current I_O. For an input voltage of 3.6 V and an output current of 100 mA, the calculated power dissipation $P_{(DISS)}$ is 580 mW. This is also the point where the charge pump operates with its lowest efficiency, which is only 45%, and hence with the highest power losses.

$P_{(DISS)}$ must be less than that allowed by the package rating. The thermal resistance junction to ambient of the thermally enhanced TSSOP is 178°C/W for an unsoldered package. The thermal resistance junction to case, with the exposed thermal pad soldered to an infinitive heat sink, is 3.5°C/W.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system can be calculated as follows:

$$R_{\Theta JA}max = \frac{T_J max - T_A}{P_{(DISS)}max} = \frac{125°C - 85°C}{580 \text{ mW}} = 69°C/W$$

(6)

Using a board layout as described in the application information section, $R_{\Theta JA}$ is typically 56°C/W for an unsoldered PowerPad and 41°C/W for a soldered PowerPad.

For more information, refer to the PowerPad application report (Literature Number: SLMA002).

TEXAS
INSTRUMENTS

APPLICATION INFORMATION

layout and board space

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be soldered in close proximity to the IC. Connect ground and power ground terminals through a short, low-impedance trace. A PCB layout proposal for a two-layer board is given in Figure 17. The bottom layer of the board carries only ground potential for best performance. The layout also provides improved thermal performance as the exposed lead frame of the PowerPad package is soldered to the PCB.

An evaluation module for the TPS60140 is available and can be ordered under product code TPS60140EVM–144. The EVM uses the layout shown in Figure 17.
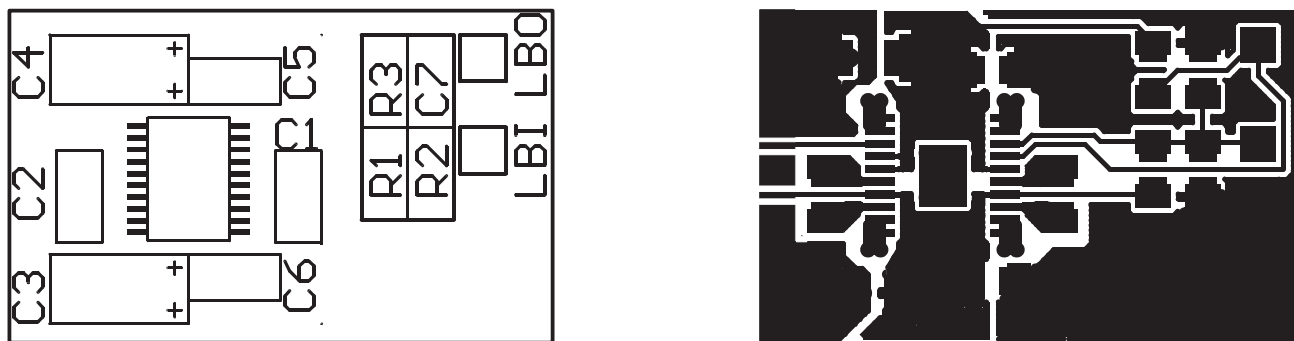
NOTE: Actual size is 15 mm x 25 mm.

Figure 17. Recommended Component Placement and Board Layout

Table 5. Component Identification

IC1	TPS6014x
C1, C2	Flying capacitors
C3, C6	Input capacitors
C4, C5	Output capacitors
C7	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO

The best performance of the converter is achieved with additional bypass capacitors C5 and C6 at the input and output. Capacitor C7 should be included if the large line transients are expected. The capacitors are not required. They can be omitted in most applications.

APPLICATION INFORMATION

related information

application reports

For more application information see:

- *PowerPAD Application Report*, Literature Number SLMA002
- *TPS6010x/TPS6011x Charge Pump Application Report*, Literature Number SLVA070

device family products

Other devices in this family are:

PART NUMBER	DESCRIPTION
TPS60100	Regulated 3.3-V, 200-mA low-noise charge pump dc-dc converter
TPS60101	Regulated 3.3-V, 100-mA low-noise charge pump dc-dc converter
TPS60110	Regulated 5-V, 300-mA low-noise charge pump dc-dc converter
TPS60111	Regulated 5-V, 150-mA low-noise charge pump dc-dc converter
TPS60120	Regulated 3.3-V, 200-mA high efficiency charge pump dc-dc converter with low-battery comparator
TPS60121	Regulated 3.3-V, 200-mA high efficiency charge pump dc-dc converter with power-good comparator
TPS60122	Regulated 3.3-V, 100-mA high efficiency charge pump dc-dc converter with low-battery comparator
TPS60123	Regulated 3.3-V, 100-mA high efficiency charge pump dc-dc converter with power-good comparator
TPS60130	Regulated 5-V, 300-mA high efficiency charge pump dc-dc converter with low-battery comparator
TPS60131	Regulated 5-V, 300-mA high efficiency charge pump dc-dc converter with power-good comparator
TPS60132	Regulated 5-V, 150-mA high efficiency charge pump dc-dc converter with low-battery comparator
TPS60133	Regulated 5-V, 150-mA high efficiency charge pump dc-dc converter with power-good comparator

![Texas Instruments logo]

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60140PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60140	Samples
TPS60140PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60140	Samples
TPS60140PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60140	Samples
TPS60140PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60140	Samples
TPS60141PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60141	Samples
TPS60141PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS60141	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60140PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS60141PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60140PWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0
TPS60141PWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0

PWP (R−PDSO−G20)   PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL PAD

SIZE AND SHAPE
SHOWN ON
SEPARATE SHEET

0,65

0,30 / 0,19   ⊕ 0,10 Ⓜ

20 · · · 11

4,50 / 4,30   6,60 / 6,20

1 · · · 10

6,60 / 6,40

0,15 NOM

Gauge Plane

Seating Plane

0°−8°

0,25

0,75 / 0,50

1,20 MAX

0,15 / 0,05

Seating Plane

△ 0,10

4073225−4/I 05/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout.   This document is available at www.ti.com <http://www.ti.com>.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         E.   Falls within JEDEC MO−153

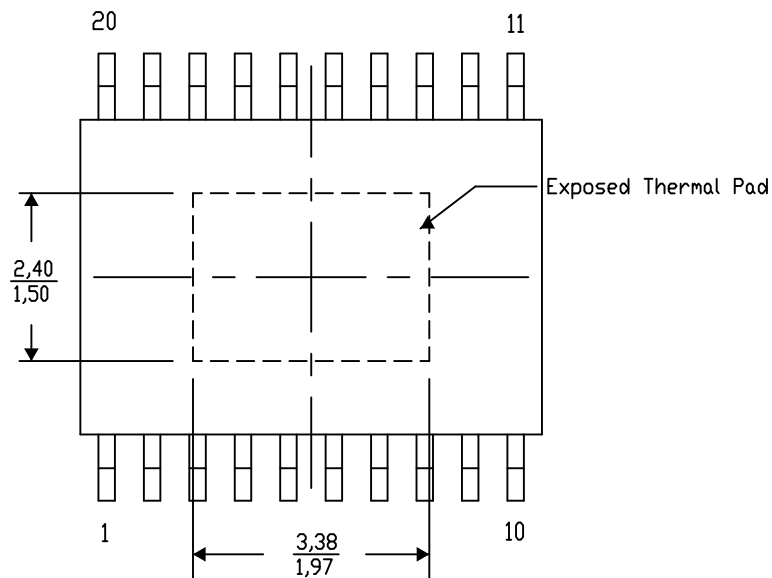**PowerPAD is a trademark of Texas Instruments.**

PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
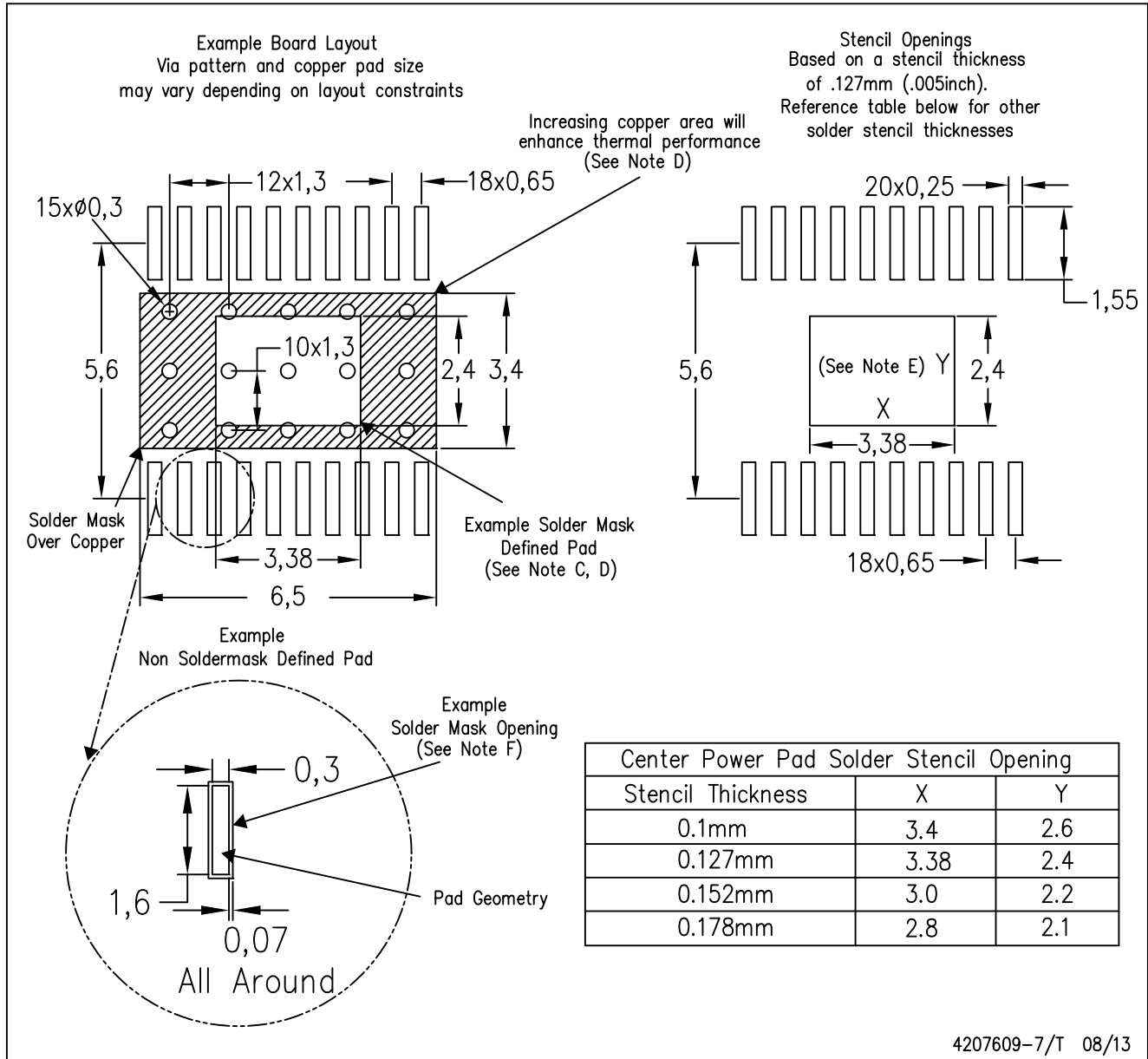

20   11

Exposed Thermal Pad

$\frac{2,40}{1,50}$

1     $\frac{3,38}{1,97}$ 10

Top View

Exposed Thermal Pad Dimensions

4206332-19/AH 11/13

NOTE: A. All linear dimensions are in millimeters

TEXAS INSTRUMENTS
www.ti.com

PWP (R-PDSO-G20)   PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

Increasing copper area will
enhance thermal performance
(See Note D)

15x⌀0,3

12x1,3   18x0,65

20x0,25

1,55

10x1,3

5,6   2,4 3,4   5,6   (See Note E) Y   2,4

X

3,38

18x0,65

Solder Mask
Over Copper

3,38

6,5

Example Solder Mask
Defined Pad
(See Note C, D)

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

0,07
All Around

Pad Geometry

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.4	2.6
0.127mm	3.38	2.4
0.152mm	3.0	2.2
0.178mm	2.8	2.1

4207609-7/T 08/13

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated