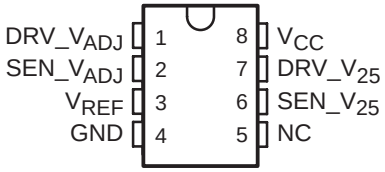
LFC789D25
DUAL LINEAR FET CONTROLLER

SLLS565B − MARCH 2003 − REVISED SEPTEMBER 2004

- **Two Independent Controllers for Regulation of:**
  - **Fixed 2.5-V and an Adjustable Output**
  - **±2% (Max) Regulation Across Temperature and Load (1 mA to 3 A)**
- **Adjustable Output Can Be Set Via an External Reference Pin, Allowing for the Creation of a Tracking Regulator**
- **Great Design Flexibility With Minimal External Components**
- **Applications: High-Current, Low-Dropout Regulators for:**
  - **DDR/RDRAM Memory Termination**
  - **Motherboards**
  - **Chipset I/O**
  - **GTLP Termination**

D OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The LFC789D25 is a dual linear FET controller that simplifies the design of dual power supplies. The device consists of two independent controllers, each of which drives an external MOSFET to implement a low-dropout regulator. One controller is programmed to regulate a fixed 2.5-V output, while the second controller can be programmed to regulate any desired output voltage via a reference input pin, allowing for the creation of a tracking regulator often needed for termination schemes. And, because heating effects of the external FETs easily can be isolated from the controllers, the controllers can regulate the output voltages to a maximum tolerance of ±2% across temperature and load.

The LFC789D25 allows designers a great deal of flexibility in selecting external components and topology to implement their specific power-supply needs. With appropriate heat sinking, the designer can build a regulator with as much current capability as allowed by the external MOSFET and power supply. And, because the dropout of the regulator simply is the product of the $R_{DS(on)}$ of the external power MOSFET and the load current, very low dropout can be achieved via proper selection of the power MOSFET.

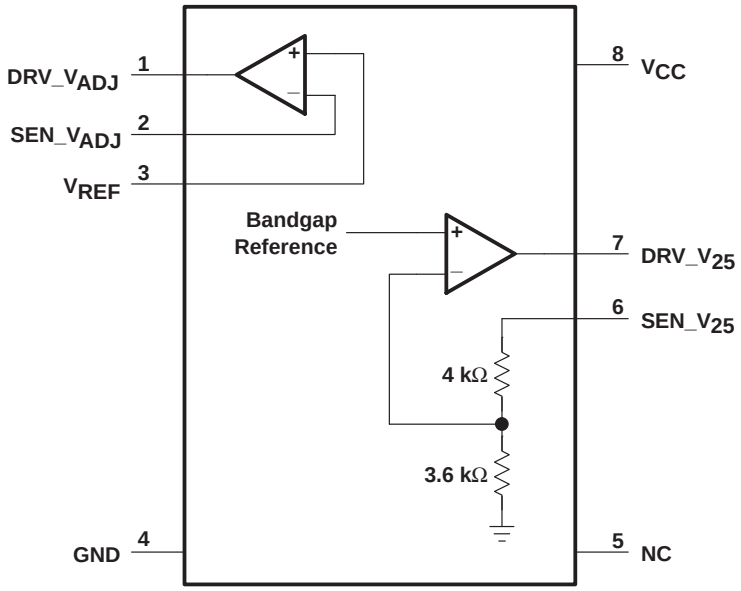
Packaged in 8-pin SOIC and space-saving TSSOP, the LFC789D25 is characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC (D)	Tube of 75	LFC789D25CD	KADAC
		Reel of 2500	LFC789D25CDR	
	TSSOP (PW)	Tube of 150	LFC789D25CPW	KADAC
		Reel of 2000	LFC789D25CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional block diagram



PIN DESCRIPTION

PIN	PIN NAME	PIN FUNCTION
1	DRV_V_{ADJ}	Output of adjustable controller. Drives gate(s) of FET(s) to output user-programmable voltage (V_{ADJ}).
2	SEN_V_{ADJ}	Sense input of adjustable controller. Senses changes in V_{ADJ}.
3	V_{REF}	Input pin used to program V_{ADJ}, allowing V_{ADJ} to track changes in V_{REF}
4	GND	Ground
5	NC	No connection
6	SEN_V_{25}	Sense Input of 2.5-V controller. Senses changes in 2.5-V supply.
7	DRV_V_{25}	Output of 2.5-V controller. Drives gate(s) of FET(s) to output fixed 2.5 V.
8	V_{CC}	Power supply for device

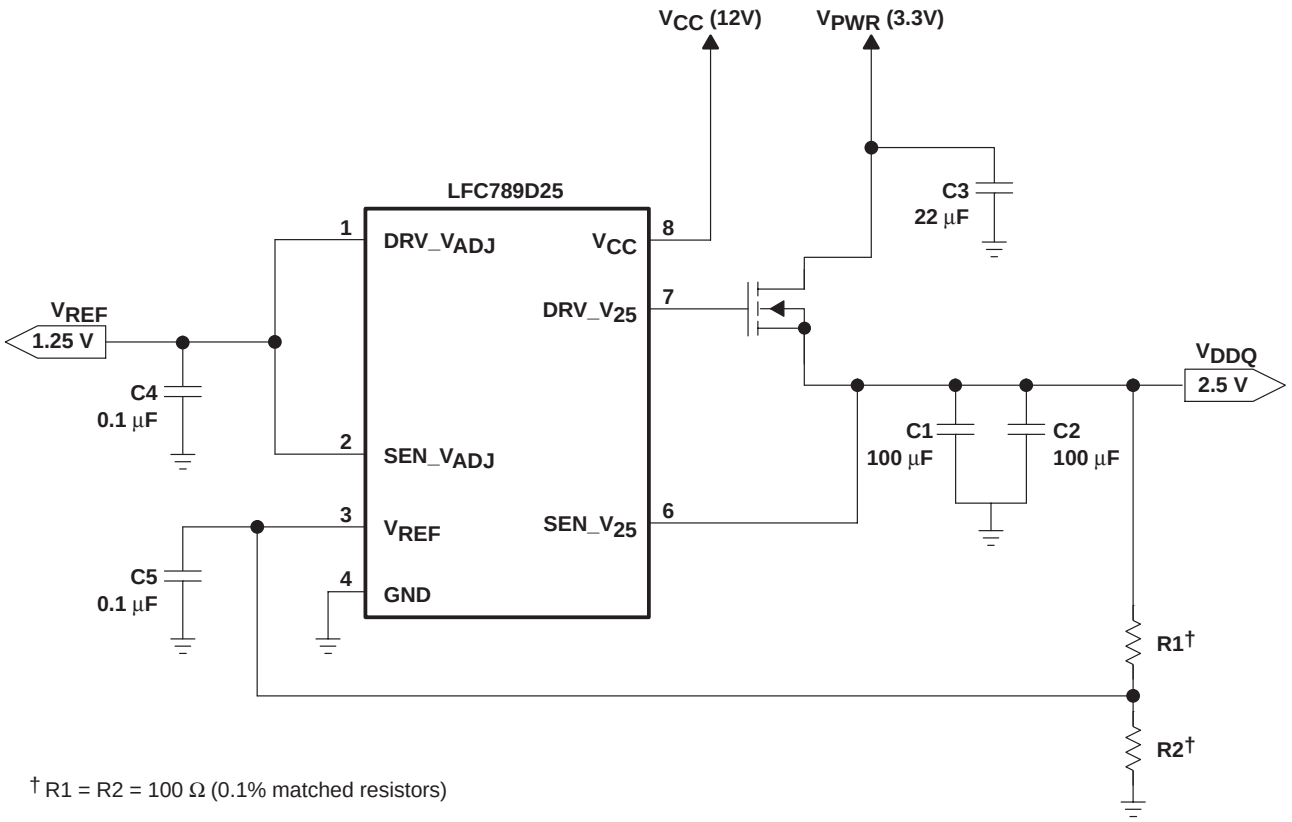


Figure 1. Typical Application Circuit for DDR1 − Memory Voltage (V_{DDQ}) and V_{REF} Buffer for DIMMs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Input voltage range, V_{REF}, SEN_V_{ADJ}, SEN_V_{25} . . . . . −0.3 V to 18 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 97°C/W
PW package . . . . . 149°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	9	16	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics, V_{CC} = 12 V ± 5%, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Sense	$I_{SEN\_V_{ADJ}}$	V_{ADJ} sense-pin current				−20		nA
				Full range			−500	
	$I_{SEN\_V_{25}}$	V_{25} sense-pin current	V_{25} = 2.5 V			125		µA
				Full range			500	
Driver	V_{DRV}	Driver output voltage	I_{DRV} = 0		V_{CC} − 1.5			V
				Full range	V_{CC} − 3			
	I_{DRV}	Driver output current	V_{DRV} = 4 V, V_{SEN} = 0.8 V_{OUT} (nom)			10		mA
				Full range	5			
Reference	$I_{V_{REF}}$	Pin current, V_{REF}				−20	−250	nA
				Full range			−500	
Output regulation (see Figure 1)		V_{25} output voltage regulation	I_{OUT} = 1 mA to 3 A, V_{PWR} = 3 .3 V ± 10%			2.5		V
				Full range	2.45	2.5	2.55	
		V_{ADJ} output voltage regulation	I_{OUT} = 1 mA to 2 A, V_{PWR} = 3.3 V ±10%, V_{REF} = V_{25}/2			V_{REF}		
				Full range	0.98 × V_{REF}	V_{REF}	1.02 × V_{REF}	
Supply	I_{CC}	Supply current				2		mA
				Full range			2.5	

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

A linear voltage regulator can be broken down into four essential building blocks: a pass transistor, a voltage reference, a feedback network, and a control circuit to drive the pass element, based on the comparison between the output voltage (as sampled by the feedback network) and the voltage reference. With the exception of the pass transistor, the -ADJ provides the other three building blocks needed. Thus, with minimal external components and low overall solution cost, a designer can create two independent, tightly regulated output voltages capable of delivering high currents in excess of 3 A (as limited by the external pass transistor). One output is fixed at 2.5 V. The other output can be adjusted to any desired voltage via an externally applied signal to the V_{REF} pin. Because the output of the regulator always tracks any changes to this V_{REF} pin, it is relatively easy to implement a tracking regulator. See the *typical application circuit* (Figure 1).

internal reference

The fixed 2.5-V output controller uses an internal temperature-compensated bandgap reference centered at 1.2 V. Its tolerance is designed to be <±2% over the specified temperature range, which, when coupled with the low offset of the driver circuit, allows the 2.5-V output to have a tolerance of 2% over the specified temperature range and full load.

external reference pin (V_{REF})

For the adjustable output controller, the V_{REF} pin allows great flexibility for the designer. Taking a simple resistor divider tied to an external voltage source and connecting the divider to the V_{REF} pin allows the controller to regulate an output voltage that is some fraction of the external voltage source. And, because any changes in the external voltage source are sensed by the voltage divider, the regulated output tracks those changes.

If a tracking regulator is not desired, a fixed voltage can be achieved by applying a constant voltage to the V_{REF} pin. This signal can be provided by a simple device such as the TL431 adjustable shunt regulator.

The V_{REF} pin typically *sources* a current of 20 nA and, as such, has a minimal loading effect on the resistor divider or the shunt regulator. The accuracy of the adjustable output depends on the accuracy of the signal applied to the V_{REF} pin. Using high-precision resistors or a TL431A (1% output tolerance) helps achieve good accuracy.

feedback network (SENSE pins)

The 2.5-V controller senses the output voltage via the SEN_V_{25} pin. This pin is tied to an internal resistor divider that essentially halves the sensed output voltage and feeds it back to the controller for comparison to the internal bandgap reference.

For the adjustable output controller, the SEN_V_{ADJ} pin provides direct feedback of the output voltage to the controller for comparison to the externally applied V_{REF} signal.

controller/driver

Both drivers essentially are error amplifiers that can output a worst-case minimum of 9 V (10.5 V at 25°C) when the LFC789D25 is powered by 12 V. This allows the controllers to regulate a large range of output voltages, as limited by the threshold voltages of the external NMOS. Both drivers sample the output voltage via a SEN pin. For the adjustable version, this SEN pin typically *sources* a current of 20 nA and, thus, has minimal loading on the output voltage. For the 2.5-V version, this SEN pin *sinks* a current of approximately 125 µA (including the currents through the internal resistor divider); this results in minimal loading on the output voltage.

Although not tested, both of these controllers are designed with very low offset (typically less than 4 mV), resulting in very accurate control of the drive signals.

APPLICATION INFORMATION

MOSFET SELECTION: BENEFITS OF NMOS PASS ELEMENTS REVISITED

A great benefit of having an external pass element is that the control circuitry can be powered by a separate supply (V_{CC}), other than the one used as the input to the pass element (V_{PWR}). This feature allows the use of an NMOS pass element, which requires a positive $V_{GS} > V_T$ for operation. With a separate V_{CC} pin to the controller, the voltage at the gate of the NMOS readily can exceed the voltage at the drain; thus, V_{GS} easily can exceed $V_{DS} + V_T$, allowing the NMOS to operate in the triode region ($V_{DS} \geq V_{GS} - V_T$). In the triode region, V_{DS} can be very small, thus achieving very low dropout.

The external NMOS selected for the pass transistor has significant impact on the overall characteristics of the regulator, as discussed in the following paragraphs.

- **Maximum output current**

  A benefit of an external pass element is that the designer can size the NMOS to easily sustain the maximum I_{OUT} expected. This allows great flexibility, along with cost and space savings, because each regulator has its pass element tailored to its individual needs. In addition, using an NMOS pass element allows for smaller size (and subsequently, lower cost) than a PMOS element for the same current-carrying ability.

- **Dropout**

  Choosing an NMOS with very low $R_{DS(on)}$ characteristics provides the regulator with very low dropout because dropout will be $\sim I_{OUT} \times R_{DS(on)}$. This lower dropout also results in better efficiency and lower heat dissipation in the pass element for a given I_{OUT}.

- **Maximum programmable output voltage and NMOS threshold voltage, V_T**

  The maximum output voltage that can be regulated by the programmable regulator depends on the device's power supply (V_{CC}) and threshold voltage (V_T) of the NMOS. With the drive voltage tied to the gate and V_{OUT} connected to the source of the NMOS, a minimum $V_{GS} = V_T$ must be maintained in order to maintain the n-channel inversion layer. The maximum V_{OUT} is calculated as follows:

  $$V_{OUT} = V_S = V_G - V_T$$

  With V_{CC} = 12 V and a corresponding worst-case gate drive voltage of 9 V, the highest achievable $V_{OUT} = 9\ V - V_T$.

- **Stability**

  A quality of the old npn regulators was their inherent stability under almost any type of load conditions and output capacitors. An NMOS regulator has the same benefit. Thus, capacitor selection and equivalent-series-resistance (ESR) values are not needed for stability, but still should be chosen properly for best transient response (see below).

capacitor selection

C_{out}: Although a minimum capacitance is not needed for stability with an NMOS pass device, higher capacitance values improve transient response. In addition, low-ESR capacitors also help transient response. Tantalum or aluminum electrolytics can be used for bulk capacitances, while ceramic bypass capacitors can be used to decouple high-frequency transients due to their low ESL (equivalent series inductance).

C_{in}: Input capacitors placed at the drain of the NMOS pass transistor (V_{PWR}) help improve the overall transient response by suppressing surges in V_{PWR} during fast load changes. Low-ESR tantalum or aluminum electrolytic capacitors can be used; higher capacitance values improve transient response. A 0.1-μF ceramic capacitor can be placed at the V_{CC} pin of the LFC789D25 to provide bypassing.

APPLICATION INFORMATION

layout

Another benefit of a separate controller and pass element is that the heat dissipated in the external NMOS can be well isolated from the controller, which has very low power dissipation. Both of these factors allow the bandgap reference and control circuitry to operate over a more stable temperature range, resulting in very good accuracy over full-load conditions. The LFC789D25 should be placed as close as possible to the external pass element because short PCB traces allow minimal EMI coupling to both the drive and sense lines.

For best accuracy, connect the SEN pins as close to the load as possible, not to the source of the NMOS. Also, place the SEN trace in the same direction and plane as the power trace that connects the source of the NMOS to the load. Also, it is good practice to keep the load current return path as far as possible from the SEN trace.

Place the 0.1-μF bypass capacitor as close as possible to the V_{CC} pin and connect it directly to the ground plane. The GND pin of the LFC789D25 should be connected to the ground plane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LFC789D25CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	KADAC	Samples
LFC789D25CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	KADAC	Samples
LFC789D25CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	KADAC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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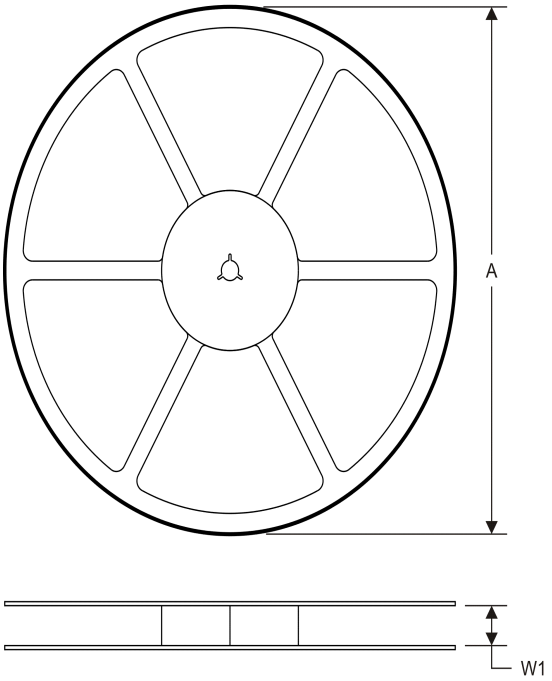
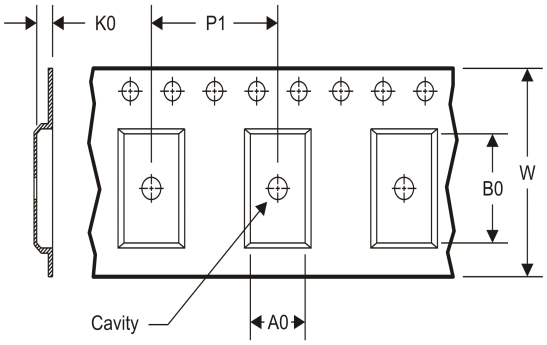
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



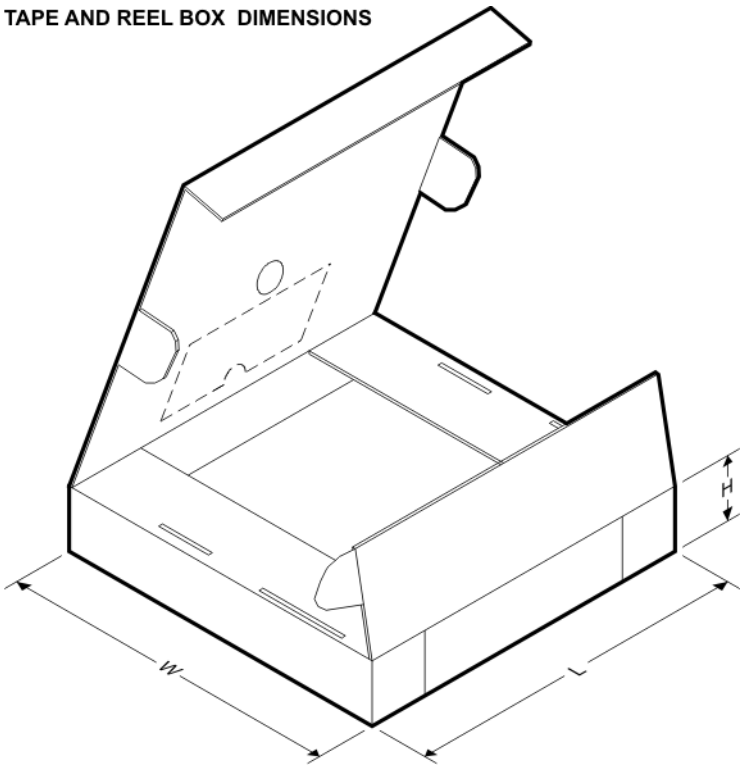
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LFC789D25CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LFC789D25CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

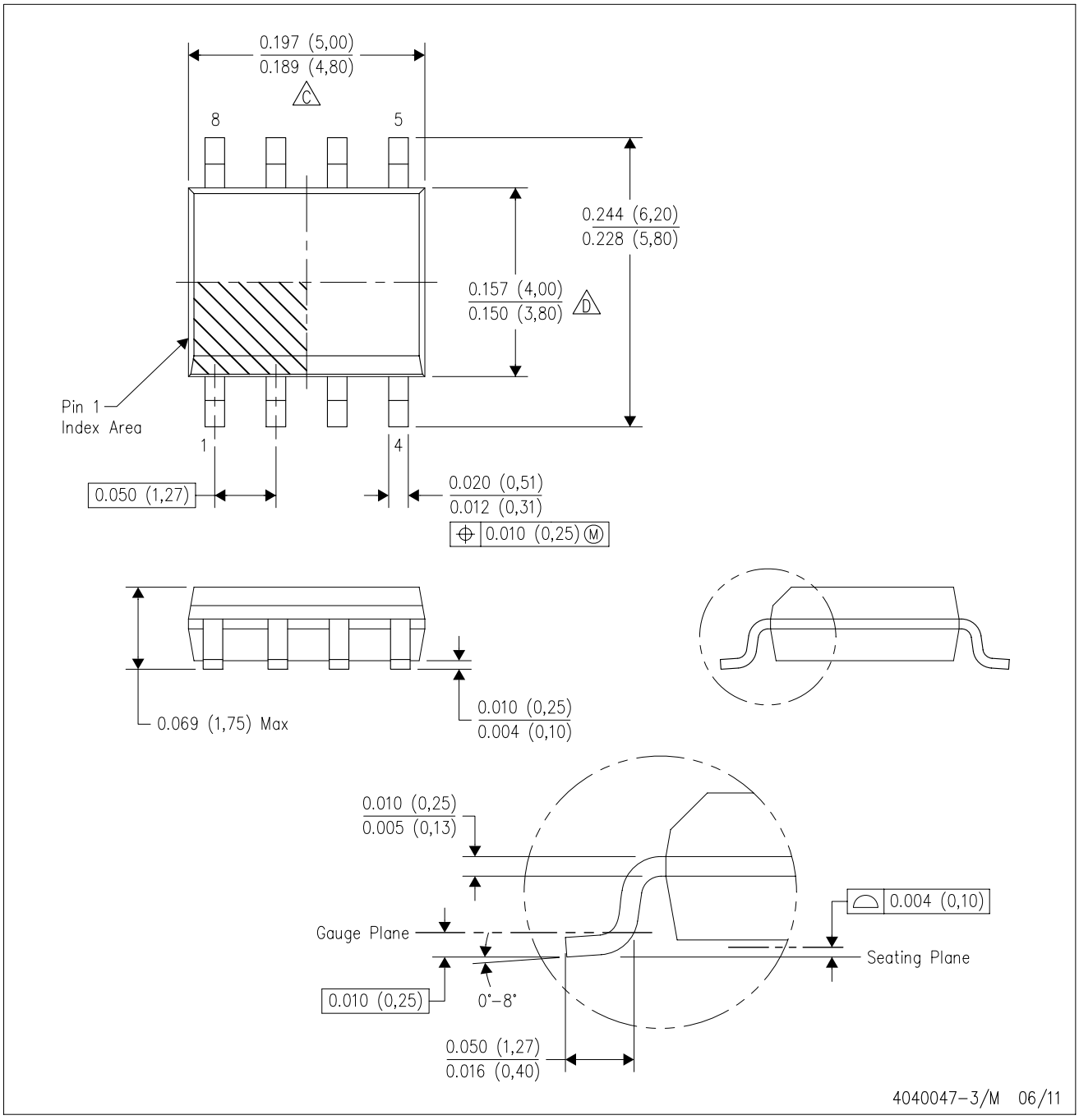
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

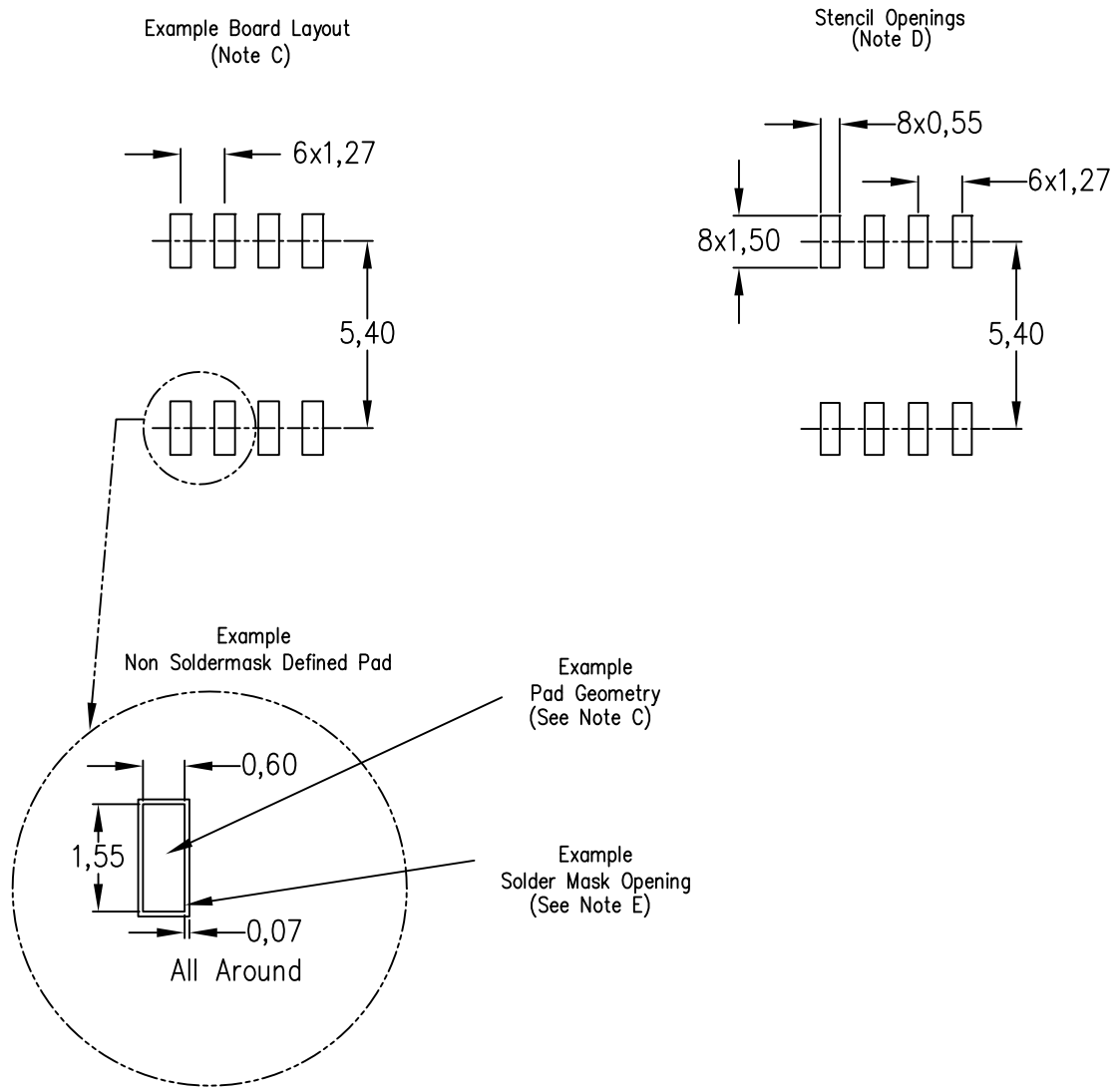
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LFC789D25CDR	SOIC	D	8	2500	340.5	338.1	20.6
LFC789D25CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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