**FEATURES**

- Guaranteed AC performance over temperature and voltage:
  - DC-to >10.7Gbps data rate throughput
  - DC-to >7GHz clock \( f_{\text{MAX}} \)
  - <220ps in-to-out \( t_{\text{pd}} \)
  - \( t_r / t_f <60ps \)
- Ultra low-jitter design:
  - <1ps\(_{\text{RMS}}\) random jitter
  - <10ps\(_{\text{PP}}\) deterministic jitter
  - <10ps\(_{\text{PP}}\) total jitter (clock)
- Minimum input swing 200mV (\( |\text{IN}–/\text{IN}| \))
- Unique, patent-pending input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, PECL, LVDS)
- Internal 50\( \Omega \) output source termination
- Typical 400mV CML output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to 85°C industrial temperature range
- Available in an ultra-small (2mm × 2mm) 8-pin MLF\( ^\circ \) package

**APPLICATIONS**

- Backplane buffering
- OC-12 to OC-192 SONET/SDN clock/data distribution
- All Gigabit Ethernet distribution
- Fibre Channel distribution

**FUNCTIONAL BLOCK DIAGRAM**

**DESCRIPTION**

The SY58600U is a 2.5V/3.3V precision, high-speed, differential receiver capable of handling clocks up to 7GHz and data streams up to 10.7Gbps.

The differential input includes Micrel’s unique, 3-pin input termination architecture that allows users to interface to any differential signal (AC or DC-coupled) as small as 200mV\(_{\text{pp}}\) without any level shifting or termination resistor networks in the signal path. The outputs are 400mV CML, with extremely fast rise/fall times guaranteed to be less than 60ps.

The SY58600U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require 800mV LVPECL outputs, consider the SY58601U or for 400mV LVPECL outputs the SY58602U. The SY58600U is part of Micrel’s high-speed, Precision Edge\( ^\circ \) product line.

All support documentation can be found on Micrel’s website at www.micrel.com.
### PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 4</td>
<td>IN, /IN</td>
<td>Differential Input: This input pair is the signal to be buffered. These inputs accept AC or DC-coupled signals as small as 100mV. Each pin of this pair internally terminates to a VT pin through 50Ω. Note that this input will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.</td>
</tr>
<tr>
<td>2</td>
<td>VT</td>
<td>Input Termination Center-Tap: Each side of the differential input pair terminates to this pin. The VT pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.</td>
</tr>
<tr>
<td>3</td>
<td>VREF-AC</td>
<td>Reference Output Voltage: This output biases to ( V_{CC} - 1.2V ). Connect to VT pin when AC-coupling the input. Bypass with 0.01μF low ESR capacitor to ( V_{CC} ). Maximum current source or sink is 0.5mA. See “Input Interface Applications” section.</td>
</tr>
<tr>
<td>8</td>
<td>VCC</td>
<td>Positive Power Supply. Bypass with 0.1μF</td>
</tr>
<tr>
<td>7, 6</td>
<td>Q, /Q</td>
<td>Differential CML Output: Differential buffered output copy of the input signal. The differential output swing is typically 800mV into a 50Ω load, or 100Ω across the pair. See “Output Interface Applications” section.</td>
</tr>
<tr>
<td>5</td>
<td>GND, Exposed</td>
<td>Ground. Ground pin and exposed pad must be connected to the same ground plane.</td>
</tr>
</tbody>
</table>

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Type</th>
<th>Operating Range</th>
<th>Package Marking</th>
<th>Lead Finish</th>
</tr>
</thead>
<tbody>
<tr>
<td>SY58600UMITR(2)</td>
<td>MLF-8</td>
<td>Industrial</td>
<td>600</td>
<td>Sn-Pb</td>
</tr>
<tr>
<td>SY58600UMGTR(2, 3)</td>
<td>MLF-8</td>
<td>Industrial</td>
<td>600 with Pb-Free bar-line indicator</td>
<td>Pb-Free NiPdAu</td>
</tr>
</tbody>
</table>

**Notes:**
1. Contact factory for die availability. Dice are guaranteed at \( T_A = 25°C \), DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.
Absolute Maximum Ratings\(^{(1)}\)

Supply Voltage (\(V_{CC}\)) \(-0.5\,\text{V to } +4.0\,\text{V}\)
Input Voltage (\(V_{IN}\)) \(-0.5\,\text{V to } V_{CC}\)
CML Output Voltage (\(V_{OUT}\)) \(V_{CC} - 1.0\,\text{V to } V_{CC} + 0.5\,\text{V}\)

Termination Current (3)
- Source or Sink Current on \(V_T\) \(\pm 100\,\text{mA}\)
- Source or Sink Current on \(\text{IN, } \text{/IN}\) \(\pm 50\,\text{mA}\)
- Current (\(V_{\text{REF}}\))
  - Source or Sink Current on \(V_{\text{REF}} - \text{AC}\) \(\pm 1.5\,\text{mA}\)

Lead Temperature (soldering, 20 sec.) \(+260\,\degree\text{C}\)
Storage Temperature (\(T_S\)) \(-65\,\degree\text{C to } +150\,\degree\text{C}\)

Operating Ratings\(^{(2)}\)

Supply Voltage (\(V_{CC}\)) \(+2.375\,\text{V to } +2.625\,\text{V or}\)
\(+3.0\,\text{V to } +3.6\,\text{V}\)
Ambient Temperature (\(T_A\)) \(-40\,\degree\text{C to } +85\,\degree\text{C}\)

Package Thermal Resistance\(^{(4)}\)
- MLF\(^\text{®}\) (\(\theta_{JA}\))
  - Still-Air \(93\,\text{°C/W}\)
- MLF\(^\text{®}\) (\(\psi_{JB}\))
  - Junction-to-Board \(32\,\text{°C/W}\)

DC ELECTRICAL CHARACTERISTICS\(^{(5)}\)

\(T_A = -40\,\degree\text{C to } +85\,\degree\text{C, unless otherwise noted.}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>Power Supply</td>
<td>(V_{CC} = 2.5,\text{V})</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>(I_{CC})</td>
<td>Power Supply Current</td>
<td>No Load, max. (V_{CC}), \text{Note 6}</td>
<td>45</td>
<td>65</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(R_{\text{DIFF_IN}})</td>
<td>Differential Input Resistance ((\text{IN-to-} \text{/IN}))</td>
<td></td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(R_{\text{IN}})</td>
<td>Input Resistance ((\text{IN-to-V_T, } \text{/IN-to-V_T}))</td>
<td></td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(V_{\text{IH}})</td>
<td>Input HIGH Voltage ((\text{IN, } \text{/IN}))</td>
<td>(V_{CC} - 1.6,\text{V})</td>
<td>1.28</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{IL}})</td>
<td>Input LOW Voltage ((\text{IN, } \text{/IN}))</td>
<td></td>
<td>0</td>
<td>(V_{\text{IH}} - 0.1,\text{V})</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{IN}})</td>
<td>Input Voltage Swing ((\text{IN, } \text{/IN}))</td>
<td>See Figure 1a.</td>
<td>0.2</td>
<td>1.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{DIFF_IN}})</td>
<td>Differential Input Voltage Swing ([\text{IN-}, \text{IN}])</td>
<td>See Figure 1b.</td>
<td>0.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{T\text{-IN}})</td>
<td>In-to-V_T ((\text{IN, } \text{/IN}))</td>
<td></td>
<td>1.28</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{REF-AC}})</td>
<td>Output Reference Voltage</td>
<td>(V_{CC} - 1.3)</td>
<td>(V_{CC} - 1.2)</td>
<td>(V_{CC} - 1.1)</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Permanent device damage may occur if the ratings in “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. \(\psi_{JB}\) uses 4-layer \(\theta_{JA}\) in still-air, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Includes current through internal 50\(\Omega\) pull-ups.
7. \(V_{\text{IH}}\) (min) not lower than 1.2V.
### CML OUTPUTS DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 100\Omega$ across output pair or equivalent, unless otherwise noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output HIGH Voltage $Q, /Q$</td>
<td>$V_{CC}-0.020$ to $V_{CC}-0.010$</td>
<td></td>
<td></td>
<td></td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage Swing $Q, /Q$</td>
<td></td>
<td>325</td>
<td>400</td>
<td></td>
<td>$mV$</td>
</tr>
<tr>
<td>$V_{DIFF_OUT}$</td>
<td>Differential Output Voltage Swing $Q, /Q$</td>
<td></td>
<td>650</td>
<td>800</td>
<td></td>
<td>$mV$</td>
</tr>
<tr>
<td>$R_{OUT}$</td>
<td>Output Source Impedance $Q, /Q$</td>
<td></td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>$\Omega$</td>
</tr>
</tbody>
</table>

### AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 100\Omega$ across output pair or equivalent, unless otherwise noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Maximum Operating Frequency</td>
<td>NRZ Data $V_{OUT} \geq 200mV$ Clock</td>
<td>10.7</td>
<td></td>
<td></td>
<td>$Gbps$</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>Propagation Delay</td>
<td>IN-to-$Q$</td>
<td>70</td>
<td>125</td>
<td>220</td>
<td>$ps$</td>
</tr>
<tr>
<td>$t_{pd_Tempco}$</td>
<td>Differential Propagation Delay Temperature Coefficient</td>
<td></td>
<td>115</td>
<td></td>
<td></td>
<td>$fs/^\circ C$</td>
</tr>
<tr>
<td>$t_{JITTER}$</td>
<td>Data Random Jitter (RJ)</td>
<td>Note 10</td>
<td>1</td>
<td></td>
<td></td>
<td>$ps_{RMS}$</td>
</tr>
<tr>
<td></td>
<td>Deterministic Jitter (DJ)</td>
<td>Note 11</td>
<td>10</td>
<td></td>
<td></td>
<td>$ps_{PP}$</td>
</tr>
<tr>
<td></td>
<td>Clock Cycle-to-Cycle Jitter</td>
<td>Note 12</td>
<td>1</td>
<td></td>
<td></td>
<td>$ps_{RMS}$</td>
</tr>
<tr>
<td></td>
<td>Total Jitter (TJ)</td>
<td>Note 13</td>
<td>10</td>
<td></td>
<td></td>
<td>$ps_{PP}$</td>
</tr>
<tr>
<td>$t_r, t_f$</td>
<td>Output Rise/Fall Times $Q, /Q$</td>
<td>(20% to 80%) At full output swing.</td>
<td>20</td>
<td>40</td>
<td>60</td>
<td>$ps$</td>
</tr>
</tbody>
</table>

**Notes:**
8. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
9. High frequency AC electricals are guaranteed by design and characterization.
10. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.
11. Deterministic jitter is measured at 2.5Gbps/3.2Gbps with both K28.5 and $2^{23-1}$ PRBS pattern.
12. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_{n}-T_{n-1}$, where $T$ is the time between rising edges of the output signal.
13. Total jitter definition: with an ideal clock input of frequency $\leq f_{MAX}$, no more than one output edge in $10^{12}$ output edges will deviate by more than the specified peak-to-peak jitter value.
DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWINGS

**Figure 1a. Single-Ended Swing**

V<sub>IN</sub>, V<sub>OUT</sub>
400mV (typical)

**Figure 1b. Differential Swing**

V<sub>DIFF_IN</sub>, V<sub>DIFF_OUT</sub>
800mV (typical)

INPUT AND OUTPUT STAGE INTERNAL TERMINATION

**Figure 2a. Simplified Differential Input Stage**

**Figure 2b. Simplified Differential Output Stage**
**TYPICAL OPERATING CHARACTERISTICS**

$V_{CC} = 3.3\, \text{V}$, $GND = 0$, $V_{IN} = 800\, \text{mV}$.

- **200MHz Clock**
  - Output Swing (100mV/div.)
  - TIME (500ps/div.)

- **1xGBE Mask $2^{23-1}$**
  - Output Swing (100mV/div.)
  - TIME (200ps/div.)

- **OC-12 Mask $2^{23-1}$ PRBS**
  - Output Swing (100mV/div.)
  - TIME (300ps/div.)

- **2xGBE Mask $2^{23-1}$ PRBS**
  - Output Swing (100mV/div.)
  - TIME (100ps/div.)

- **2xFC Mask $2^{23-1}$ PRBS**
  - Output Swing (100mV/div.)
  - TIME (100ps/div.)

- **OC-192 Mask $2^{23-1}$ PRBS**
  - Output Swing (100mV/div.)
  - TIME (20ps/div.)
**TYPICAL OPERATING CHARACTERISTICS CONT’D**

$V_{CC} = 3.3\text{V}$, $GND = 0$, $V_{IN} = 800\text{mV}$.

**10xGBE Mask $2^{23}-1$ PRBS**

- **Output Swing** (100mV/div.)
- **TIME** (15ps/div.)
INPUT INTERFACE APPLICATIONS

**Figure 3a. CML Interface (DC-Coupled)**

Option: \( V_T \) may be connected to \( V_{CC} \).

**Figure 3b. CML Interface (AC-Coupled)**

**Figure 3c. LVPECL Interface (DC-Coupled)**

**Figure 3d. LVPECL Interface (AC-Coupled)**

**Figure 3e. LVDS Interface**
**OUTPUT INTERFACE APPLICATIONS**

**Figure 4a. CML DC-Coupled Termination**

**Figure 4b. CML DC-Coupled Termination**

**Figure 4c. CML AC-Coupled Termination**

**RELATED PRODUCT AND SUPPORT DOCUMENTATION**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Function</th>
<th>Data Sheet Link</th>
</tr>
</thead>
<tbody>
<tr>
<td>SY58601U</td>
<td>2.5V/3.3V 5Gbps Differential 800mV LVPECL Line Driver/Receiver with Internal Termination</td>
<td><a href="http://www.micrel.com/product-info/products/sy58601u.shtml">www.micrel.com/product-info/products/sy58601u.shtml</a></td>
</tr>
<tr>
<td>SY58602U</td>
<td>2.5V/3.3V 10.7Gbps Differential 400mV LVPECL Line Driver/Receiver with Internal Termination</td>
<td><a href="http://www.micrel.com/product-info/products/sy58602u.shtml">www.micrel.com/product-info/products/sy58602u.shtml</a></td>
</tr>
<tr>
<td></td>
<td>MLF™ Application Note</td>
<td><a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a></td>
</tr>
</tbody>
</table>
8-PIN ULTRA-SMALL EPAD MicroLeadFrame® (MLF-8)

Package Notes:
1. Package meets Level 2 qualification.
2. All parts dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

PCB Thermal Consideration for 8-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)