



July 2014

# FDFMA2N028Z

## Integrated N-Channel PowerTrench<sup>®</sup> MOSFET and Schottky Diode

20V, 3.7A, 68mΩ

### Features

#### MOSFET

- Max  $r_{DS(on)}$  = 68mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 3.7A$
- Max  $r_{DS(on)}$  = 86mΩ at  $V_{GS} = 2.5V$ ,  $I_D = 3.3A$
- HBM ESD protection level > 2kV (Note 3)

#### Schottky

- $V_F < 0.37V$  @ 500mA
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- RoHS Compliant



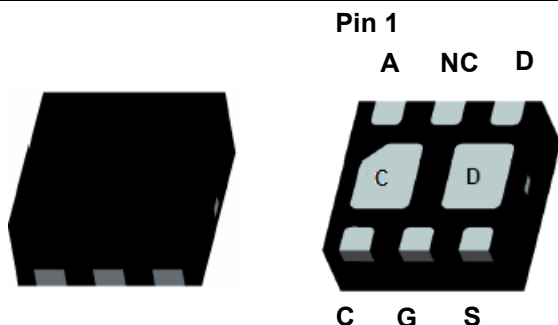
### General Description

This device is designed specifically as a single package solution for a boost topology in cellular handset and other ultra-portable applications. It features a MOSFET with low on-state resistance, and an independently connected schottky diode with low forward voltage.

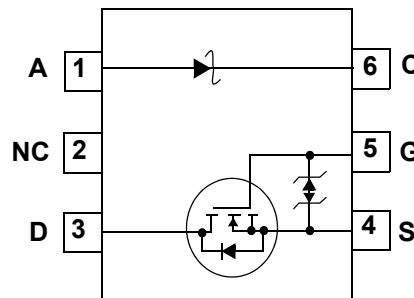
The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

### Application

- DC - DC Conversion



MicroFET 2X2



### MOSFET Maximum Ratings $T_J = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	20	V
$V_{GS}$	Gate to Source Voltage	$\pm 12$	V
$I_D$	Drain Current -Continuous (Note 1a)	3.7	A
	-Pulsed	6	
$P_D$	Power Dissipation (Note 1a)	1.4	W
	Power Dissipation (Note 1b)	0.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$
$V_{RR}$	Schottky Repetitive Peak Reverse Voltage	20	V
$I_O$	Schottky Average Forward Current	2	A

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	86	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	173	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	86	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	140	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.N28	FDFMA2N028Z	MicroFET 2X2	7"	8mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		15		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	0.6	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-4		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\text{V}, I_D = 3.7\text{A}$		37	68	$\text{m}\Omega$
		$V_{GS} = 2.5\text{V}, I_D = 3.3\text{A}$		50	86	
		$V_{GS} = 4.5\text{V}, I_D = 3.7\text{A}, T_J = 125^\circ\text{C}$		53	90	
$g_{FS}$	Forward Trans conductance	$V_{DS} = 10\text{V}, I_D = 3.7\text{A}$		16		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$		340	455	$\text{pF}$
$C_{oss}$	Output Capacitance			80	110	$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance			60	90	$\text{pF}$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{V}, I_D = 1\text{A}$ $V_{GS} = 4.5\text{V}, R_{GEN} = 6\Omega$		8	16	ns
$t_r$	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			14	26	ns
$t_f$	Fall Time			3	6	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{DS} = 10\text{V}, I_D = 3.7\text{A}$		4	6
$Q_{gs}$	Gate to Source Gate Charge	$V_{GS} = 4.5\text{V}$		0.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.1		nC

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				1.1	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1.1\text{A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 3.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$		11		ns
$Q_{rr}$	Reverse Recovery Charge			2		nC

### Schottky Diode Characteristics

$V_R$	Reverse Voltage	$I_R = 1\text{mA}$	$T_J = 25^\circ\text{C}$	20			V
$I_R$	Reverse Leakage	$V_R = 20\text{V}$	$T_J = 25^\circ\text{C}$		30	300	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	45	mA
$V_F$	Forward Voltage	$I_F = 500\text{mA}$	$T_J = 25^\circ\text{C}$		0.32	0.37	V
			$T_J = 125^\circ\text{C}$		0.21	0.26	
		$I_F = 1\text{A}$	$T_J = 25^\circ\text{C}$		0.37	0.435	
			$T_J = 125^\circ\text{C}$		0.28	0.33	

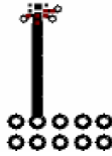
## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

### Notes:

- 1:  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz. copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
  - (a) MOSFET  $R_{\theta JA} = 86^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper,  $1.5'' \times 1.5'' \times 0.062''$  thick PCB.
  - (b) MOSFET  $R_{\theta JA} = 173^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.
  - (c) Schottky  $R_{\theta JA} = 86^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper,  $1.5'' \times 1.5'' \times 0.062''$  thick PCB.
  - (d) Schottky  $R_{\theta JA} = 140^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.



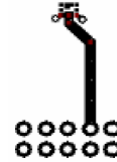
a)  $86^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.



b)  $173^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.



c)  $86^\circ\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.

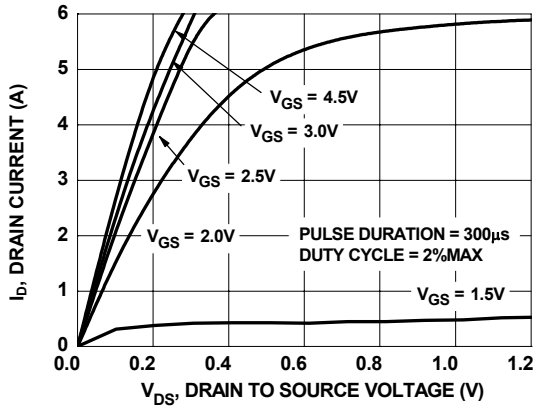


d)  $140^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

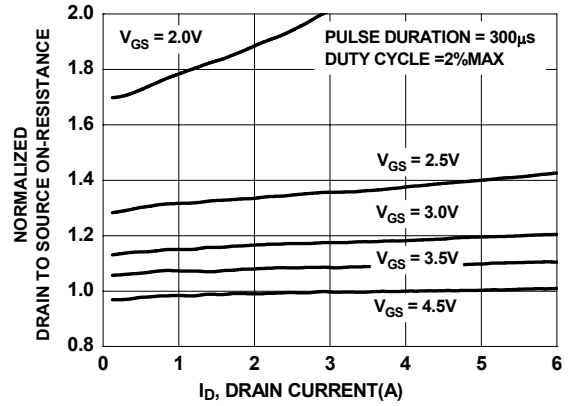
2: Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3: The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

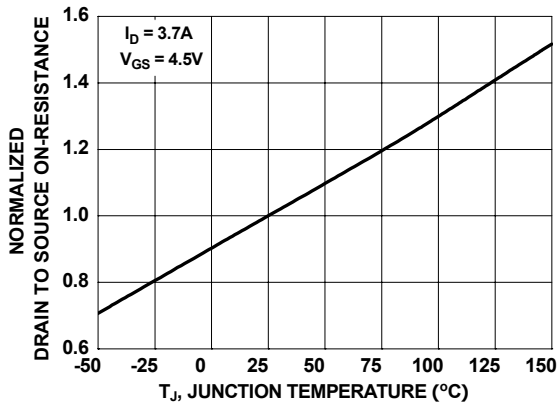
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



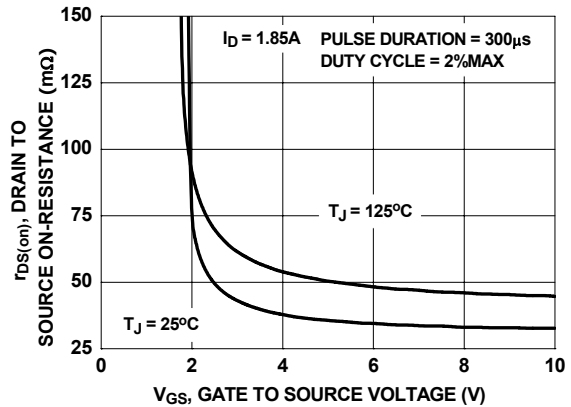
**Figure 1. On-Region Characteristics**



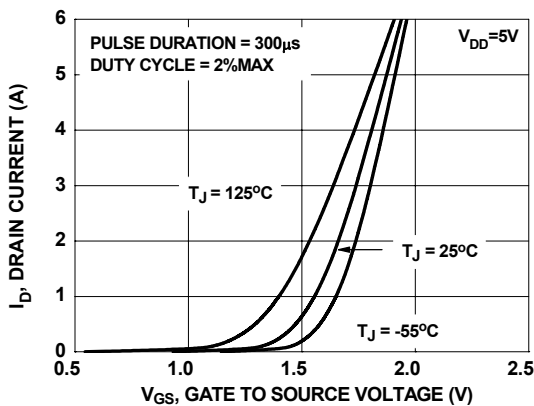
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



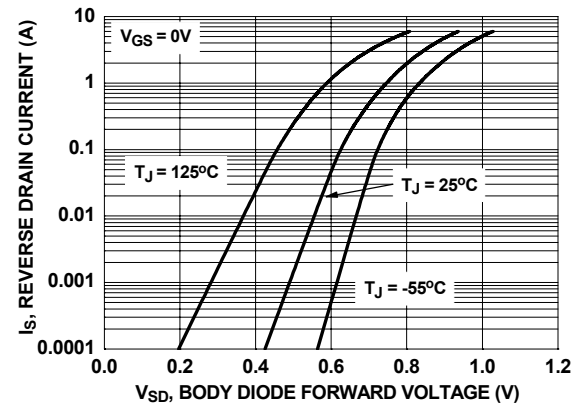
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

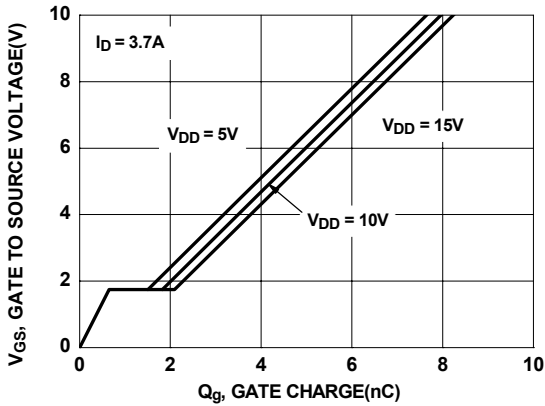


**Figure 5. Transfer Characteristics**

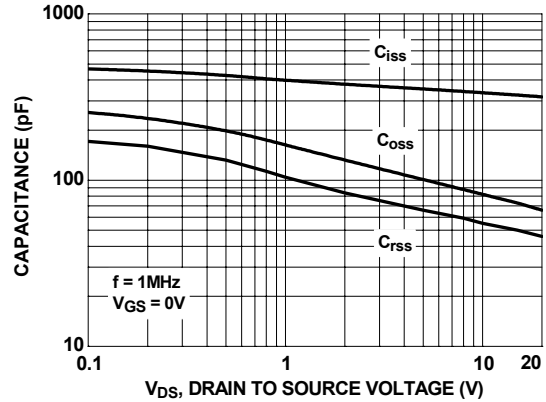


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

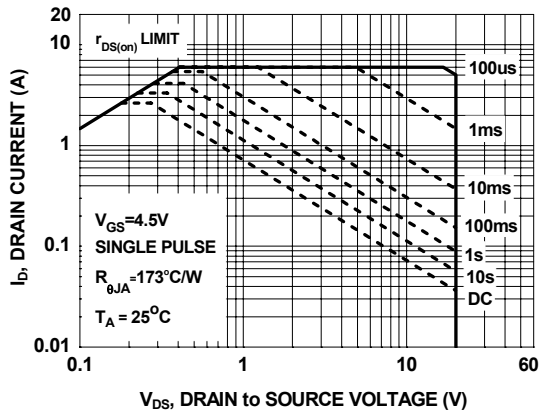
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



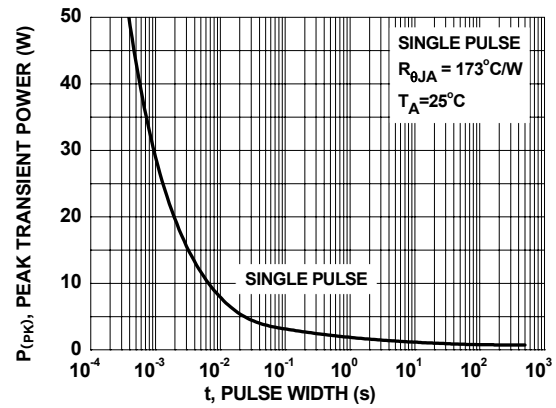
**Figure 7. Gate Charge Characteristics**



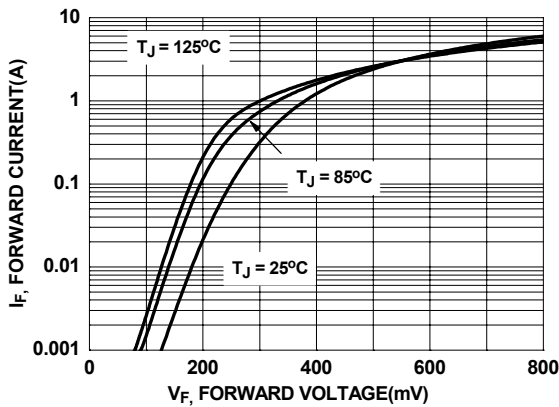
**Figure 8. Capacitance Characteristics**



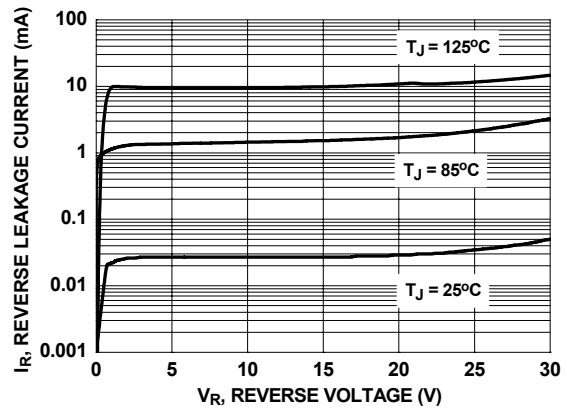
**Figure 9. Forward Bias Safe Operating Area**



**Figure 10. Single Pulse Maximum Power Dissipation**

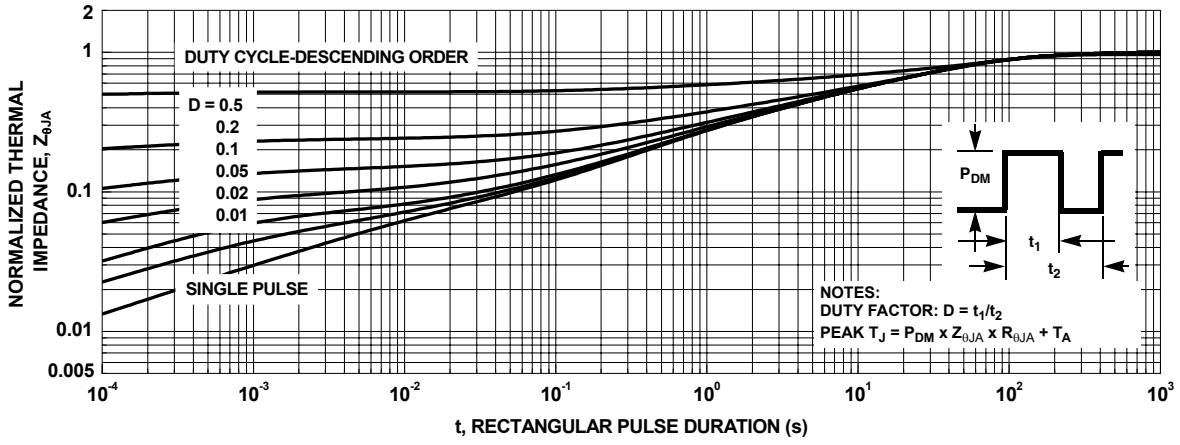


**Figure 11. Schottky Diode Forward Current**

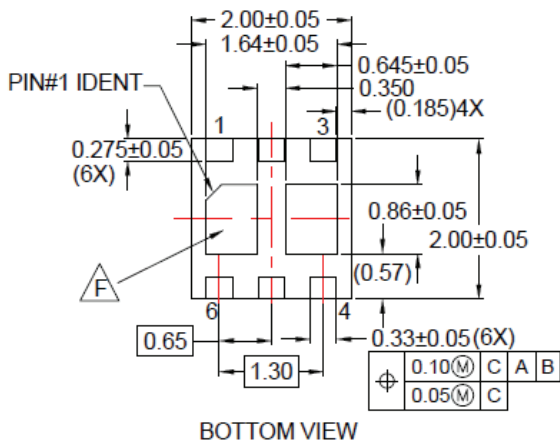
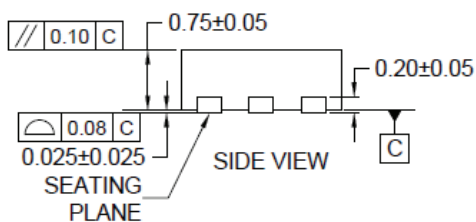
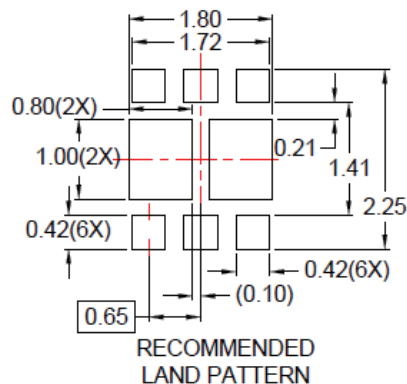
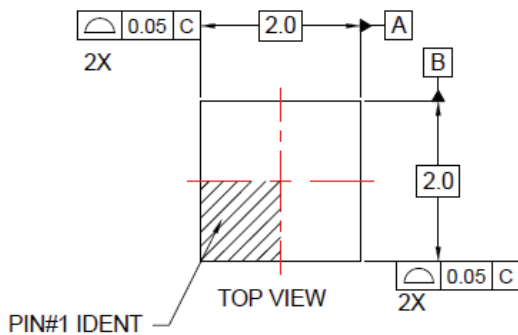


**Figure 12. Schottky Diode Reverse Current**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



## Dimensional Outline and Pad Layout



### NOTES:

- A. CONFORM TO JADEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
  - D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
  - E. DRAWING FILENAME: MKT-UMLP16Erev4
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Rev. I68