58V, 2A Step-Down µModule Regulator

FEATURES

- **Wide Input Voltage Range: 3.6V to 58V (60V Absolute Maximum)**
- **Up to 2A Output Current**
- **Parallelable for Increased Output Current**
- **0.8V to 24V Output Voltage**
- **Adjustable Switching Frequency: 100kHz to 2.4MHz**
- Configurable as an Inverter
- Current Mode Control
- Programmable Soft-Start
- 9mm × 15mm × 4.92mm BGA Package

APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

DESCRIPTION

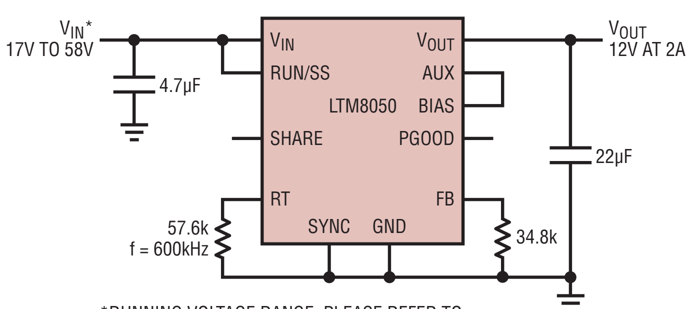
The LTM®8050 is a 58V_{IN}, 2A step down µModule® (micromodule) converter. Included in the package are the switching controller, power switches, inductor and all support components. Operating over an input voltage range of 3.6V to 58V, the LTM8050 supports an output voltage range of 0.8V to 24V and a switching frequency range of 100kHz to 2.4MHz, each set by a single resistor. Only the bulk input and output filter capacitors are needed to finish the design.

The LTM8050 is packaged in a 9mm × 15mm × 4.92mm ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8050 is available with SnPb (BGA) or RoHS compliant terminal finish.

Click to view associated TechClip Videos.

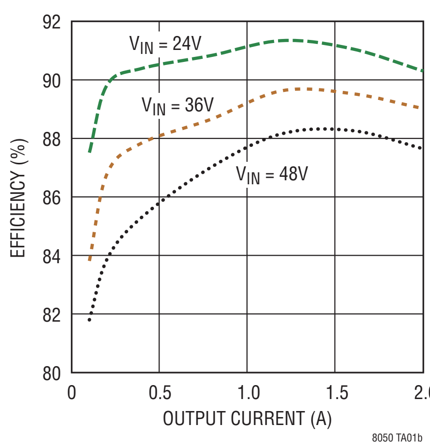
TYPICAL APPLICATION

12V_{OUT}, 2A µModule Regulator



*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS

Efficiency vs Output Current, 12V_{OUT}



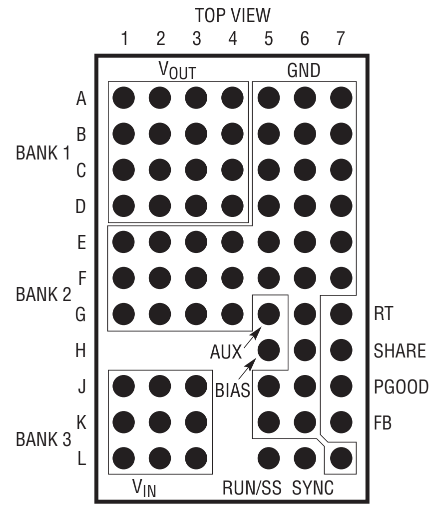
8050fb

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 3)

V_{IN}, RUN/SS Voltage 60V
FB, RT, SHARE Voltage 5V
V_{OUT}, AUX 25V
PGOOD, SYNC, BIAS 25V
V_{IN} + BIAS 72V
Maximum Junction Temperature (Note 2) .... 125°C
Solder Temperature... 245°C
Storage Temperature... 125°C

PIN CONFIGURATION



BGA PACKAGE
70-PIN (15mm × 9mm × 4.92mm)
T_{JMAX} = 125°C, θ_{JA} = 24.4°C/W, $\theta_{JC(BOTTOM)}$ = 11.5°C/W,
$\theta_{JC(TOP)}$ = 42.7°C/W, θ_{JB} = 18.7°C/W
θ VALUES DETERMINED PER JESD51-9, MAX OUTPUT POWER
WEIGHT = 1.8 GRAMS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM8050EY#PBF	SAC305 (RoHS)	LTM8050Y	e1	BGA	3	–40°C to 125°C
LTM8050IY#PBF	SAC305 (RoHS)	LTM8050Y	e1	BGA	3	–40°C to 125°C
LTM8050IY	SnPb (63/37)	LTM8050Y	e0	BGA	3	–40°C to 125°C
LTM8050MPY#PBF	SAC305 (RoHS)	LTM8050Y	e1	BGA	3	–55°C to 125°C
LTM8050MPY	SnPb (63/37)	LTM8050Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN/SS = 12V, BIAS = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●			3.6	V
Output DC Voltage	0 < I_{OUT} ≤ 2A; R_{FB} Open 0 < I_{OUT} ≤ 2A; R_{FB} = 16.9k; V_{IN} = 32V			0.8 24		V V
Output DC Current			0		2	A
Quiescent Current into V_{IN}	RUN/SS = 0V Not Switching BIAS = 0V, Not Switching			0.01 35 120	1 60 160	µA µA µA
Quiescent Current into BIAS	RUN/SS = 0V Not Switching BIAS = 0V, Not Switching			0.01 82 1	0.5 120 5	µA µA µA
Line Regulation	5.5V < V_{IN} < 58V, I_{OUT} = 1A			0.3		%
Load Regulation	0A < I_{OUT} < 2A			0.3		%
Output Voltage Ripple (RMS)	0A < I_{OUT} < 2A			10		mV
Switching Frequency	R_T = 45.3k			750		kHz
Voltage (at FB Pin)		 ●	775 770	790	805 810	mV mV
Internal Feedback Resistor				499		kΩ
Minimum BIAS Voltage for Proper Operation					2.8	V
RUN/SS Pin Current	RUN/SS = 2.5V			6	10	µA
RUN Input High Voltage			2.5			V
RUN Input Low Voltage					0.2	V
PGOOD Threshold (at FB Pin)	V_{OUT} Rising			730		mV
PGOOD Leakage Current	PGOOD = 30V			0.1	1	µA
PGOOD Sink Current	PGOOD = 0.4V		200	600		µA
SYNC Input Low Threshold	f_{SYNC} = 550kHz				0.5	V
SYNC Input High Threshold	f_{SYNC} = 550kHz		0.7			V
SYNC Bias Current	SYNC = 0V			0.1		µA

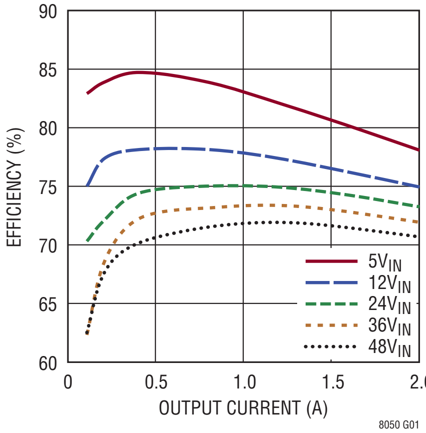
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM8050E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8050I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8050MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

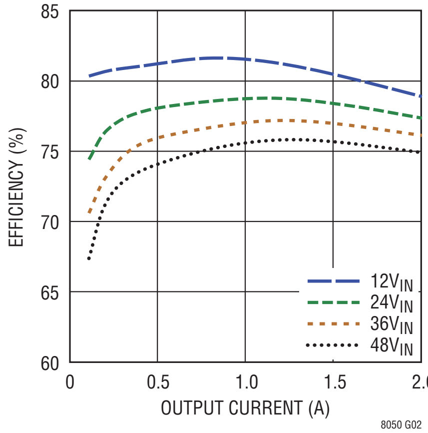
Note 3: Unless otherwise noted, the absolute minimum voltage is zero.

TYPICAL PERFORMANCE CHARACTERISTICS Operating conditions are per Table 1 and T_A = 25°C, unless otherwise noted.

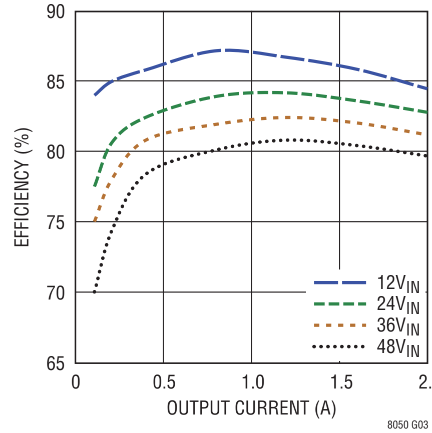
Efficiency vs Output Current, 2.5V$_{OUT}$



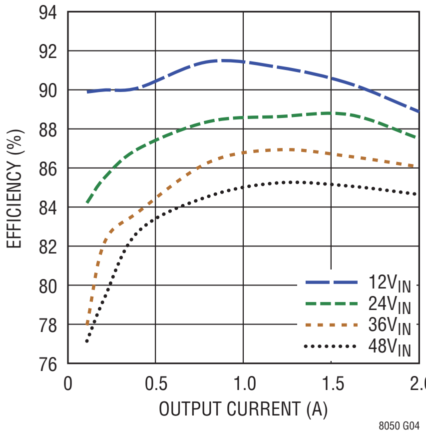
Efficiency vs Output Current, 3.3V$_{OUT}$



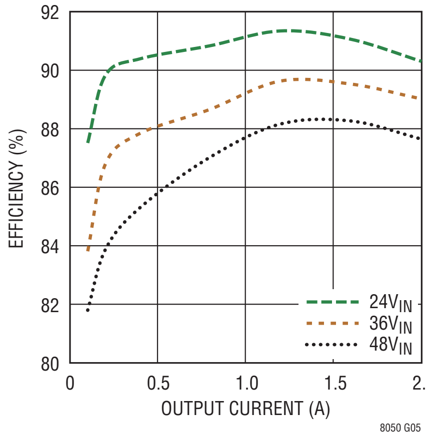
Efficiency vs Output Current, 5V$_{OUT}$



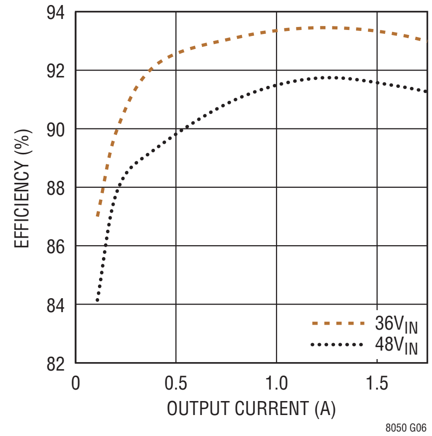
Efficiency vs Output Current, 8V$_{OUT}$



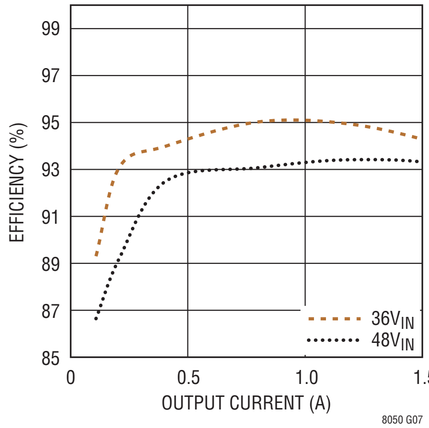
Efficiency vs Output Current, 12V$_{OUT}$



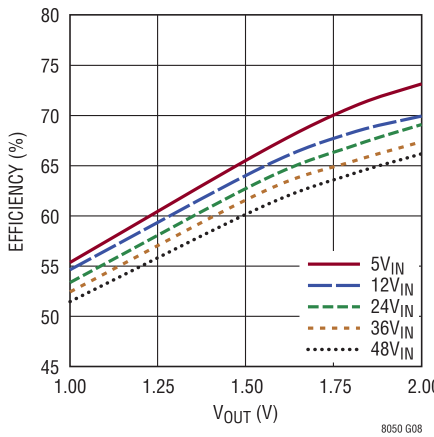
Efficiency vs Output Current, 18V$_{OUT}$



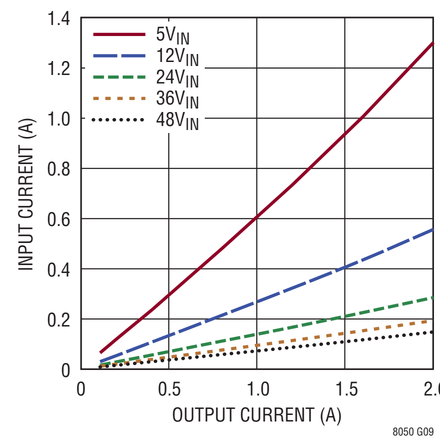
Efficiency vs Output Current, 24V$_{OUT}$



Efficiency, V$_{OUT}$ ≤ 2V, 2A Load, BIAS = 5V



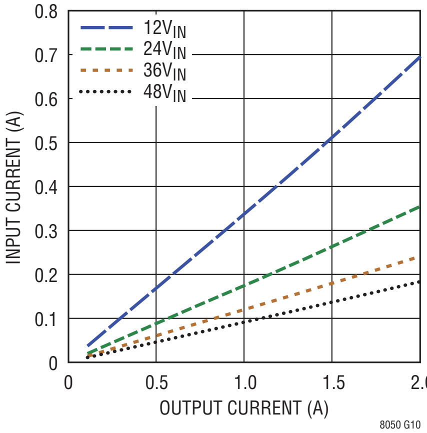
Input Current vs Output Current 2.5V$_{OUT}$



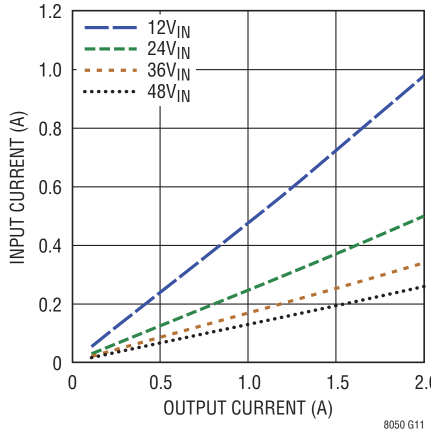
TYPICAL PERFORMANCE CHARACTERISTICS

Operating conditions are per Table 1 and T_A = 25°C, unless otherwise noted.

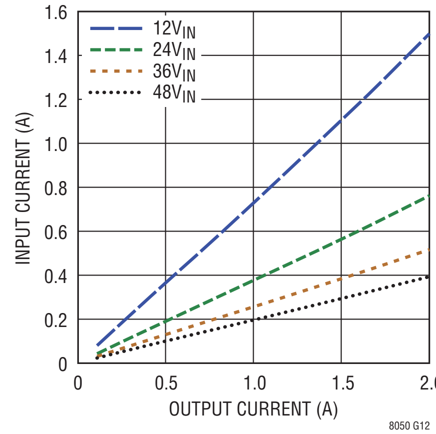
Input Current vs Output Current 3.3V$_{OUT}$



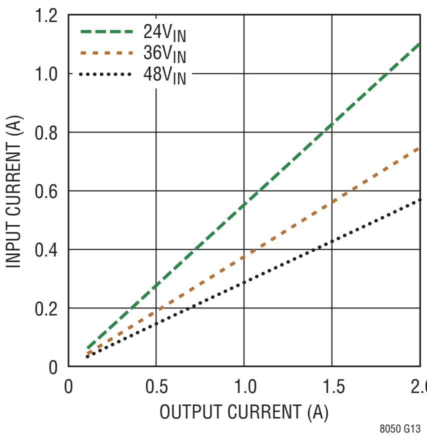
Input Current vs Output Current 5V$_{OUT}$



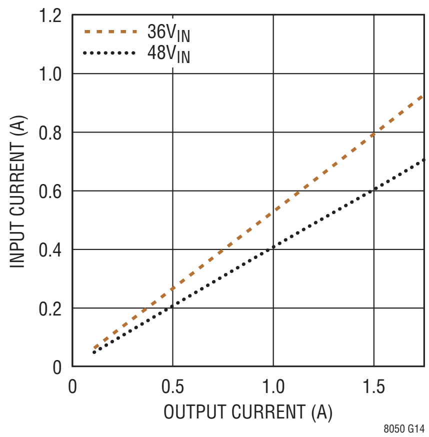
Input Current vs Output Current 8V$_{OUT}$



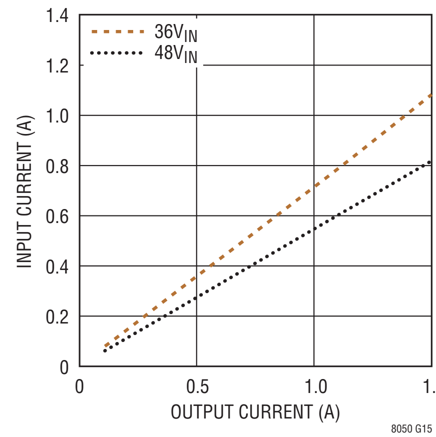
Input Current vs Output Current 12V$_{OUT}$



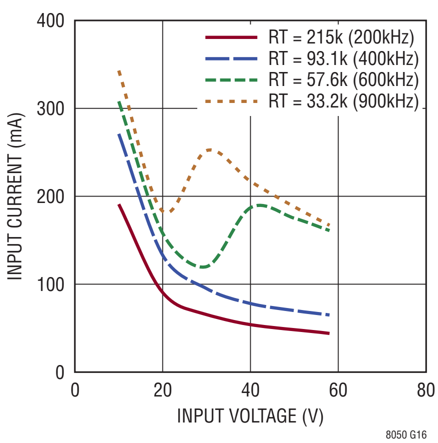
Input Current vs Output Current 18V$_{OUT}$



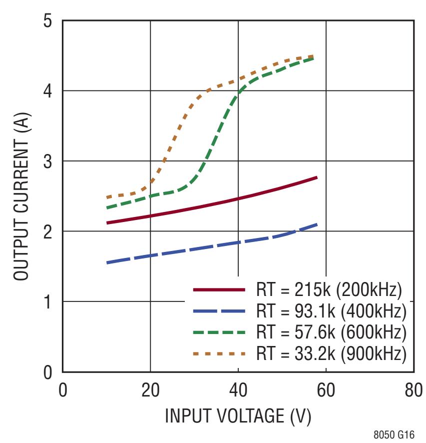
Input Current vs Output Current 24V$_{OUT}$



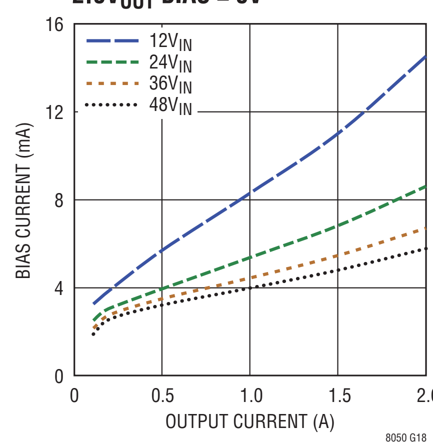
Input Current vs V$_{IN}$ Output Shorted



Output Current vs V$_{IN}$ Output Shorted



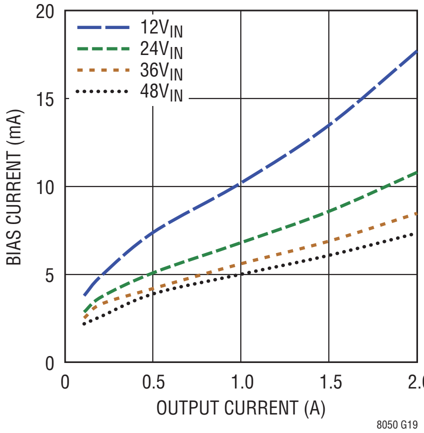
BIAS Current vs Output Current 2.5V$_{OUT}$ BIAS = 5V



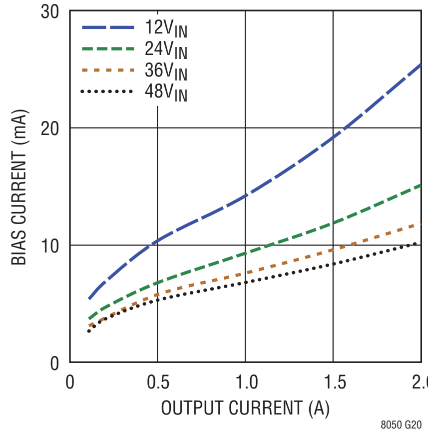
TYPICAL PERFORMANCE CHARACTERISTICS

Operating conditions are per Table 1 and T_A = 25°C, unless otherwise noted.

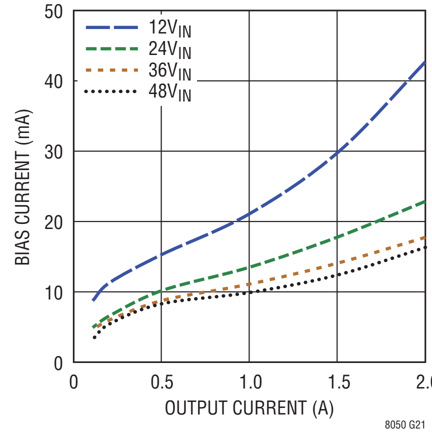
BIAS Current vs Output Current $3.3V_{OUT}$ BIAS = 5V



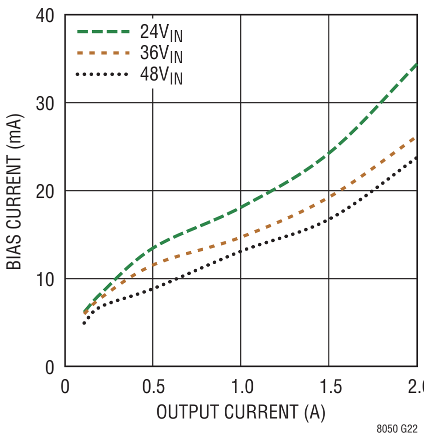
BIAS Current vs Output Current $5V_{OUT}$ BIAS = 5V



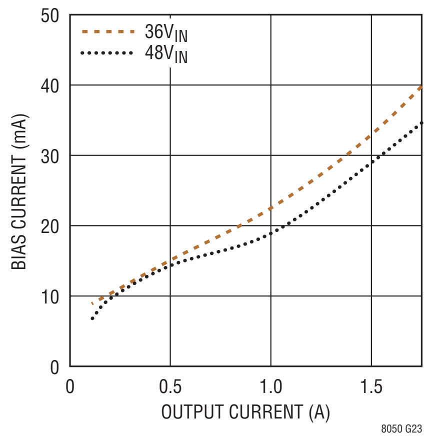
BIAS Current vs Output Current $8V_{OUT}$ BIAS = 5V



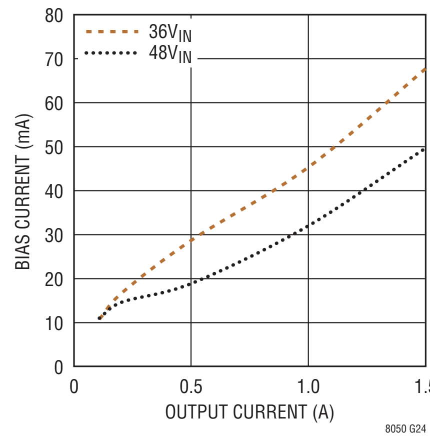
BIAS Current vs Output Current $12V_{OUT}$ BIAS = 5V



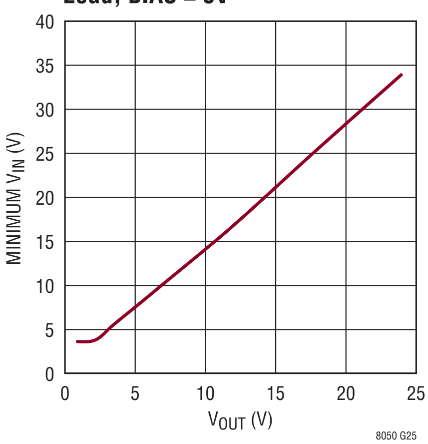
BIAS Current vs Output Current $18V_{OUT}$ BIAS = 5V



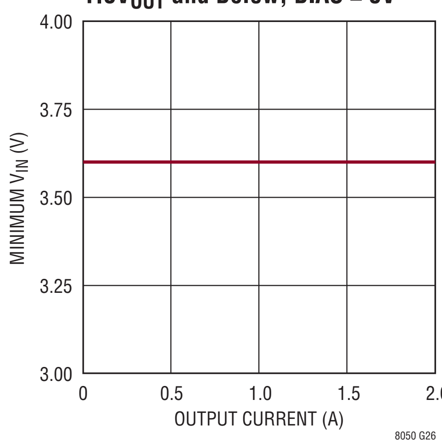
BIAS Current vs Output Current $24V_{OUT}$ BIAS = 5V



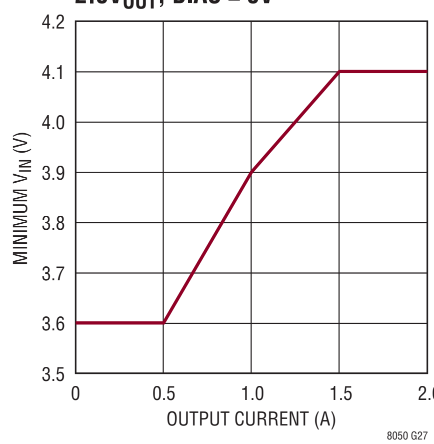
Minimum V_{IN} vs V_{OUT} Maximum Load, BIAS = 5V



Minimum V_{IN} vs Output Current $1.8V_{OUT}$ and Below, BIAS = 5V

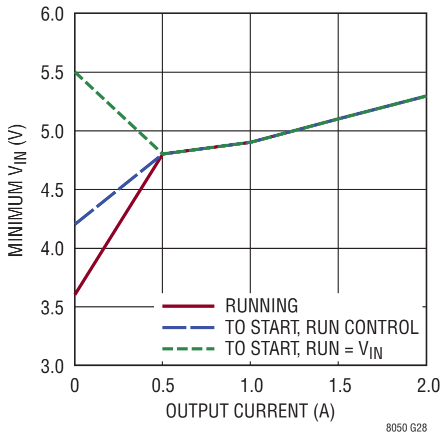


Minimum V_{IN} vs Output Current $2.5V_{OUT}$, BIAS = 5V

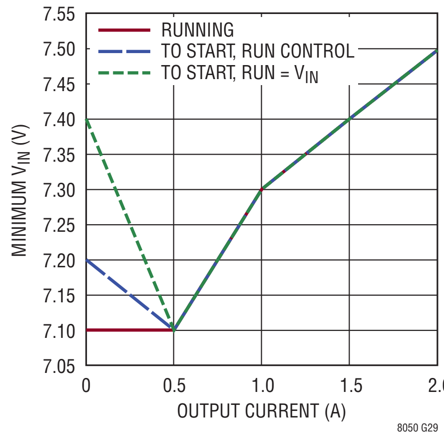


TYPICAL PERFORMANCE CHARACTERISTICS Operating conditions are per Table 1 and T_A = 25°C, unless otherwise noted.

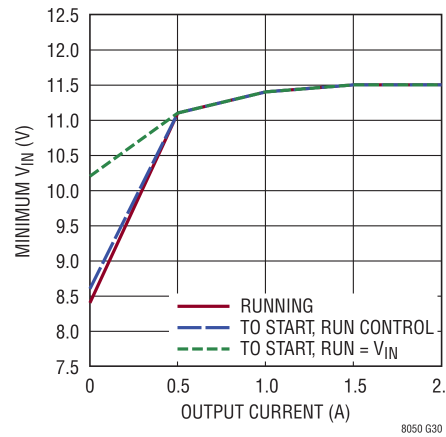
Minimum V_{IN} vs Output Current 3.3V_{OUT}, BIAS = V_{OUT}



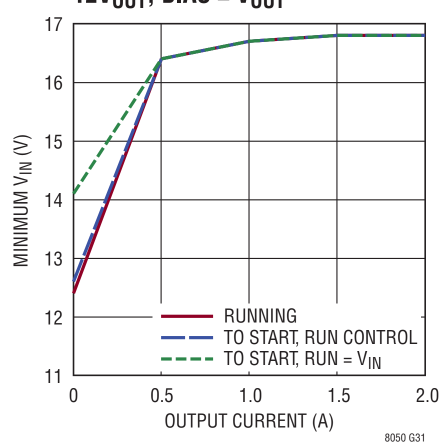
Minimum V_{IN} vs Output Current 5V_{OUT}, BIAS = V_{OUT}



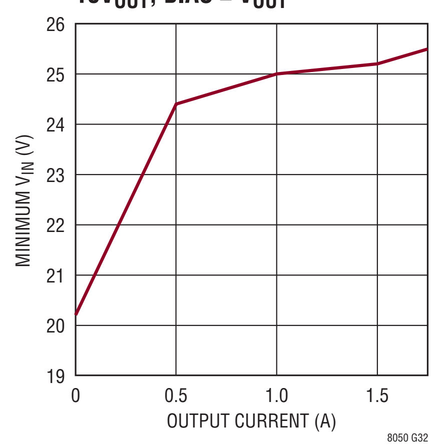
Minimum V_{IN} vs Output Current 8V_{OUT}, BIAS = V_{OUT}



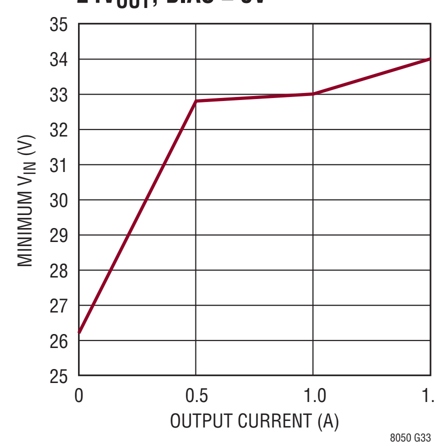
Minimum V_{IN} vs Output Current 12V_{OUT}, BIAS = V_{OUT}



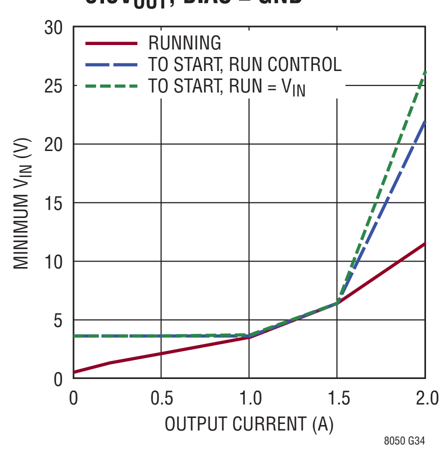
Minimum V_{IN} vs Output Current 18V_{OUT}, BIAS = V_{OUT}



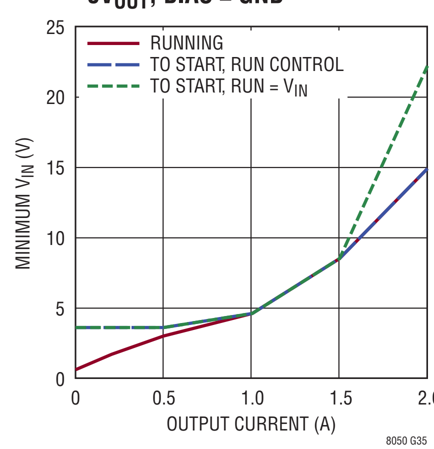
Minimum V_{IN} vs Output Current 24V_{OUT}, BIAS = 5V



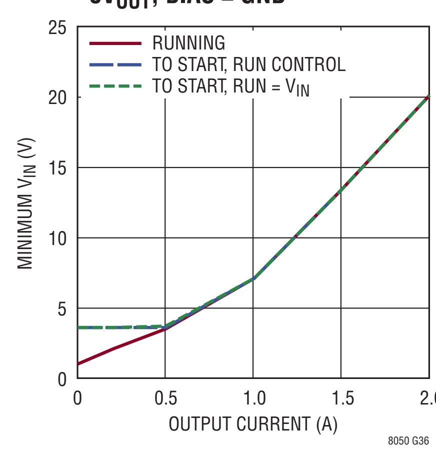
Minimum V_{IN} vs Output Current –3.3V_{OUT}, BIAS = GND



Minimum V_{IN} vs Output Current –5V_{OUT}, BIAS = GND



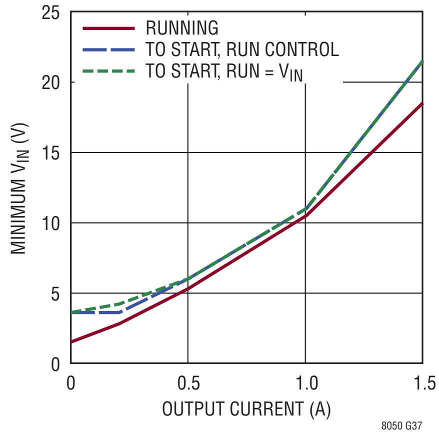
Minimum V_{IN} vs Output Current –8V_{OUT}, BIAS = GND



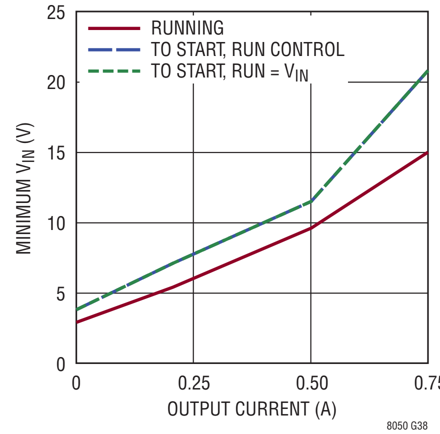
TYPICAL PERFORMANCE CHARACTERISTICS

Operating conditions are per Table 1 and T_A = 25°C, unless otherwise noted.

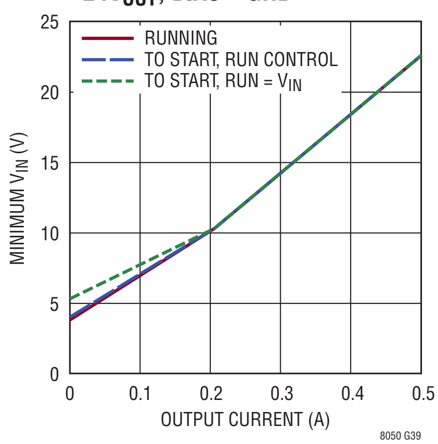
Minimum V_{IN} vs Output Current $-12V_{OUT}$, BIAS = GND



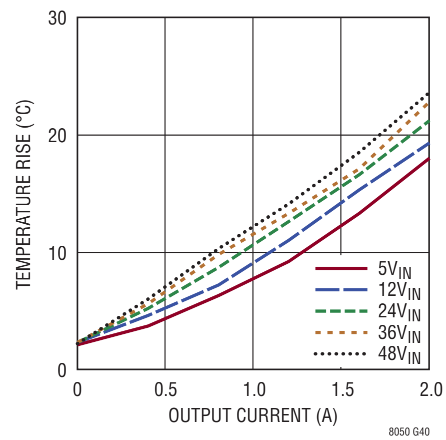
Minimum V_{IN} vs Output Current $-18V_{OUT}$, BIAS = GND



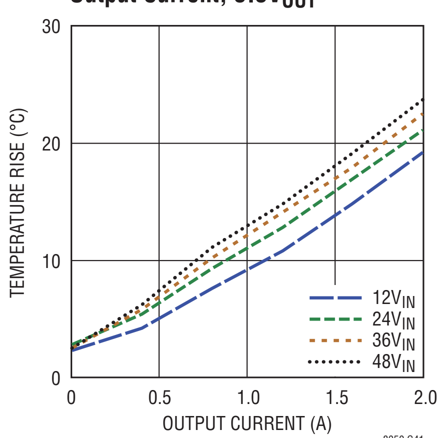
Minimum V_{IN} vs Output Current $-24V_{OUT}$, BIAS = GND



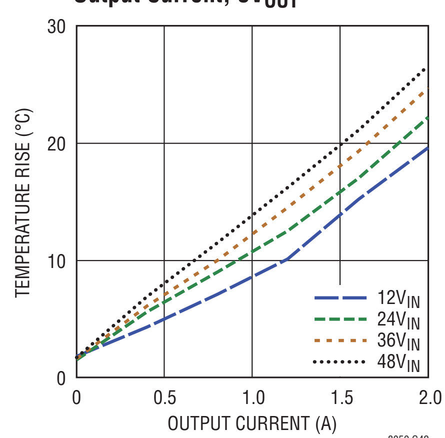
Internal Temperature Rise vs Output Current, $2.5V_{OUT}$



Internal Temperature Rise vs Output Current, $3.3V_{OUT}$



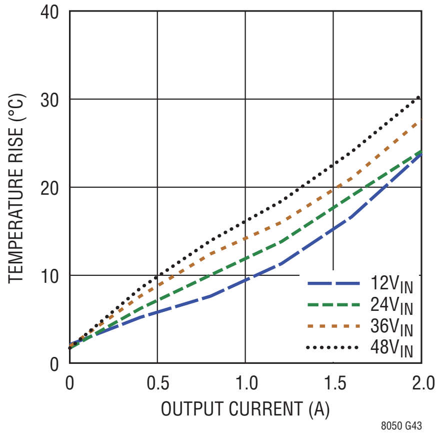
Internal Temperature Rise vs Output Current, $5V_{OUT}$



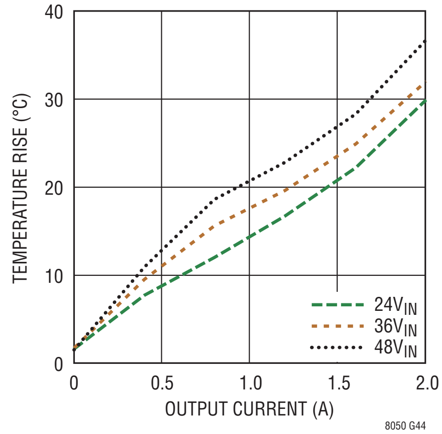
TYPICAL PERFORMANCE CHARACTERISTICS

Operating conditions are per Table 1 and T_A = 25°C, unless otherwise noted.

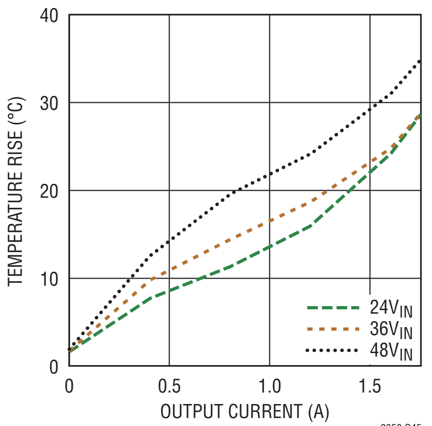
Internal Temperature Rise vs Output Current, $8V_{OUT}$



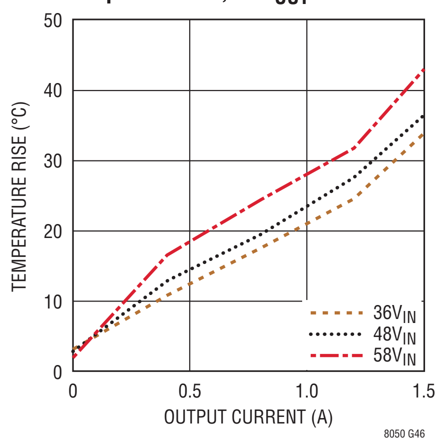
Internal Temperature Rise vs Output Current, $12V_{OUT}$



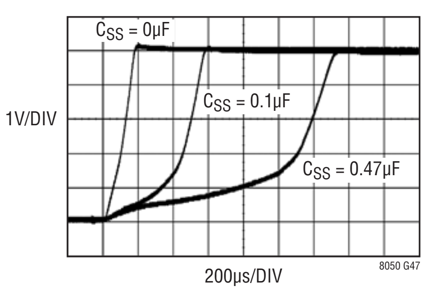
Internal Temperature Rise vs Output Current, $18V_{OUT}$



Internal Temperature Rise vs Output Current, $24V_{OUT}$

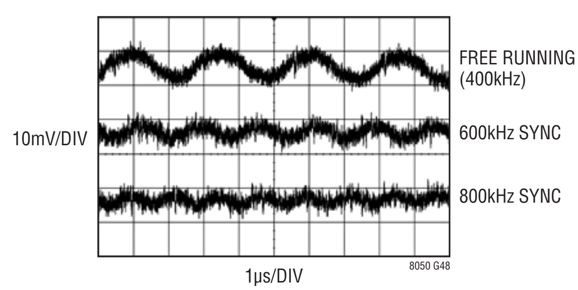


Soft-Start Waveform for Various C_{SS} Values 1A Resistive Load, DC1723A Demo Board



R_{SS} = 100k

Output Ripple at 2A Load, Standard DC1723A Demo Board



REFER TO DC1723A DEMO MANUAL FOR PROPER RIPPLE MEASUREMENT TECHNIQUE

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT} (Bank 1): Power Output Pins. Apply the output filter capacitor and the output load between these pins and GND pins.

GND (Bank 2): Tie these GND pins to a local ground plane below the LTM8050 and the circuit components. In most applications, the bulk of the heat flow out of the LTM8050 is through these pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Return the feedback divider (R_{FB}) to this net.

V_{IN} (Bank 3): The V_{IN} pin supplies current to the LTM8050's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor; see Table 1 for recommended values.

AUX (Pin G5): Low Current Voltage Source for BIAS. In many designs, the BIAS pin is simply connected to V_{OUT}. The AUX pin is internally connected to V_{OUT} and is placed adjacent to the BIAS pin to ease printed circuit board routing. Although this pin is internally connected to V_{OUT}, it is not intended to deliver a high current, so do **not** draw current from this pin to the load. If this pin is not tied to BIAS, leave it floating.

BIAS (Pin H5): The BIAS pin connects to the internal power bus. Connect to a power source greater than 2.8V and less than 25V. If the output is greater than 2.8V, connect this pin there. If the output voltage is less, connect this to a voltage source between 2.8V and 25V. Also, make sure that BIAS + V_{IN} is less than 72V.

RUN/SS (Pin L5): Pull the RUN/SS pin below 0.2V to shut down the LTM8050. Tie to 2.5V or more for normal operation. If the shutdown feature is not used, tie this pin to the V_{IN} pin. RUN/SS also provides a soft-start function; see the Applications Information section.

SYNC (Pin L6): This is the external clock synchronization input. Ground this pin for low ripple Burst Mode operation at low output loads. Tie to a stable voltage source greater than 0.7V to disable Burst Mode operation. Do not leave this pin floating. Tie to a clock source for synchronization. Clock edges should have rise and fall times faster than 1µs. See the Synchronization section in Applications Information.

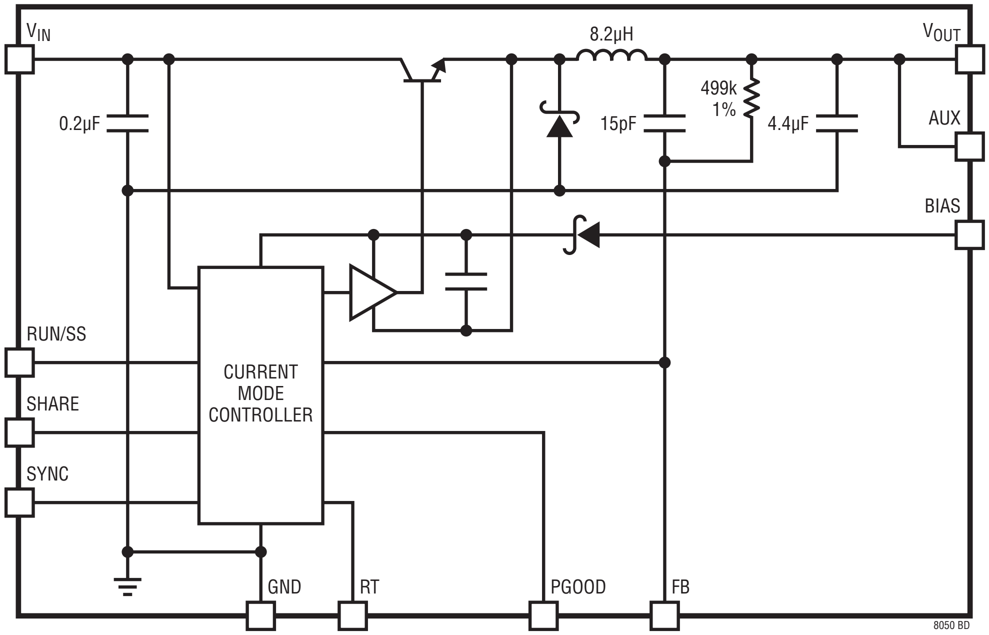
RT (Pin G7): The RT pin is used to program the switching frequency of the LTM8050 by connecting a resistor from this pin to ground. Table 2 gives the resistor values that correspond to the resultant switching frequency. Minimize the capacitance at this pin.

SHARE (Pin H7): Tie this to the SHARE pin of another LTM8050 when paralleling the outputs. Otherwise, do not connect.

PGOOD (Pin J7): The PGOOD pin is the open-collector output of an internal comparator. PGOOD remains low until the FB pin is within 10% of the final regulation voltage. PGOOD output is valid when V_{IN} is above 3.6V and RUN/SS is high. If this function is not used, leave this pin floating.

FB (Pin K7): The LTM8050 regulates its FB pin to 0.79V. Connect the adjust resistor from this pin to ground. The value of R_{FB} is given by the equation $R_{FB} = 394.21/(V_{OUT} – 0.79)$, where R_{FB} is in kΩ.

BLOCK DIAGRAM



OPERATION

The LTM8050 is a standalone nonisolated step-down switching DC/DC power supply that can deliver up to 2A of output current. This module provides a precisely regulated output voltage programmable via one external resistor from 0.8V to 24V. The input voltage range is 3.6V to 58V. Given that the LTM8050 is a step-down converter, make sure that the input voltage is high enough to support the desired output voltage and load current.

As shown in the Block Diagram, the LTM8050 contains a current mode controller, power switching element, power inductor, power Schottky diode and a modest amount of input and output capacitance. The LTM8050 is a fixed frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to GND.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 2.8V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency. The RUN/SS pin is used to place the LTM8050 in shutdown, disconnecting the output and reducing the input current to less than 1µA.

To further optimize efficiency, the LTM8050 automatically switches to Burst Mode® operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 50µA in a typical application.

The oscillator reduces the LTM8050's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LTM8050 contains a power good comparator which trips when the FB pin is at roughly 90% of its regulated value. The PGOOD output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PGOOD pin high. Power good is valid when the LTM8050 is enabled and V_{IN} is above 3.6V.

The LTM8050 is equipped with a thermal shutdown that will inhibit power switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

APPLICATIONS INFORMATION

For most applications, the design process is straight forward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{FB} and R_T values.
3. Connect BIAS as indicated.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current is limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM8050 should be allowed to switch is given in Table 1 in the f_{MAX} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the $f_{OPTIMAL}$ column. There are additional conditions that must be satisfied if the synchronization function is used. Please refer to the Synchronization section for details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. In Burst Mode operation, the LTM8050's switching frequency depends on the load current, and can excite a ceramic capacitor at audio frequencies, generating audible noise. Since the LTM8050 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8050. A ceramic input capacitor combined with trace or cable inductance forms a high Q (under damped) tank circuit. If the LTM8050 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Frequency Selection

The LTM8050 uses a constant frequency PWM architecture that can be programmed to switch from 100kHz to 2.4MHz by using a resistor tied from the RT pin to ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

APPLICATIONS INFORMATION

Table 1: Recommended Component Values and Configuration (T_A = 25°C)

V_{IN} RANGE	V_{OUT}	V_{BIAS}	C_{IN}	C_{OUT}	R_{FB}	$f_{OPTIMAL}$	$R_{T(OPTIMAL)}$	f_{MAX}	$R_{T(MIN)}$
3.6V to 58V	0.8V	2.8V to 25V	3× 4.7µF, 2220, 100V	3× 220µF, 1206, 4V	Open	110kHz	392k	125kHz	340k
3.6V to 58V	1V	2.8V to 25V	3× 4.7µF, 2220, 100V	3× 220µF, 1206, 4V	1.87M	110kHz	392k	125kHz	340k
3.6V to 58V	1.2V	2.8V to 25V	2× 4.7µF, 2220, 100V	3× 220µF, 1206, 4V	953k	125kHz	340k	150kHz	280k
3.6V to 58V	1.5V	2.8V to 25V	2× 4.7µF, 2220, 100V	2× 220µF, 1206, 4V	549k	150kHz	280k	180kHz	232k
3.6V to 58V	1.8V	2.8V to 25V	2× 4.7µF, 2220, 100V	2× 220µF, 1206, 4V	383k	180kHz	232k	215kHz	191k
4.1V to 58V	2.5V	2.8V to 25V	4.7µF, 2220, 100V	220µF, 1206, 4V	226k	230kHz	174k	270kHz	150k
5.3V to 58V	3.3V	AUX	4.7µF, 2220, 100V	220µF, 1206, 4V	154k	280kHz	140k	330kHz	118k
7.5V to 58V	5V	AUX	4.7µF, 2220, 100V	100µF, 1210, 6.3V	93.1k	400kHz	93.1k	460kHz	80.6k
10.5V to 58V	8V	AUX	4.7µF, 2220, 100V	47µF, 1210, 10V	54.9k	550kHz	64.9k	690kHz	49.9k
17V to 58V	12V	AUX	4.7µF, 2220, 100V	22µF, 1210, 16V	34.8k	600kHz	57.6k	750kHz	44.2k
24V to 58V	18V	2.8V to 25V	4.7µF, 2220, 100V	22µF, 1812, 25V	22.6k	760kHz	42.2k	850kHz	37.4k
34V to 58V	24V	2.8V to 25V	4.7µF, 2220, 100V	22µF, 1812, 25V	16.5k	900kHz	33.2k	960kHz	30.1k
9V to 24V	0.8V	V_{IN}	4.7µF, 1206, 25V	2× 220µF, 1206, 4V	Open	150kHz	280k	300kHz	130k
9V to 24V	1V	V_{IN}	4.7µF, 1206, 25V	2× 220µF, 1206, 4V	1.87M	180kHz	232k	345kHz	113k
9V to 24V	1.2V	V_{IN}	4.7µF, 1206, 25V	2× 220µF, 1206, 4V	953k	230kHz	174k	400kHz	93.1k
9V to 24V	1.5V	V_{IN}	4.7µF, 1206, 25V	220µF, 1206, 4V	549k	280kHz	140k	460kHz	80.6k
9V to 24V	1.8V	V_{IN}	4.7µF, 1206, 25V	220µF, 1206, 4V	383k	330kHz	118k	500kHz	73.2k
9V to 24V	2.5V	V_{IN}	4.7µF, 1206, 25V	100µF, 1210, 6.3V	226k	345kHz	113k	600kHz	57.6k
9V to 24V	3.3V	AUX	4.7µF, 1206, 25V	100µF, 1210, 6.3V	154k	425kHz	88.7k	650kHz	52.3k
9V to 24V	5V	AUX	4.7µF, 1206, 25V	47µF, 1210, 10V	93.1k	500kHz	73.2k	700kHz	48.7k
10.5V to 24V	8V	AUX	4.7µF, 1206, 25V	47µF, 1210, 10V	54.9k	600kHz	57.6k	750kHz	44.2k
17V to 24V	12V	AUX	2.2µF, 1206, 50V	22µF, 1210, 16V	34.8k	760kHz	42.2k	850kHz	36.5k
18V to 36V	0.8V	2.8V to 25V	1µF, 1206, 50V	3× 220µF, 1206, 4V	Open	100kHz	432k	200kHz	205k
18V to 36V	1V	2.8V to 25V	1µF, 1206, 50V	3× 220µF, 1206, 4V	1.87M	120kHz	357k	250kHz	162k
18V to 36V	1.2V	2.8V to 25V	1µF, 1206, 50V	2× 220µF, 1206, 4V	953k	140kHz	301k	270kHz	150k
18V to 36V	1.5V	2.8V to 25V	1µF, 1206, 50V	2× 220µF, 1206, 4V	549k	180kHz	232k	300kHz	130k
18V to 36V	1.8V	2.8V to 25V	1µF, 1206, 50V	220µF, 1206, 4V	383k	220kHz	187k	350kHz	110k
18V to 36V	2.5V	2.8V to 25V	1µF, 1206, 50V	100µF, 1210, 6.3V	226k	300kHz	130k	425kHz	88.7k
18V to 36V	3.3V	AUX	1µF, 1206, 50V	100µF, 1210, 6.3V	154k	345kHz	113k	550kHz	64.9k
18V to 36V	5V	AUX	1µF, 1206, 50V	47µF, 1210, 10V	93.1k	425kHz	88.7k	800kHz	38.3k
18V to 36V	8V	AUX	2.2µF, 1206, 50V	22µF, 1210, 16V	54.9k	550kHz	64.9k	1.03MHz	25.5k
18V to 36V	12V	AUX	2.2µF, 1206, 50V	22µF, 1210, 16V	34.8k	760kHz	42.2k	1.03MHz	25.5k
24V to 36V	18V	2.8V to 25V	2.2µF, 1206, 50V	22µF, 1812, 25V	22.6k	800kHz	38.3k	1.03MHz	25.5k
18V to 58V	0.8V	2.8V to 25V	1µF, 1206, 100V	3× 220µF, 1206, 4V	Open	100kHz	432k	125kHz	340k
18V to 58V	1V	2.8V to 25V	1µF, 1206, 100V	3× 220µF, 1206, 4V	1.87M	100kHz	432k	125kHz	340k
18V to 58V	1.2V	2.8V to 25V	1µF, 1206, 100V	3× 220µF, 1206, 4V	953k	100kHz	432k	150kHz	280k
18V to 58V	1.5V	2.8V to 25V	1µF, 1206, 100V	2× 220µF, 1206, 4V	549k	110kHz	392k	180kHz	232k
18V to 58V	1.8V	2.8V to 25V	1µF, 1206, 100V	2× 220µF, 1206, 4V	383k	125kHz	340k	215kHz	191k
18V to 58V	2.5V	2.8V to 25V	1µF, 1206, 100V	220µF, 1206, 4V	226k	180kHz	232k	270kHz	150k
18V to 58V	3.3V	AUX	1µF, 1206, 100V	100µF, 1210, 6.3V	154k	280kHz	140k	330kHz	118k
18V to 58V	5V	AUX	1µF, 1206, 100V	100µF, 1210, 6.3V	93.1k	400kHz	93.1k	460kHz	80.6k
18V to 58V	8V	AUX	2.2µF, 1206, 100V	47µF, 1210, 10V	54.9k	550kHz	64.9k	690kHz	49.9k
18V to 58V	12V	AUX	2.2µF, 1206, 100V	22µF, 1210, 16V	34.8k	600kHz	57.6k	960kHz	30.1k
2.5V to 54.7V	–3.3V	AUX	2× 4.7µF, 2220, 100V	100µF, 1210, 6.3V	154k	300kHz	130k	330kHz	118k
3.3V to 53V	–5V	AUX	4.7µF, 2220, 100V	100µF, 1210, 6.3V	93.1k	400kHz	93.1k	460kHz	80.6k
3.3V to 50V	–8V	AUX	4.7µF, 2220, 100V	47µF, 1210, 10V	54.9k	550kHz	64.9k	690kHz	49.9k
4.5V to 46V	–12V	AUX	4.7µF, 2220, 100V	47µF, 1210, 16V	34.8k	600kHz	57.6k	750kHz	44.2k
6V to 40V	–18V	2.8V to 25V	4.7µF, 2220, 100V	22µF, 1812, 25V	22.6k	760kHz	42.2k	850kHz	37.4k
10V to 34V	–24V	2.8V to 25V	4.7µF, 2220, 100V	22µF, 1812, 25V	16.5k	900kHz	33.2k	960kHz	30.1k

Note: Do not allow V_{IN} + BIAS to exceed 72V.

APPLICATIONS INFORMATION

Table 2. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.1	432
0.2	215
0.3	137
0.4	93.1
0.5	73.2
0.6	57.6
0.7	51.1
0.8	38.3
0.9	33.2
1	32.4
1.2	24.9
1.4	20
1.6	16.2
1.8	14
2	11
2.2	8.06
2.4	7.15

Operating Frequency Trade-offs

It is recommended that the user apply the optimal R_T value given in Table 1 for the input and output operating condition. System level or other considerations, however, may necessitate another operating frequency. While the LTM8050 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat or even damage the LTM8050 if the output is overloaded or short circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

BIAS Pin Considerations

The BIAS pin is used to provide drive power for the internal power switching stage and operate other internal circuitry. For proper operation, it must be powered by at least 2.8V. If the output voltage is programmed to 2.8V or higher, BIAS may be simply tied to AUX. If V_{OUT} is less than 2.8V, BIAS can be tied to V_{IN} or some other voltage source. If the BIAS pin voltage is too high, the efficiency of the LTM8050 may suffer. The optimum BIAS voltage is dependent upon many factors, such as load current, input voltage, output voltage and switching frequency, but 4V to 5V works well in many applications. In all cases, ensure that the maximum voltage at the BIAS pin is less than 25V and that the sum of V_{IN} and BIAS is less than 72V. If BIAS power is applied from a remote or noisy voltage source, it may be necessary to apply a decoupling capacitor locally to the pin.

Load Sharing

Two or more LTM8050's may be paralleled to produce higher currents. To do this, tie the V_{IN}, FB, V_{OUT} and SHARE pins of all the paralleled LTM8050's together. To ensure that paralleled modules start up together, the RUN/SS pins may be tied together, as well. If the RUN/SS pins are not tied together, make sure that the same valued soft-start capacitors are used for each module. Current sharing can be improved by synchronizing the LTM8050s. An example of two LTM8050s configured for load sharing is given in the Typical Applications section. When n number of units are connected for parallel operation and a single feedback resistor is used for all of them, the equation for the feedback resistor is:

$$R_{FB} = \frac{394.21}{N\left(V_{OUT} - 0.79\right)} k\Omega$$

Burst Mode Operation

To enhance efficiency at light loads, the LTM8050 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LTM8050 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are each reduced to microamps during the sleep time. As the load current decreases towards a no load condition, the percentage of time that the LTM8050 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher efficiency.

Burst Mode operation is enabled by tying SYNC to GND. To disable Burst Mode operation, tie SYNC to a stable voltage above 0.7V. *Do not leave the SYNC pin floating.*

APPLICATIONS INFORMATION

Minimum Input Voltage

The LTM8050 is a step-down converter, so a minimum amount of headroom is required to keep the output in regulation. In addition, the input voltage required to turn on is higher than that required to run, and depends upon whether the RUN/SS is used. As shown in the Typical Performance Characteristics section, the minimum input voltage to run a 3.3V output at light load is only about 3.6V, but, if RUN/SS is pulled up to V_{IN}, it takes $5.5V_{IN}$ to start. If the LTM8050 is enabled with the RUN/SS pin after V_{IN} is applied, the minimum voltage to start at light loads is lower, about 4.3V. Similar curves detailing this behavior of the LTM8050 for other outputs are also included in the Typical Performance Characteristics section.

Soft-Start

The RUN/SS pin can be used to soft-start the LTM8050, reducing the maximum input current during start-up. The RUN/SS pin is driven through an external RC network to create a voltage ramp at this pin. (See Figure 1). By choosing an appropriate RC time constant, the peak start-up current can be reduced to the current that is required to regulate the output, with no overshoot. Choose the value of the resistor so that it can supply at least 20µA when the RUN/SS pin reaches 2.5V. Output voltage soft-start waveforms for various values of R_{SS} and C_{SS} are given in the Typical Performance Characteristics section.

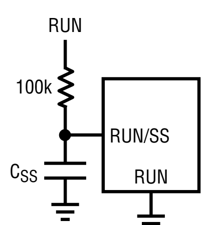


Figure 1. Apply an RC Network to RUN/SS to Control the Soft-Start Behavior of the LTM8050 at Power-Up

Frequency Foldback

The LTM8050 is equipped with frequency foldback which acts to reduce the thermal and energy stress on the internal power elements during a short circuit or output overload condition. If the LTM8050 detects that the output has fallen out of regulation, the switching frequency is reduced as a function of how far the output is below the target voltage. This in turn limits the amount of energy that can be delivered to the load under fault. During the start-up time, frequency foldback is also active to limit the energy delivered to the potentially large output capacitance of the load.

Synchronization

The internal oscillator of the LTM8050 can be synchronized by applying an external 250kHz to 2MHz clock to the SYNC pin. Do not leave this pin floating. When synchronizing the LTM8050, select an R_T resistor value that corresponds to an operating frequency 20% lower than the intended synchronization frequency (see the Frequency Selection section).

In addition to synchronization, the SYNC pin controls Burst Mode behavior. If the SYNC pin is driven by an external clock, or pulled up above 0.7V, the LTM8050 will not enter Burst Mode operation, but will instead skip pulses to maintain regulation instead.

Shorted Input Protection

Care needs to be taken in systems where the output will be held high when the input to the LTM8050 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LTM8050's output. If the V_{IN} pin is allowed to float and the SHDN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM8050's internal circuitry will pull its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN/SS pin, the input current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LTM8050 can pull large currents from the output through the V_{IN} pin. Figure 2 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8050. The LTM8050 is nevertheless a switching power supply, and care must be taken to

APPLICATIONS INFORMATION

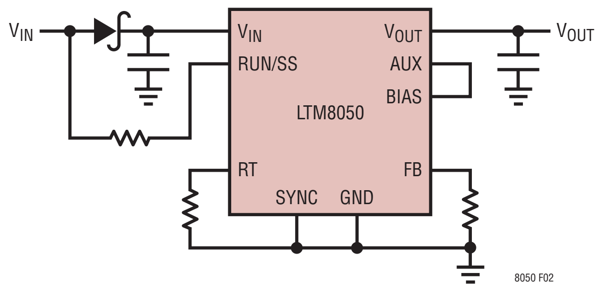


Figure 2. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LTM8050 Runs Only When the Input is Present

minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

1. Place the R_{FB} and R_T resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connection of the LTM8050.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM8050.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent to or underneath the LTM8050.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8050.
6. For good heat sinking, use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 3. The LTM8050 can benefit from the heat-sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

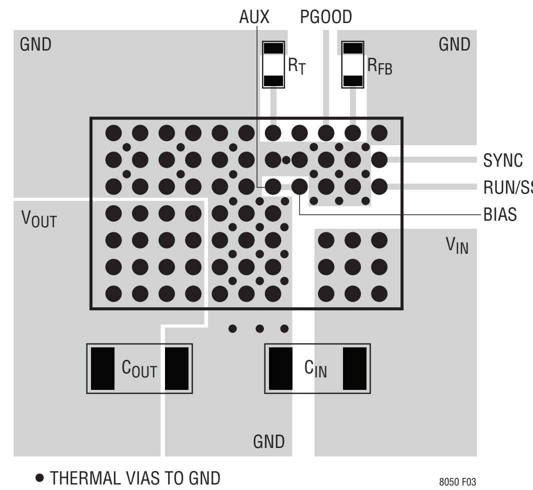


Figure 3. Layout Showing Suggested External Components, GND Plane and Thermal Vias

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM8050. However, these capacitors can cause problems if the LTM8050 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8050 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8050's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8050 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is to add an electrolytic bulk capacitor to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

APPLICATIONS INFORMATION

Negative Output Considerations

The LTM8050 may be configured to generate a negative output voltage. Examples of this are shown in the Typical Applications section. For very fast rising input voltages, care must be taken to ensure that start-up does not create excessive surge currents that may create unwanted voltages or even damage the LTM8050.

Consider the circuit in Figure 4. If a step input is applied between V_{IN} and system GND, the C_{IN} and C_{OUT} capacitors form an AC divider network that tends to create a positive voltage on system V_{OUT}. In order to protect the load from seeing an excessive inverted voltage, an anti-parallel Schottky diode may be used to clamp the voltage. Furthermore, current flowing out of the BIAS pin can have adverse affects. To prevent this from happening, apply a series resistor (about 200Ω) and Schottky diode between BIAS and its voltage source.

Thermal Considerations

The LTM8050 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by a LTM8050 mounted to a $40cm^2$ 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in Page 2 of the data sheet are based on modeling the µModule package mounted on a test board specified per JESD51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The thermal coefficients provided in this page are based on JESD 51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, Page 2 of the data sheet typically gives four thermal coefficients:

θ_{JA} – Thermal resistance from junction to ambient

$\theta_{JCbottom}$ – Thermal resistance from junction to the bottom of the product case

θ_{JCtop} – Thermal resistance from junction to top of the product case

θ_{JB} – Thermal resistance from junction to the printed circuit board

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased below:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as

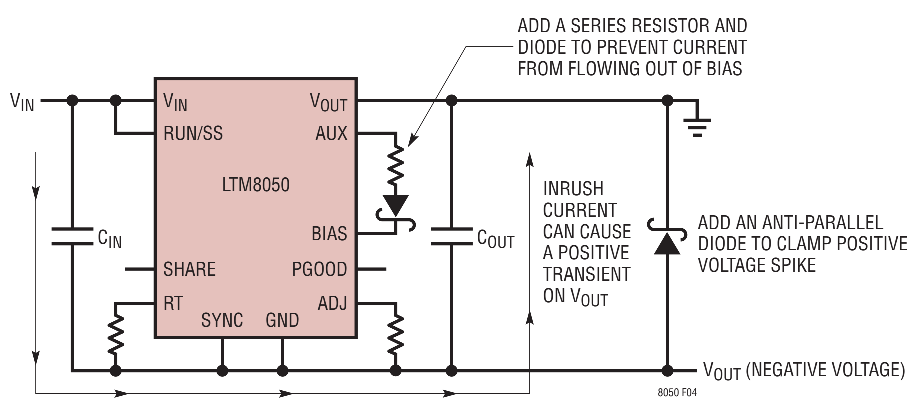


Figure 4. In Negative Output Voltage Applications, Prevent Adverse Effects from Fast Rising V_{IN} by Adding Clamp and Rectifying Diodes

APPLICATIONS INFORMATION

still air although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the thermal resistance between the junction and bottom of the package with all of the component power dissipation flowing through the bottom of the package. In the typical µModule converter, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule converter are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

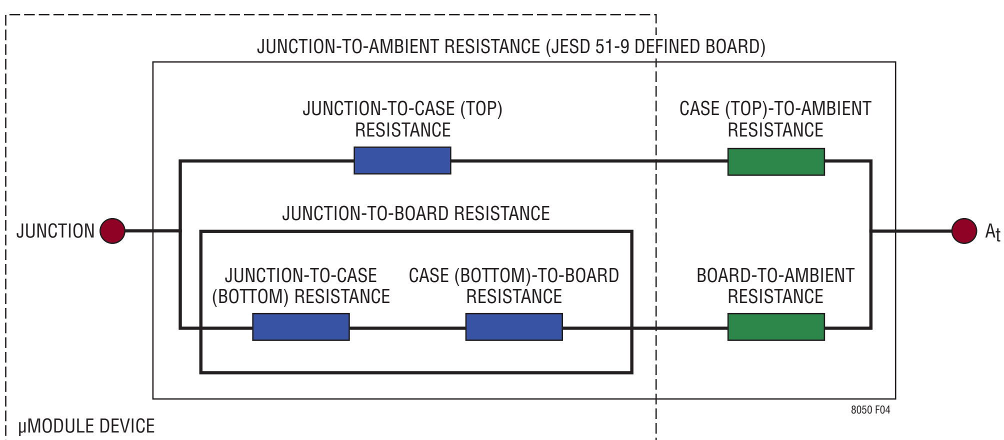
θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule converter and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule converter. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances follows:

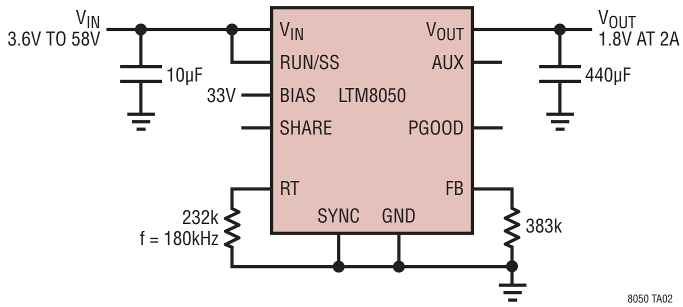
The blue resistances are contained within the µModule converter, and the green are outside.

The die temperature of the LTM8050 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8050. The bulk of the heat flow out of the LTM8050 is through the bottom of the µModule converter and the LGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

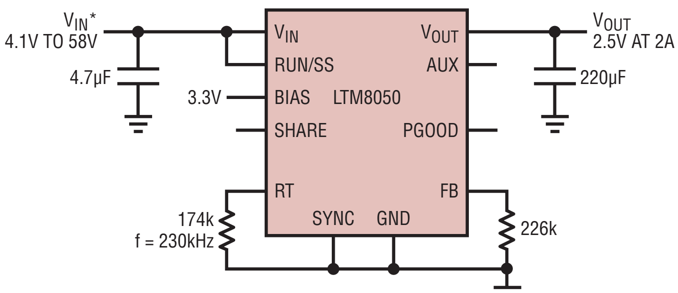


TYPICAL APPLICATIONS

1.8V Step-Down Converter

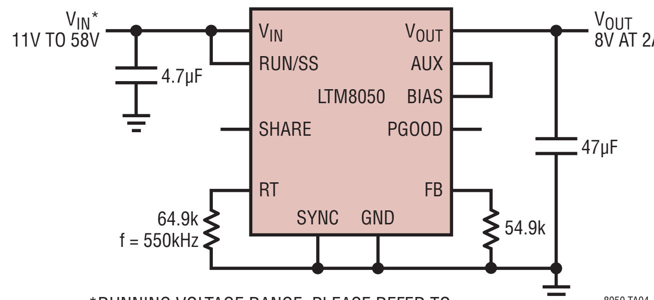


2.5V Step-Down Converter



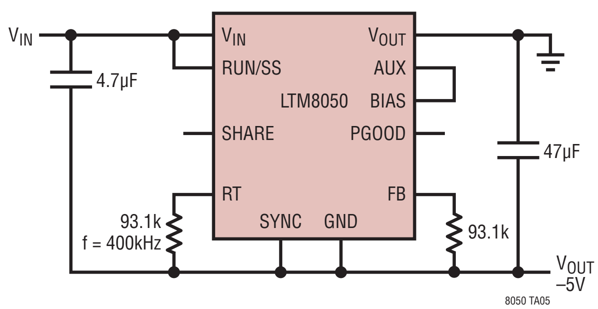
*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS

8V Step-Down Converter

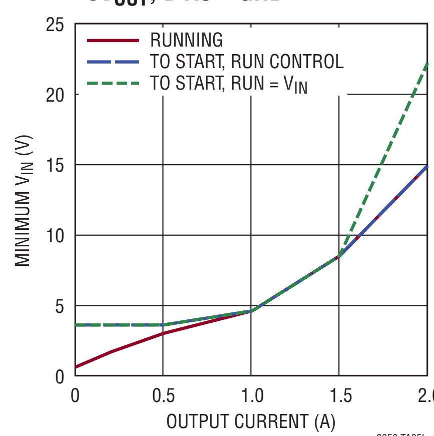


*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS

–5V Negative Output Converter



Minimum V_{IN} vs Output Current $-5V_{OUT}$, BIAS = GND



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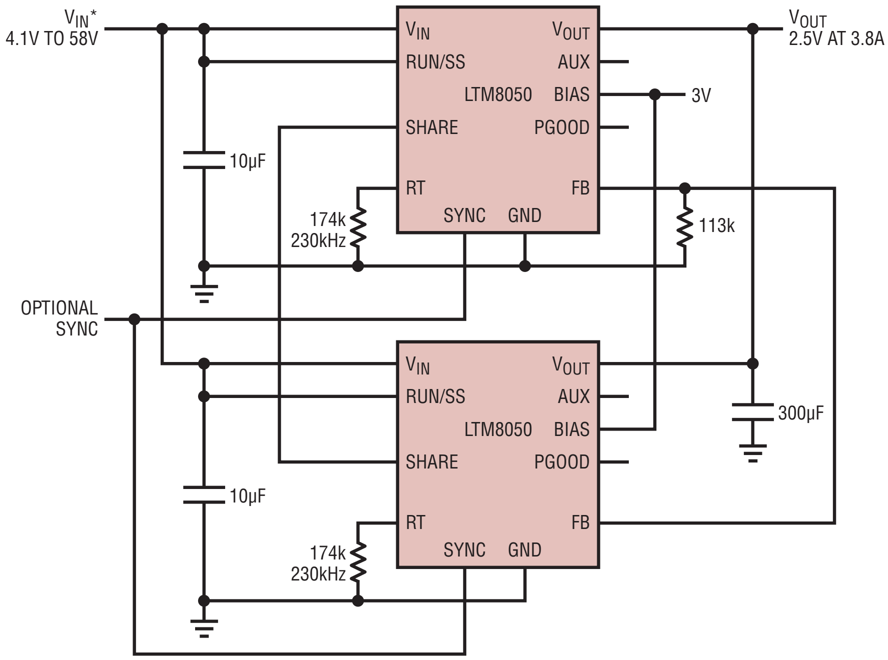
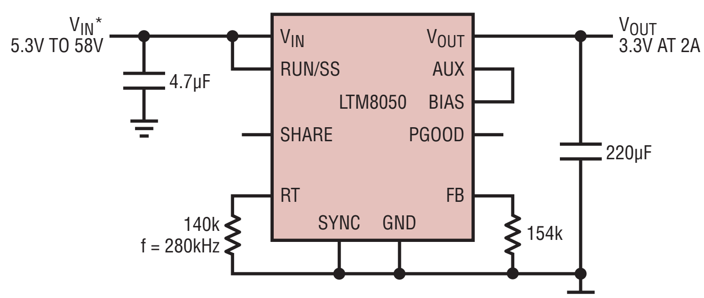
TYPICAL APPLICATIONS

Two LTM8050s in Parallel, 2.5V at 3.8A



*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS
NOTE: SYNCHRONIZE THE TWO MODULES TO AVOID BEAT FREQUENCIES, IF NECESSARY. OTHERWISE, TIE EACH SYNC TO GND

3.3V Step-Down Converter



*RUNNING VOLTAGE RANGE. PLEASE REFER TO APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS

PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Assignment Table
(Arranged by Pin Number)

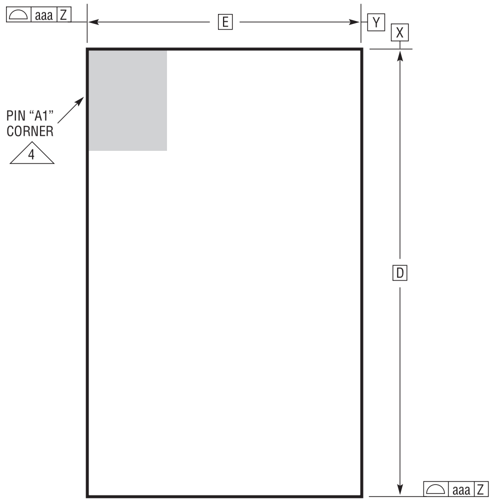
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	V_{OUT}	B1	V_{OUT}	C1	V_{OUT}	D1	V_{OUT}	E1	GND	F1	GND
A2	V_{OUT}	B2	V_{OUT}	C2	V_{OUT}	D2	V_{OUT}	E2	GND	F2	GND
A3	V_{OUT}	B3	V_{OUT}	C3	V_{OUT}	D3	V_{OUT}	E3	GND	F3	GND
A4	V_{OUT}	B4	V_{OUT}	C4	V_{OUT}	D4	V_{OUT}	E4	GND	F4	GND
A5	GND	B5	GND	C5	GND	D5	GND	E5	GND	F5	GND
A6	GND	B6	GND	C6	GND	D6	GND	E6	GND	F6	GND
A7	GND	B7	GND	C7	GND	D7	GND	E7	GND	F7	GND

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
G1	GND	H1	-	J1	V_{IN}	K1	V_{IN}	L1	V_{IN}
G2	GND	H2	-	J2	V_{IN}	K2	V_{IN}	L2	V_{IN}
G3	GND	H3	-	J3	V_{IN}	K3	V_{IN}	L3	V_{IN}
G4	GND	H4	-	J4	-	K4	-	L4	-
G5	AUX	H5	BIAS	J5	GND	K5	GND	L5	RUN/SS
G6	GND	H6	GND	J6	GND	K6	GND	L6	SYNC
G7	RT	H7	SHARE	J7	PGOOD	K7	FB	L7	GND

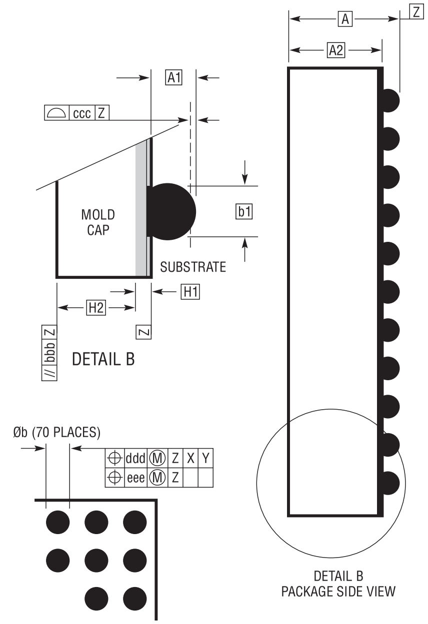
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

BGA Package
70-Lead (15mm × 9mm × 4.92mm)
(Reference LTC DWG# 05-08-1918 Rev A)



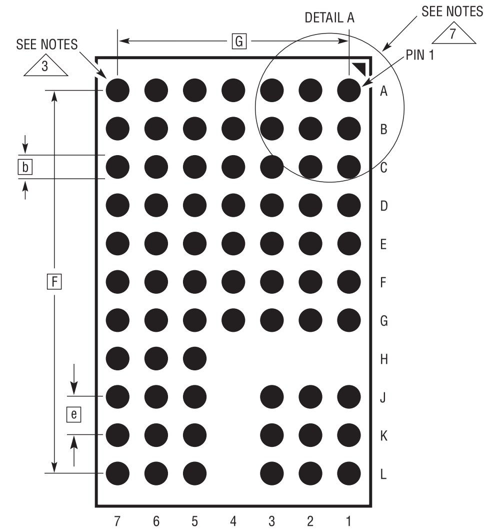
PACKAGE TOP VIEW



DETAIL B

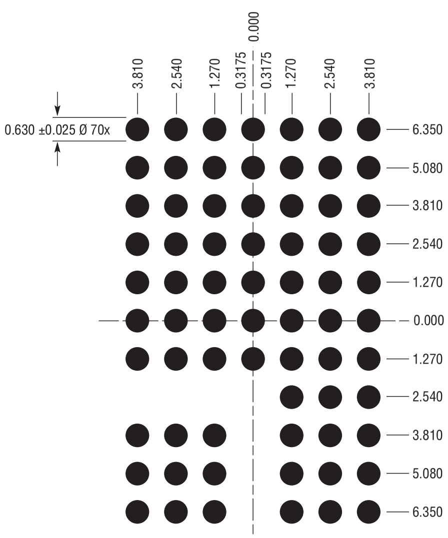
DETAIL A

DETAIL B
PACKAGE SIDE VIEW



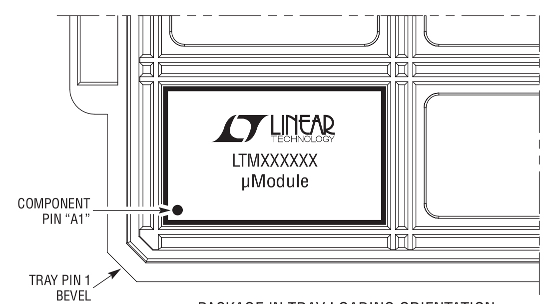
PACKAGE BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
7. ⚠ PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



SUGGESTED PCB LAYOUT
TOP VIEW

	DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		9.00		
e		1.27		
F		12.70		
G		7.62		
H1	0.27	0.32	0.37	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 70				



PACKAGE IN TRAY LOADING ORIENTATION

BGA 70 1212 REV A

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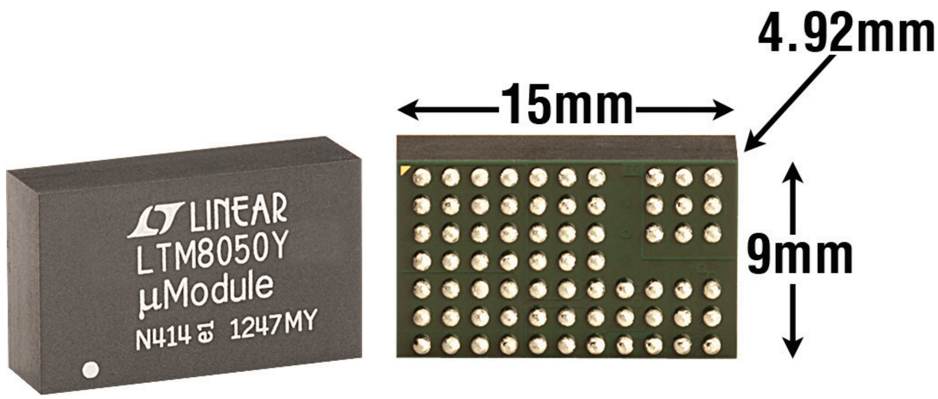
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/14	Add SnPb BGA package option	1, 2
B	05/14	Add TechClip Video icons	1
		Correct Typical Performance Characteristics labels	8

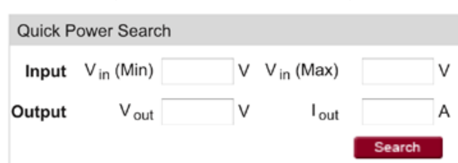
PACKAGE PHOTO



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4601/LTM4603	12A and 6A DC/DC µModule	Pin Compatible; Remote Sensing; PLL, Tracking and Margining, $4.5V \le V_{IN} \le 28V$
LTM4604A	4A, Low V_{IN} DC/DC µModule	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 9mm × 15mm × 2.3mm LGA Package
LTM4606	Low EMI 6A, 28V DC/DC µModule	$4.5V \le V_{IN} \le 28V$, $0.6V \le V_{OUT} \le 5V$, 15mm × 15mm × 2.8mm LGA Package
LTM8020	200mA, 36V DC/DC µModule	$4V \le V_{IN} \le 36V$, $1.25V \le V_{OUT} \le 5V$, 6.25mm × 6.25mm × 2.32mm LGA Package
LTM8022/LTM8023	1A and 2A, 36V DC/DC µModule	Pin Compatible $3.6V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$, 11.25mm × 9mm × 2.82mm LGA Package
LTM8027	60V, 4A DC/DC µModule	$4.5V \le V_{IN} \le 60V$; $2.5V \le V_{OUT} \le 24V$, 15mm × 15mm × 4.32mm LGA Package

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

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