16-Bit, 310 MSPS, 3.3 V/1.8 V Dual Analog-to-Digital Converter (ADC)

Data Sheet **AD9652**

FEATURES

- High dynamic range
  - SNR = 75.0 dBFS at 70 MHz (A_{IN} = −1 dBFS)
  - SFDR = 87 dBc at 70 MHz (A_{IN} = −1 dBFS)
  - Noise spectral density (NSD) = −156.7 dBFS/Hz input noise at −1 dBFS at 70 MHz
  - NSD = −157.6 dBFS/Hz for small signal at −7dBFS at 70 MHz
  - 90 dB channel isolation/crosstalk
  - On-chip dithering (improves small signal linearity)
- Excellent IF sampling performance
  - SNR = 73.7 dBFS at 170 MHz (A_{IN} = −1 dBFS)
  - SFDR = 85 dBc at 170 MHz (A_{IN} = −1 dBFS)
  - Full power bandwidth of 465 MHz
- On-chip 3.3 V buffer
  - Programmable input span of 2 V p-p to 2.5 V p-p (default)
- Differential clock input receiver with 1, 2, 4, and 8 integer inputs (clock divider input accepts up to 1.24 GHz)
- Internal ADC clock duty cycle stabilizer
- SYNC input allows multichip synchronization
- Total power consumption: 2.16 W
  - 3.3 V and 1.8 V supply voltages
- DDR LVDS (ANSI-644 levels) outputs
- Serial port control
- Energy saving power-down modes

APPLICATIONS

- Military radar and communications
- Multimode digital receivers (3G or 4G)
- Test and instrumentation
- Smart antenna systems

FUNCTIONAL BLOCK DIAGRAM

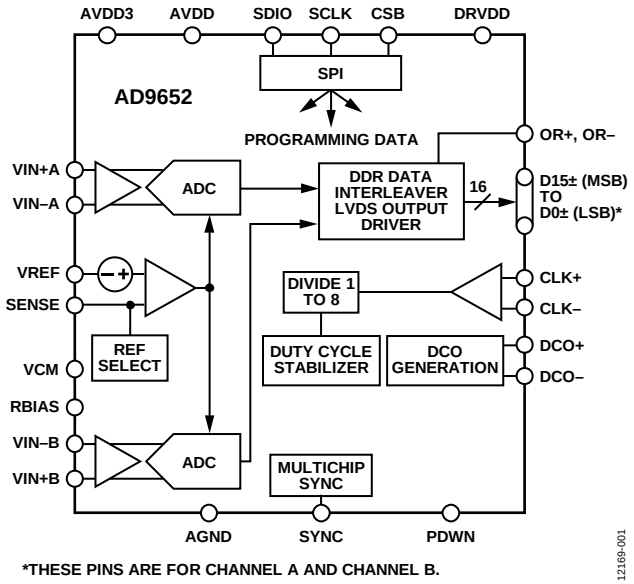

Figure 1.

GENERAL DESCRIPTION

The AD9652 is a dual, 16-bit analog-to-digital converter (ADC) with sampling speeds of up to 310 MSPS. It is designed to support demanding, high speed signal processing applications that require exceptional dynamic range over a wide input frequency range (up to 465 MHz). Its exceptional low noise floor of −157.6 dBFS and large signal spurious-free dynamic range (SFDR) performance (exceeding 85 dBFS, typical) allows low level signals to be resolved in the presence of large signals.

The dual ADC cores feature a multistage, pipelined architecture with integrated output error correction logic. A high performance on-chip buffer and internal voltage reference simplify the interface to external driving circuitry while preserving the exceptional performance of the ADC.

The AD9652 can support input clock frequencies of up to 1.24 GHz with a 1, 2, 4, and 8 integer clock divider used to generate the ADC sample clock. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle. The 16-bit output data (with an overrange bit) from each ADC is interleaved onto a single LVDS output port along with a double data rate (DDR) clock. Programming for setup and control are accomplished using a 3-wire SPI-compatible serial interface.

The AD9652 is available in a 144-ball CSP_BGA and is specified over the industrial temperature range of −40°C to +85°C. This product is protected by pending U.S. patents.

PRODUCT HIGHLIGHTS

1. Integrated dual, 16-bit, 310 MSPS ADCs.
2. On-chip buffer simplifies ADC driver interface.
3. Operation from 3.3 V and 1.8 V supplies and a separate digital output driver supply accommodating LVDS outputs.
4. Proprietary differential input maintains excellent signal-to-noise ratio (SNR) performance for input frequencies of up to 485 MHz.
5. SYNC input allows synchronization of multiple devices.
6. Three-wire, 3.3 V or 1.8 V SPI port for register programming and readback.

Rev. A Document Feedback

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REVISION HISTORY

5/14—Rev. 0 to Rev. A

Changes to Supply Current, Clock Divider = 1 Parameter and Power Consumption, Clock Divider = 1 Parameter, Table 1 ... 3

4/14—Revision 0: Initial Version

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD3 = 3.3 V, AVDD = AVDD_CLK = 1.8 V, SPIVDD = DRVDD = 1.8 V, sample rate = 310 MSPS (clock input = 1240 MHz, AD9652 divided by 4), VIN = −1.0 dBFS differential input, 2.5 V p-p full-scale input range, duty cycle stabilizer (DCS) enabled, dither disabled, unless otherwise noted.

Table 1.

Parameter	Temperature	Min	Typ	Max	Unit
RESOLUTION	Full		16		Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		1.5		mV
Gain Error	Full		−0.3		% FSR
Differential Nonlinearity (DNL) [1]	Full		−0.76/+1.1		LSB
Integral Nonlinearity (INL)[1]	Full		−4.5/+4.5		LSB
MATCHING CHARACTERISTIC					
Offset Error	Full		±0.7		mV
Gain Error	Full		±0.1		%FSR
TEMPERATURE DRIFT					
Offset Error	Full		±0.8		ppm/°C
Gain Error	Full		±16		ppm/°C
INPUT REFERRED NOISE					
V_{REF} = 1.25 V	25°C		3.7		LSB rms
ANALOG INPUT					
Input Span (for V_{REF} = 1.25 V)	Full		2.5		V p-p
Input Capacitance[2]	Full		5.8		pF
Input Resistance[3]	Full		27		kΩ
Input Common-Mode Voltage	Full		2.0	2.4	V
POWER SUPPLIES					
Supply Voltage					
AVDD3	Full	3.15	3.3	3.45	V
AVDD	Full	1.7	1.8	1.9	V
AVDD_CLK	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
SPIVDD	Full	1.7	1.8	3.6	V
Supply Current, Clock Divider = 1					
I_{AVDD3}	Full		145		mA
I_{AVDD}	Full		701		mA
I_{AVDD_CLK}	Full		56		mA
I_{DRVDD}	Full		180		mA
I_{SPIVDD}	Full		0.005		mA
POWER CONSUMPTION					
Clock Divider = 1					
Normal Operation[1]	Full		2160	2236	mW
Standby Power[4]	Full		80		mW
Power-Down Power	Full		1		mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Input resistance refers to the effective resistance between one differential input pin and AGND.
[4] Standby power is measured with a dc input and the CLK± pins inactive (that is, set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD3 = 3.3 V, AVDD = AVDD_CLK = 1.8 V, SPIVDD = DRVDD = 1.8 V, sample rate = 310 MSPS (clock input = 1240 MHz, AD9652 divided by 4), VIN = −1.0 dBFS differential input, 2.5 V p-p full-scale input range, DCS enabled, dither disabled, unless otherwise noted.

Table 2.

		V_{REF} = 1 V			V_{REF} = 1.25 V, Default			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DIFFERENTIAL INPUT VOLTAGE	25°C		2.0			2.5		V p-p
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 30 MHz (Use Nyquist 1 Settings)	25°C		74.0			75.4		dBFS
f_{IN} = 70 MHz (Use Nyquist 1 Settings)	25°C		73.6		74.0	75.0		dBFS
	Full				73.3			dBFS
f_{IN} = 70 MHz (Use Nyquist 1 Settings, with Dither Enabled)	25°C		73.1			74.3		dBFS
f_{IN} = 170 MHz (Use Nyquist 2 Settings)	25°C		72.1			73.7		dBFS
f_{IN} = 170 MHz (Use Nyquist 2 Settings, with Dither Enabled)	25°C		71.2			72.0		dBFS
f_{IN} = 305 MHz (Use Nyquist 2 Settings)	25°C		70.1			70.7		dBFS
f_{IN} = 400 MHz (Use Nyquist 3 Settings)	25°C		67.9			68.0		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 30 MHz (Use Nyquist 1 Settings)	25°C		72.8			74.2		dBFS
f_{IN} = 70 MHz (Use Nyquist 1 Settings)	25°C		73.5		73.8	74.6		dBFS
	Full				73.2			dBFS
f_{IN} = 70 MHz (Use Nyquist 1 Settings, with Dither Enabled)	25°C		73.0			74.0		dBFS
f_{IN} = 170 MHz (Use Nyquist 2 Settings)	25°C		72.0			72.6		dBFS
f_{IN} = 170 MHz (Use Nyquist 2 Settings, with Dither Enabled)	25°C		71.1			71.7		dBFS
f_{IN} = 305 MHz (Use Nyquist 2 Settings)	25°C					68.5		dBFS
f_{IN} = 400 MHz (Use Nyquist 3 Settings)	25°C					65.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 30 MHz (Use Nyquist 1 Settings)	25°C		11.8			12.0		Bits
f_{IN} = 70 MHz (Use Nyquist 1 Settings)	25°C		12		12.0	12.1		Bits
	Full				11.9			Bits
f_{IN} = 70 MHz (Use Nyquist 1 Settings, with Dither Enabled)	25°C		11.8			12.0		Bits
f_{IN} = 170 MHz (Use Nyquist 2 Settings)	25°C		11.7			11.8		Bits
f_{IN} = 170 MHz (Use Nyquist 2 Settings, with Dither Enabled)	25°C		11.5			11.6		Bits
f_{IN} = 305 MHz (Use Nyquist 2 Settings)	25°C					11.1		Bits
f_{IN} = 400 MHz (Use Nyquist 3 Settings)	25°C					10.6		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 30 MHz (Use Nyquist 1 Settings)	25°C		−96			−94		dBc
f_{IN} = 70 MHz (Use Nyquist 1 Settings)	25°C		−90			−87	−83	dBc
	Full						−83	dBc
f_{IN} = 70 MHz (Use Nyquist 1 Settings, with Dither Enabled)	25°C		−92			−89		dBc
f_{IN} = 170 MHz (Use Nyquist 2 Settings)	25°C		−87			−85		dBc
f_{IN} = 170 MHz (Use Nyquist 2 Settings, with Dither Enabled)	25°C		−87			−85		dBc
f_{IN} = 305 MHz (Use Nyquist 2 Settings)	25°C		−89			−86		dBc
f_{IN} = 400 MHz (Use Nyquist 3 Settings)	25°C		−80			−77		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 30 MHz (Use Nyquist 1 Settings)	25°C		96			94		dBc
f_{IN} = 70 MHz (Use Nyquist 1 Settings)	25°C		90		83	87		dBc
	Full				83			dBc
f_{IN} = 70 MHz (Use Nyquist 1 Settings. with Dither Enabled)	25°C		92			89		dBc
f_{IN} = 170 MHz (Use Nyquist 2 Settings)	25°C		84			85		dBc
f_{IN} = 170 MHz (Use Nyquist 2 Settings, with Dither Enabled)	25°C		87			85		dBc
f_{IN} = 305 MHz (Use Nyquist 2 Settings)	25°C		89			86		dBc
f_{IN} = 400 MHz (Use Nyquist 3 Settings)	25°C		80			77		dBc

Parameter[1]	Temperature	V_{REF} = 1 V Min	V_{REF} = 1 V Typ	V_{REF} = 1 V Max	V_{REF} = 1.25 V, Default Min	V_{REF} = 1.25 V, Default Typ	V_{REF} = 1.25 V, Default Max	Unit
WORST OTHER (NOT INCLUDING 2nd or 3rd HARMONIC)								
f_{IN} = 30 MHz (Use Nyquist 1 Settings)	25°C		−101			−102		dBc
f_{IN} = 70 MHz (Use Nyquist 1 Settings)	25°C		−99			−98	−90	dBc
	Full						−86	dBc
f_{IN} = 70 MHz (Use Nyquist 1 Settings, with Dither Enabled)	25°C		−100			−100		dBc
f_{IN} = 170 MHz (Use Nyquist 2 Settings)	25°C		−91			−90		dBc
f_{IN} = 170 MHz (Use Nyquist 2 Settings, with Dither Enabled)	25°C		−90			−95		dBc
f_{IN} = 305 MHz (Use Nyquist 2 Settings)	25°C		−98			−97		dBc
f_{IN} = 400 MHz (Use Nyquist 3 Settings)	25°C		−92			−91		dBc
TWO-TONE SFDR								
f_{IN} = 70.1 MHz (−7 dBFS), 72.1 MHz (−7 dBFS)	25°C					93		dBc
f_{IN} = 184.12 MHz (−7 dBFS), 187.12 MHz (−7 dBFS)	25°C					83		dBc
CROSSTALK[2]	Full		90			90		dB
FULL POWER BANDWIDTH[3]	25°C		485			485		MHz
NOISE BANDWIDTH[4]	25°C		650			650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.
[3] Full power bandwidth is the bandwidth of operation in which proper ADC performance can be achieved.
[4] Noise bandwidth is the −3 dB bandwidth for the ADC inputs across which noise can enter the ADC and is not attenuated internally.

DIGITAL SPECIFICATIONS

AVDD3 = 3.3 V, AVDD = AVDD_CLK = 1.8 V, SPIVDD = DRVDD = 1.8 V, sample rate = 310 MSPS (clock input = 1240 MHz, AD9652 divided by 4), VIN = −1.0 dBFS differential input, 2.5 V p-p full-scale input range, DCS enabled, dither disabled, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)						
Logic Compliance				CMOS/LVDS/LVPECL		
Differential Input Voltage		Full	0.3		3.6	V p-p
Input Voltage Range		Full	AGND		AVDD_CLK	V
Internal Common-Mode Bias		Full		0.9		V
Input Common-Mode Range		Full	0.9		1.4	V
High Level Input Current		Full	+10		+145	µA
Low Level Input Current		Full	−155		−15	µA
Input Capacitance[1]		Full		5		pF
Input Resistance[1]		Full		10		kΩ
SYNC INPUT						
Logic Compliance				CMOS/LVDS		
Internal Bias		Full		0.9		V
Input Voltage Range		Full	AGND		AVDD_CLK	V
High Level Input Voltage		Full	1.2		AVDD_CLK	V
Low Level Input Voltage		Full	AGND		0.6	V
High Level Input Current		Full	−15		+110	µA
Low Level Input Current		Full	−105		+15	µA
Input Capacitance		Full		1.5		pF
Input Resistance		Full		16		kΩ

Parameter	Test Conditions/Comments	Temperature	Min	Typ	Max	Unit
LOGIC INPUT (CSB)[2]						
High Level Input Voltage		Full	1.22		SPIVDD	V
Low Level Input Voltage		Full	0		0.6	V
High Level Input Current		Full	−65		+65	µA
Low Level Input Current		Full	−135		0	µA
Input Resistance		Full		26		kΩ
Input Capacitance		Full		2		pF
LOGIC INPUT (SCLK)[3]						
High Level Input Voltage		Full	1.22		SPIVDD	V
Low Level Input Voltage		Full	0		0.6	V
High Level Input Current		Full	0		110	µA
Low Level Input Current		Full	−60		+50	µA
Input Resistance		Full		26		kΩ
Input Capacitance		Full		2		pF
LOGIC INPUTS (SDIO)[2]						
High Level Input Voltage		Full	1.22		SPIVDD	V
Low Level Input Voltage		Full	0		0.6	V
High Level Input Current		Full	−65		+70	µA
Low Level Input Current		Full	−135		0	µA
Input Resistance		Full		26		kΩ
Input Capacitance		Full		5		pF
LOGIC INPUTS (PDWN)[3]						
High Level Input Voltage		Full	1.22		DRVDD	V
Low Level Input Voltage		Full	0		0.6	V
High Level Input Current		Full	−80		+190	µA
Low Level Input Current		Full	−145		+130	µA
Input Resistance		Full		26		kΩ
Input Capacitance		Full		5		pF
DIGITAL OUTPUTS						
LVDS Data and OR± Outputs	Assumes nominal 100 Ω differential termination					
ANSI Mode						
Differential Output Voltage (V_{OD})	Maximum setting, default	Full	310	350	450	mV
Output Offset Voltage (V_{OS})		Full	1.15	1.22	1.35	V
Reduced Swing Mode						
Differential Output Voltage (V_{OD})	Minimum setting	Full	150	200	280	mV
Output Offset Voltage (V_{OS})		Full	1.15	1.22	1.35	V

[1] Input capacitance/resistance refers to the effective capacitance/resistance between one differential input pin and AGND.
[2] Internal weak pull-up.
[3] Internal weak pull-down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Test Conditions/Comments	Temperature	Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS (CLK±)						
Input Clock Rate		Full	80		1240	MHz
Conversion Rate[1]		Full	80		310	MSPS
Period—Divide-by-1 Mode (t_{CLK})		Full	3.2			ns
Pulse Width High (t_{CH}), Minimum						
Divide-by-1 Mode	DCS enabled	Full		0.8		ns
	DCS disabled	Full		1.3		ns
Divide-by-2 Mode Through Divide-by-8 Mode		Full		0.8		ns
Aperture Delay (t_A)		Full		1.0		ns
Aperture Uncertainty (Jitter, t_J)		Full		0.1		ps rms
DATA OUTPUT PARAMETERS						
LVDS Mode						
Data Propagation Delay (t_{PD})		Full		290		ps
DCO± Propagation Delay (t_{DCO})		Full		290		ps
DCO±-to-Data Skew (t_{SKEW})		Full		0		ns
Pipeline Delay (Latency)		Full		26		Cycles
Wake-Up Time	From standby	Full		100		µs
	From power-down	Full		1		sec
Out-of-Range Recovery Time		Full		3		Cycles

[1] Conversion rate is the clock rate after the divider.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to the rising edge of CLK+ setup time		0.1		ns
t_{HSYNC}	SYNC to the rising edge of CLK+ hold time		0.1		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK is in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK is in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Timing Diagrams)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Timing Diagrams)	10			ns
t_{SPI_RST}	Time required after power-up, hard or soft reset until SPI access is available (not shown in Timing Diagrams)	500			µs

Timing Diagrams

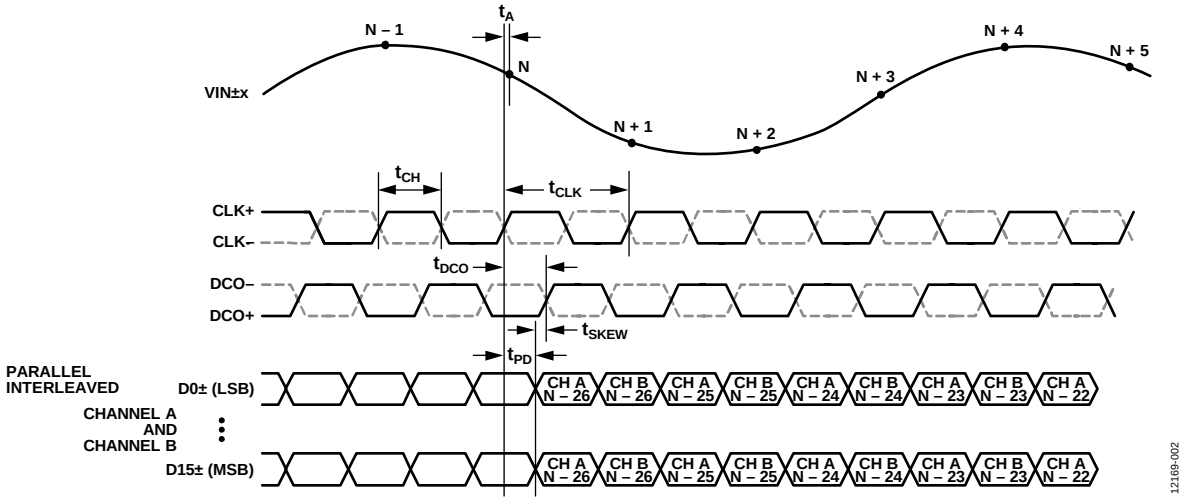

Figure 2. LVDS Data Output Timing

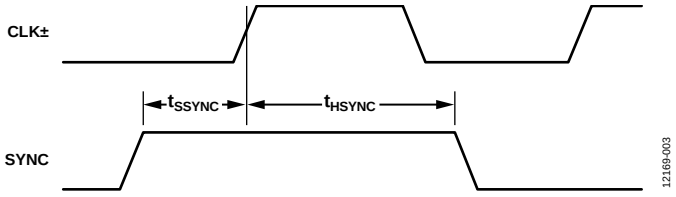

Figure 3. SYNC Timing Inputs

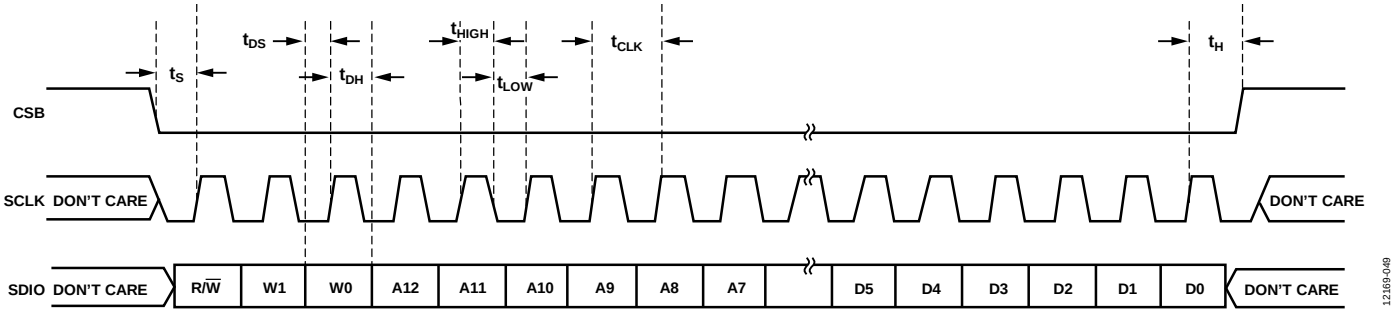

Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD3 to AGND	−0.3 V to +3.6 V
AVDD_CLK to AGND	−0.3 V to +2.0 V
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
SPIVDD to AGND	−0.3 V to +3.6 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	1.2 V to 3.0 V
CLK+, CLK− to AGND	−0.3 V to AVDD_CLK + 0.2 V
SYNC to AGND	−0.3 V to AVDD_CLK + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to SPIVDD + 0.3 V
SCLK to AGND	−0.3 V to SPIVDD + 0.3 V
SDIO to AGND	−0.3 V to SPIVDD + 0.3 V
PDWN to AGND	−0.3 V to DRVDD + 0.3 V
OR+/OR− to AGND	−0.3 V to DRVDD + 0.3 V
D0± Through D15± to AGND	−0.3 V to DRVDD + 0.3 V
DCO± to AGND	−0.3 V to DRVDD + 0.3 V
Environmental	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Typical θ_{JA} is specified for both a 4-layer printed circuit board (PCB) with a solid ground plane from the JEDEC 51-2 and an 8-layer PCB. The 8-layer PCB has 2 oz copper layers (M1 and M8), 1 oz copper inner layers, and vias connecting to layers M2, M5, and M7.

As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	Board Type	θ_{JA}[2]	Unit
144-Ball CSP_BGA 10 mm × 10 mm (BC-144-6)	0	8-layer PCB	15.8	°C/W
	1.0	8-layer PCB	13.9	°C/W
	0	JEDEC[1]	21.7	°C/W
	1.0	JEDEC[1]	19.2	°C/W

[1] Per JEDEC JESD51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

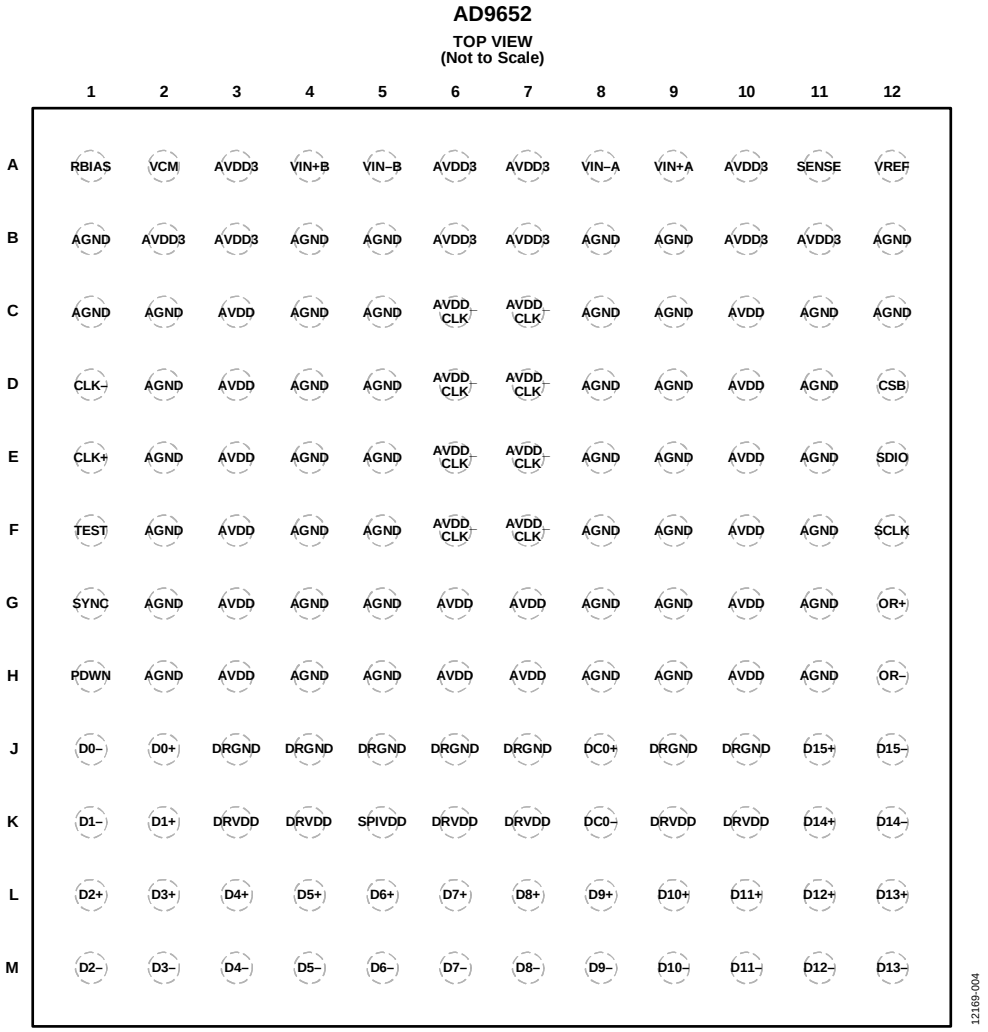

Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
K5	SPIVDD	Supply	Serial Interface Logic Voltage Supply (1.8 V Typical, 3.3 V Optional)
K3, K4, K6, K7, K9, K10	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
A3, A6, A7, A10, B2, B3, B6, B7, B10, B11	AVDD3	Supply	3.3 V Analog Power Supply (3.3 V Nominal).
C6, C7, D6, D7, E6, E7, F6, F7	AVDD_CLK	Supply	1.8 V Analog Power Supply for Clock Circuitry (1.8 V Nominal).
C3, C10, D3, D10, E3, E10, F3, F10, G3, G6, G7, G10, H3, H6, H7, H10	AVDD	Supply	1.8 V Analog Power Supply (1.8 V Nominal).
B1, B4, B5, B8, B9, B12, C1, C2, C4, C5, C8, C9, C11, C12, D2, D4, D5, D8, D9, D11, E2, E4, E5, E8, E9, E11, F2, F4, F5, F8, F9, F11, G2, G4, G5, G8, G9, G11, H2, H4, H5, H8, H9, H11	AGND	Analog Ground	Analog Ground Reference for AVDD3, AVDD_CLK, and AVDD.

Pin No.	Mnemonic	Type	Description
J3	DRGND	Digital Ground	Digital and Output Driver Ground Reference.
J4	DRGND	Digital Ground	Digital and Output Driver Ground Reference.
J5	DRGND	Digital Ground	Digital and Output Driver Ground Reference.
J6	DRGND	Digital Ground	Digital and Output Driver Ground Reference.
J7	DRGND	Digital Ground	Digital and Output Driver Ground Reference.
J9	DRGND	Digital Ground	Digital and Output Driver Ground Reference.
J10	DRGND	Digital Ground	Digital and Output Driver Ground Reference.
ADC Analog			
A9	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
A8	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
A4	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
A5	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
A2	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. Decouple this pin to ground using a 0.1 µF capacitor.
A1	RBIAS	Output	External Bias Resister Connection. A 10 kΩ resister must be connected between this pin and analog ground (AGND).
A12	VREF	Input/Output	Voltage Reference Input/Output.
A11	SENSE	Input	Reference Mode Selection (See Table 12).
E1	CLK+	Input	ADC Clock Input (True).
D1	CLK−	Input	ADC Clock Input (Complement).
Digital Inputs			
F1	TEST	Input	Pull-Down. Unused digital input, pull to ground through a 50 Ω resistor.
G1	SYNC	Input	Digital Input Clock Synchronization Pin. Tie low if unused.
H1	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Register 0x08 in Table 17).
Digital Outputs			
J2	D0+	Output	Channel A/Channel B LVDS Output Data 0 (True, LSB).
J1	D0−	Output	Channel A/Channel B LVDS Output Data 0 (Complement, LSB).
K2	D1+	Output	Channel A/Channel B LVDS Output Data 1 (True).
K1	D1−	Output	Channel A/Channel B LVDS Output Data 1 (Complement).
L1	D2+	Output	Channel A/Channel B LVDS Output Data 2 (True).
M1	D2−	Output	Channel A/Channel B LVDS Output Data 2 (Complement).
L2	D3+	Output	Channel A/Channel B LVDS Output Data 3 (True).
M2	D3−	Output	Channel A/Channel B LVDS Output Data 3 (Complement).
L3	D4+	Output	Channel A/Channel B LVDS Output Data 4 (True).
M3	D4−	Output	Channel A/Channel B LVDS Output Data 4 (Complement).
L4	D5+	Output	Channel A/Channel B LVDS Output Data 5 (True).
M4	D5−	Output	Channel A/Channel B LVDS Output Data 5 (Complement).
L5	D6+	Output	Channel A/Channel B LVDS Output Data 6 (True).
M5	D6−	Output	Channel A/Channel B LVDS Output Data 6 (Complement).
L6	D7+	Output	Channel A/Channel B LVDS Output Data 7 (True).
M6	D7−	Output	Channel A/Channel B LVDS Output Data 7 (Complement).
L7	D8+	Output	Channel A/Channel B LVDS Output Data 8 (True).
M7	D8−	Output	Channel A/Channel B LVDS Output Data 8 (Complement).
L8	D9+	Output	Channel A/Channel B LVDS Output Data 9 (True).
M8	D9−	Output	Channel A/Channel B LVDS Output Data 9 (Complement).
L9	D10+	Output	Channel A/Channel B LVDS Output Data 10 (True).
M9	D10−	Output	Channel A/Channel B LVDS Output Data 10 (Complement).
L10	D11+	Output	Channel A/Channel B LVDS Output Data 11 (True).
M10	D11−	Output	Channel A/Channel B LVDS Output Data 11 (Complement).
L11	D12+	Output	Channel A/Channel B LVDS Output Data 12 (True).
M11	D12−	Output	Channel A/Channel B LVDS Output Data 12 (Complement).

Pin No.	Mnemonic	Type	Description
L12	D13+	Output	Channel A/Channel B LVDS Output Data 13 (True).
M12	D13−	Output	Channel A/Channel B LVDS Output Data 13 (Complement).
K11	D14+	Output	Channel A/Channel B LVDS Output Data 14 (True).
K12	D14−	Output	Channel A/Channel B LVDS Output Data 14 (Complement).
J11	D15+	Output	Channel A/Channel B LVDS Output Data 15 (True, MSB).
J12	D15−	Output	Channel A/Channel B LVDS Output Data 15 (Complement, MSB).
G12	OR+	Output	Channel A/Channel B LVDS Overrange (True).
H12	OR−	Output	Channel A/Channel B LVDS Overrange (Complement).
J8	DCO+	Output	Channel A/Channel B LVDS Data Clock Output (True).
K8	DCO−	Output	Channel A/Channel B LVDS Data Clock Output (Complement).
SPI Control			
F12	SCLK	Input	SPI Serial Clock.
E12	SDIO	Input/Output	SPI Serial Data Input/Output.
D12	CSB	Input	SPI Chip Select (Active Low). This pin must be pulled high at power-up.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD3 = 3.3 V, AVDD = AVDD_CLK = 1.8 V, SPIVDD = DRVDD = 1.8 V, sample rate = 310 MSPS (clock input = 1240 MHz, AD9652 divide by 4), VIN = −1.0 dBFS differential, V_{REF} = 1.25 V, DCS enabled, dither disabled, unless otherwise noted.

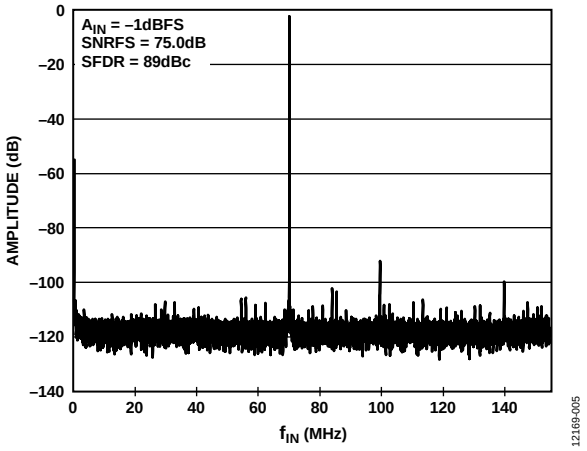

Figure 6. Single Tone Fast Fourier Transform (FFT) with f_{IN} = 70.1 MHz (NSD = −156.7 dBFS/Hz)

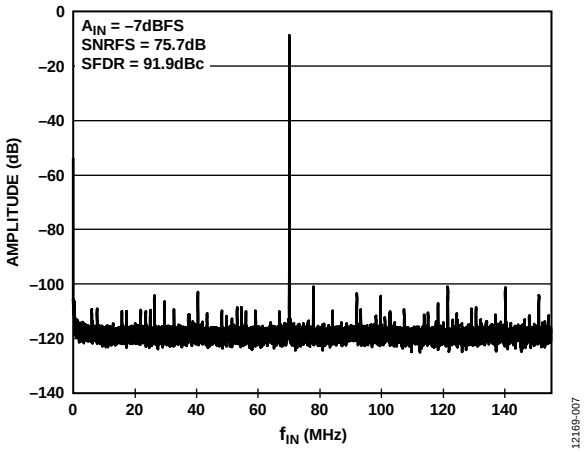

Figure 7. Single Tone FFT with f_{IN} = 70.1 MHz at −7 dBFS (NSD = −157.6 dBFS/Hz)

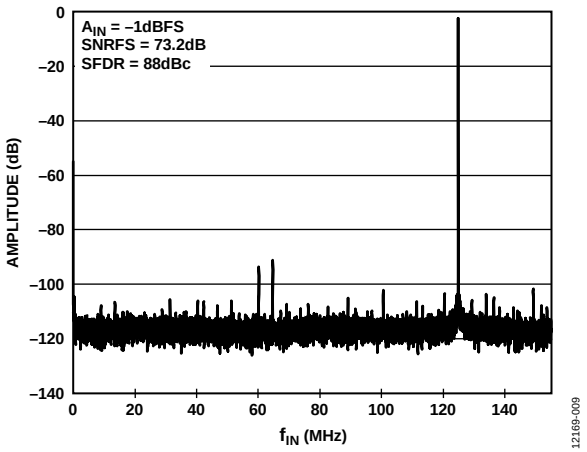

Figure 8. Single Tone FFT with f_{IN} = 185 MHz. at −1 dBFS (NSD = −155.2 dBFS/Hz), Register 0x22A = 0x01

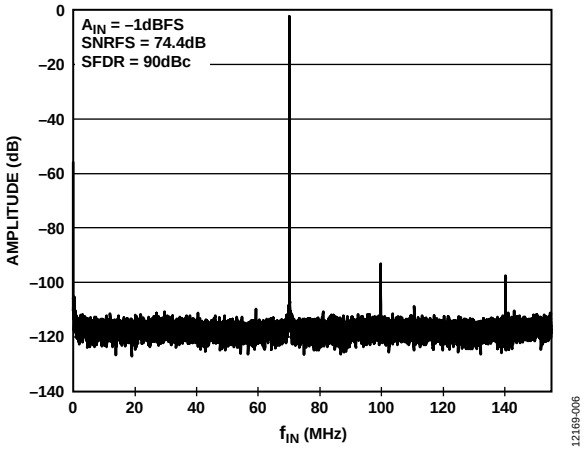

Figure 9. Single Tone FFT with f_{IN} = 70.1 MHz with Dither (NSD = −156.3 dBFS/Hz)

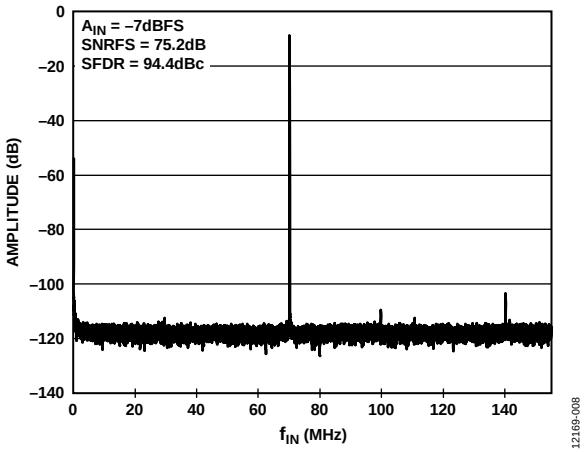

Figure 10. Single Tone FFT with f_{IN} = 70.1 MHz at −7 dBFS with Dither (NSD = −157.1 dBFS/Hz)

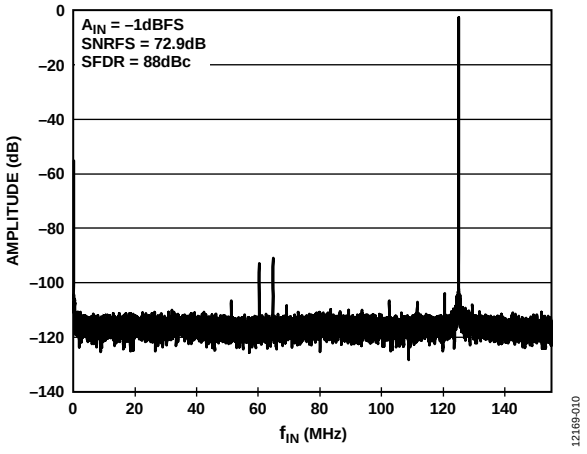

Figure 11. Single Tone FFT with f_{IN} = 185 MHz at −1 dBFS with Dither (NSD = −154.9 dBFS/Hz), Register 0x22A = 0x01

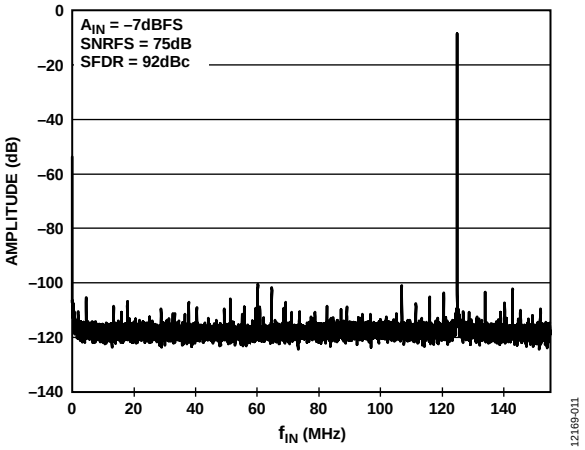

Figure 12. Single Tone FFT with f_{IN} = 185 MHz at −7 dBFS (NSD = −156.9 dBFS/Hz), Register 0x22A = 0x01

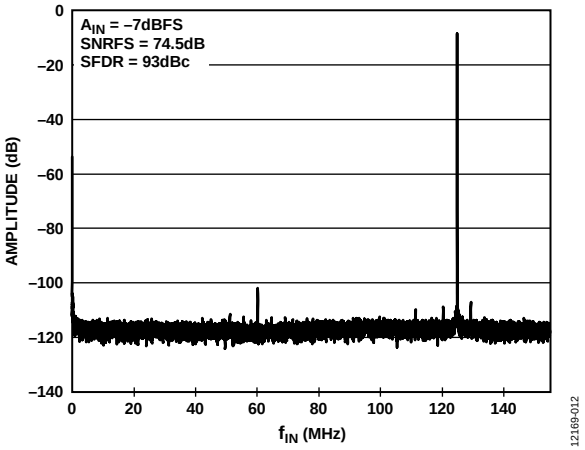

Figure 15. Single Tone FFT with f_{IN} = 185 MHz at −7dBFS with Dither (NSD = −156.4 dBFS/Hz), Register 0x22A = 0x01

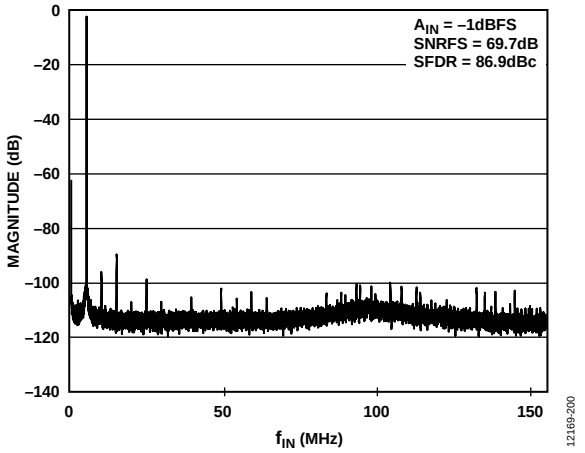

Figure 13. FFT f_{IN} = 305 MHz, A_{IN} = −1 dBFS, Dither Off, Register 0x22A = 0x01

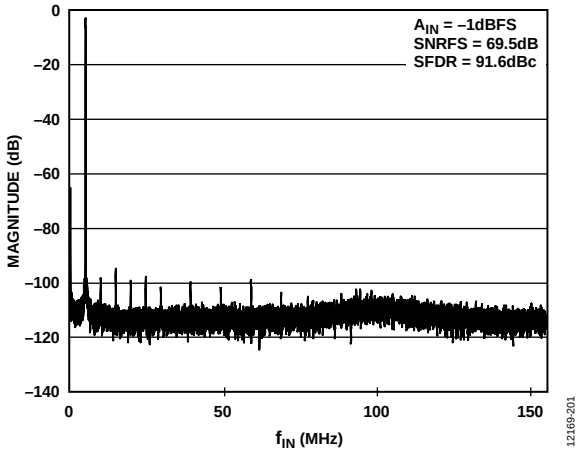

Figure 16. FFT f_{IN} = 305 MHz, A_{IN} = −1 dBFS, Dither On, Register 0x22A = 0x01

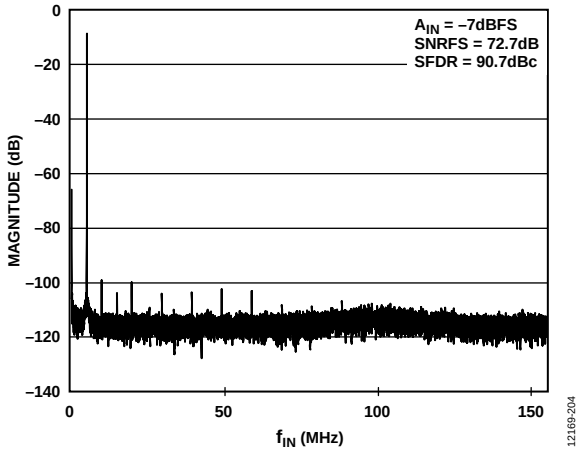

Figure 14. FFT f_{IN} = 305 MHz, A_{IN} = −7 dBFS, Dither Off, Register 0x22A = 0x01

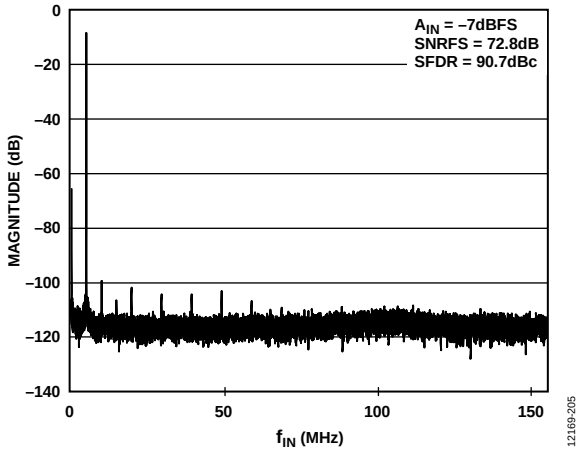

Figure 17. FFT f_{IN} = 305 MHz, A_{IN} = −7 dBFS, Dither On, Register 0x22A = 0x01

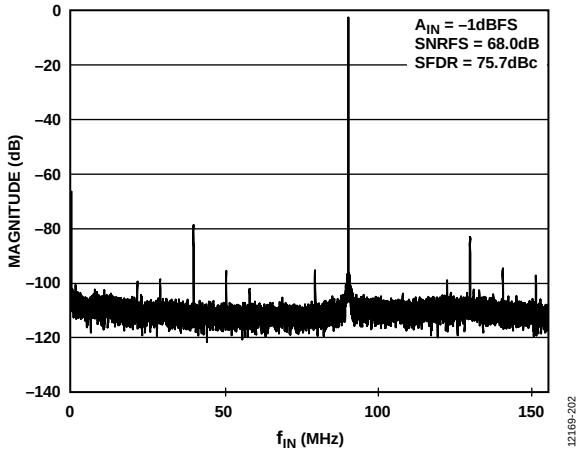

Figure 18. FFT f_{IN} = 400 MHz, A_{IN} = −1 dBFS, Dither Off, Register 0x22A = 0x02

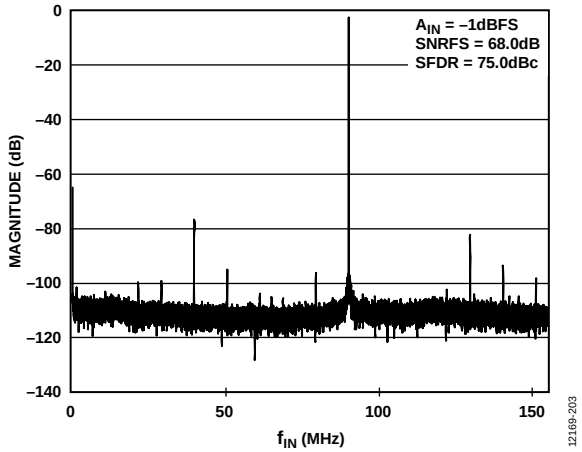

Figure 21. FFT f_{IN} = 400 MHz, A_{IN} = −1 dBFS, Dither On, Register 0x22A = 0x02

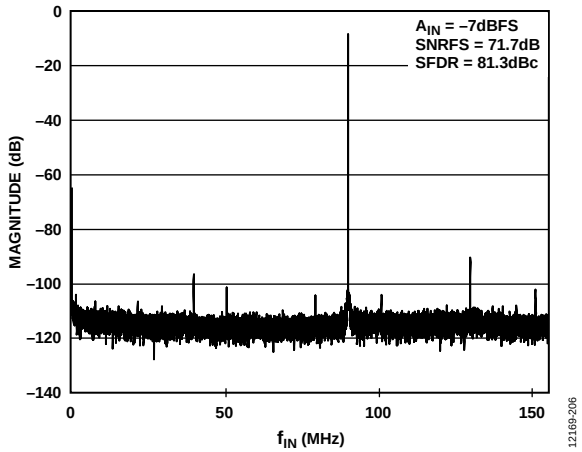

Figure 19. FFT f_{IN} = 400 MHz, A_{IN} = −7 dBFS, Dither Off, Register 0x22A = 0x02

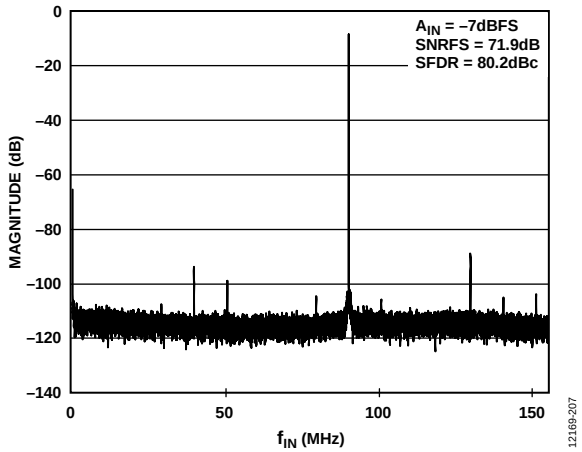

Figure 22. FFT f_{IN} = 400 MHz, A_{IN} = −7 dBFS, Dither On, Register 0x22A = 0x02

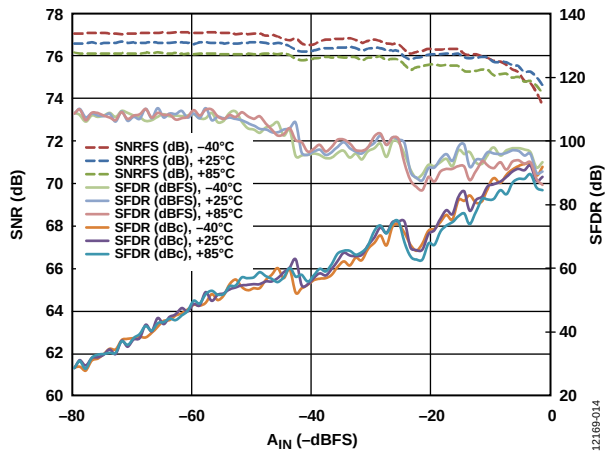

Figure 20. Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz, V_{REF} = 1.25 V, Over Temperature, Dither Off

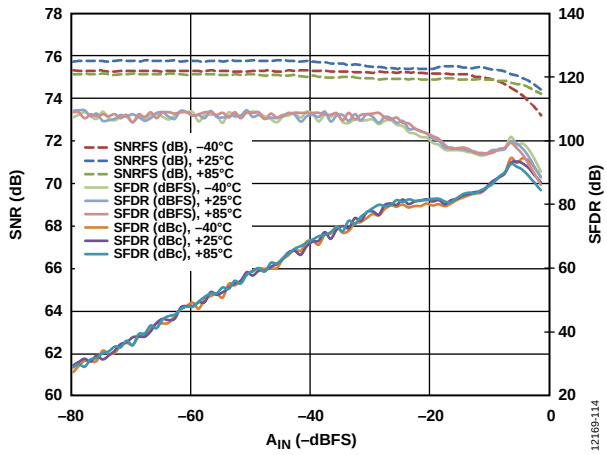

Figure 23. Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz, V_{REF} = 1.25 V, Over Temperature, Dither On

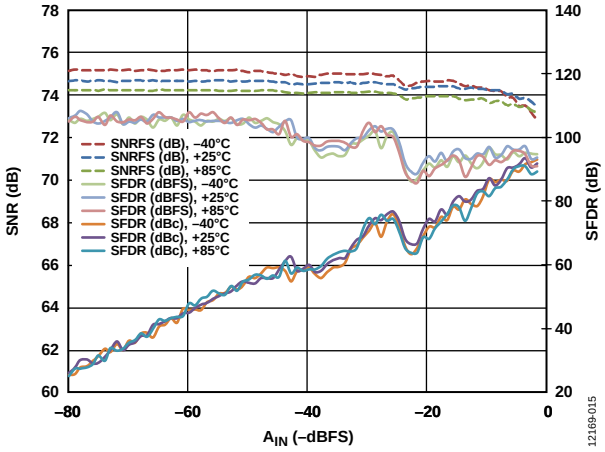

Figure 24. Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz, V_{REF} = 1.0 V, Over Temperature, Dither Off

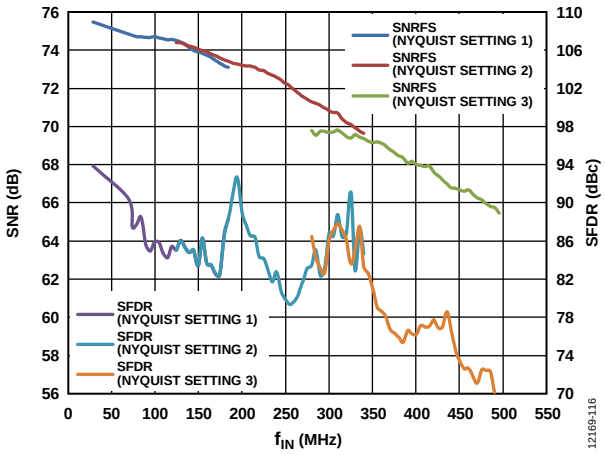

Figure 25. Single Tone SNR/SFDR vs. Input Frequency (f_{IN}), Amplitude = –1 dBFS, V_{REF} = 1.25 V

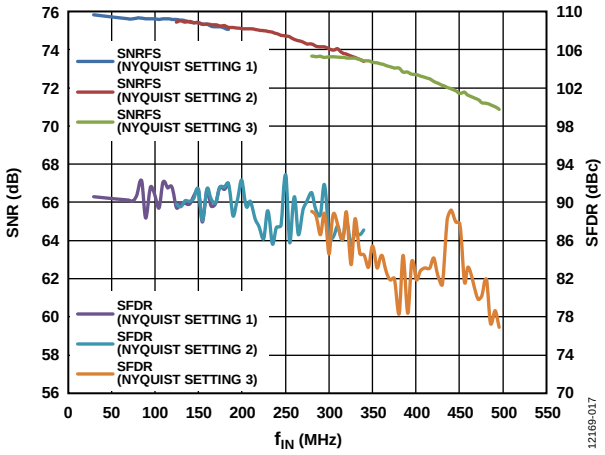

Figure 26. Single Tone SNR/SFDR vs. Input Frequency (f_{IN}), Amplitude = –7 dBFS, V_{REF} = 1.25 V

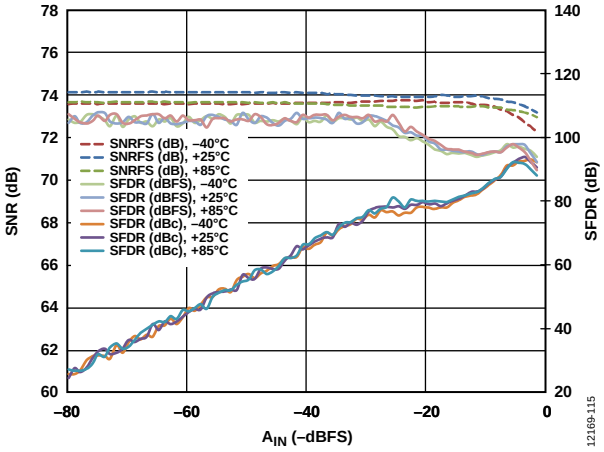

Figure 27. Single Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 90.1 MHz, V_{REF} = 1.0 V, Over Temperature, Dither On

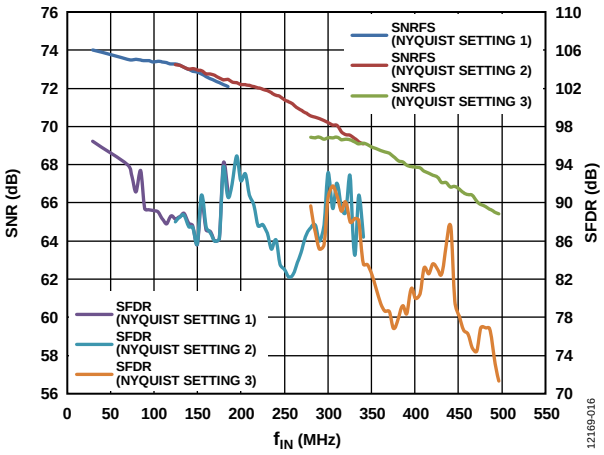

Figure 28. Single Tone SNR/SFDR vs. Input Frequency (f_{IN}), Amplitude =–1 dBFS, V_{REF} = 1.0 V

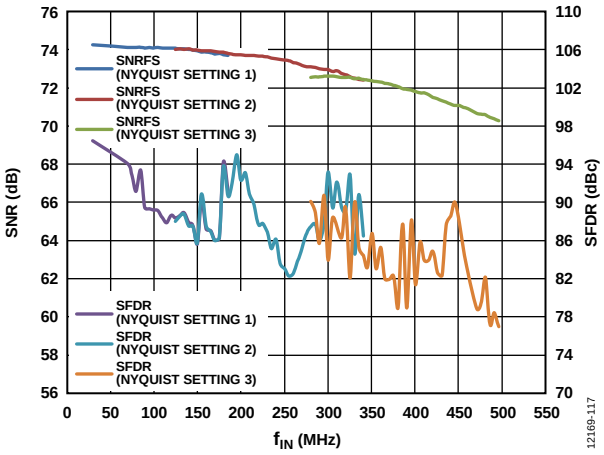

Figure 29. Single Tone SNR/SFDR vs. Input Frequency (f_{IN}), Amplitude = –7 dBFS, V_{REF} = 1.0 V

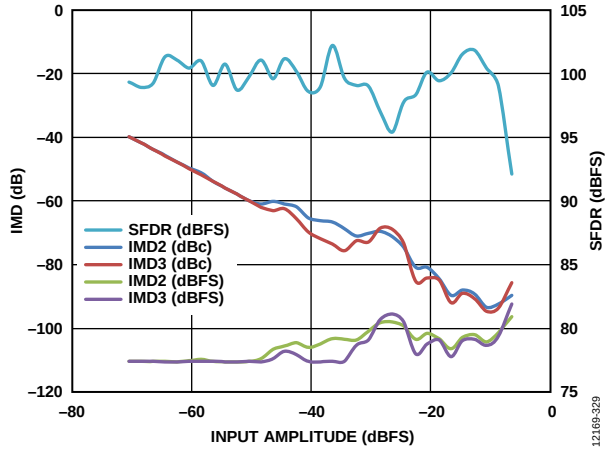

Figure 30. Two Tone SFDR/Intermodulation Distortion (IMD) vs. Input Amplitude, for f_{IN} = 70.1 MHz and 72.1 MHz, Dither Disabled

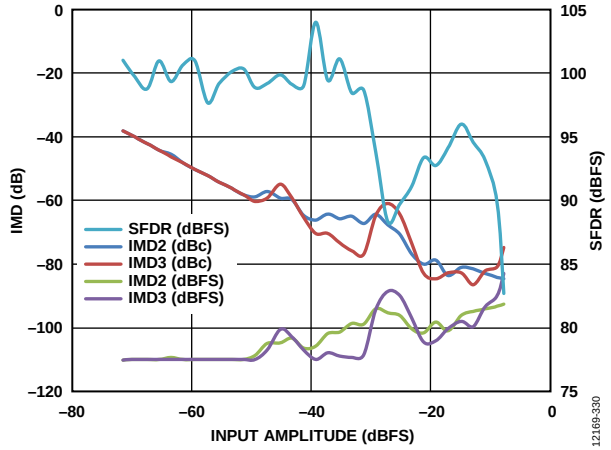

Figure 31. Two Tone SFDR/IMD vs. Input Amplitude, for f_{IN} = 184 MHz and 187 MHz, Dither Disabled, Register 0x22A = 0x01

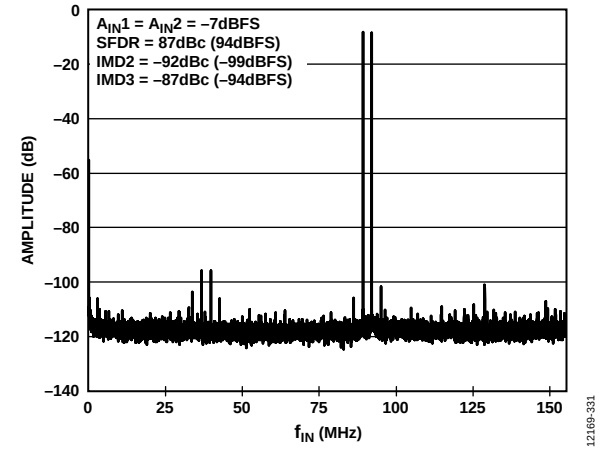

Figure 32. Two Tone FFT with f_{IN} = 89.1 MHz and 92.1 MHz, VREF = 1.25 V

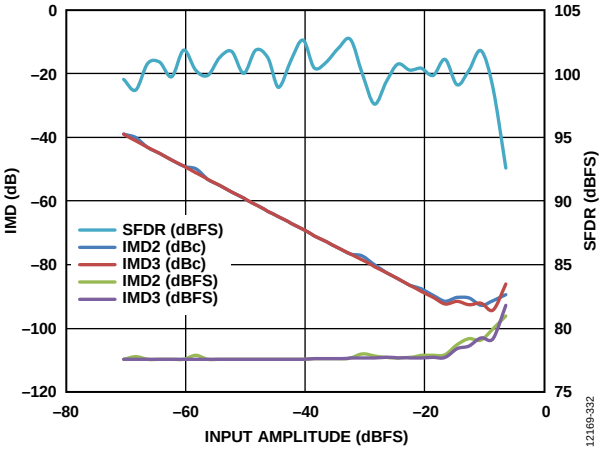

Figure 33. Two Tone SFDR/IMD vs. Input Amplitude, for f_{IN} = 70.1 MHz and 72.1 MHz, Dither Enabled

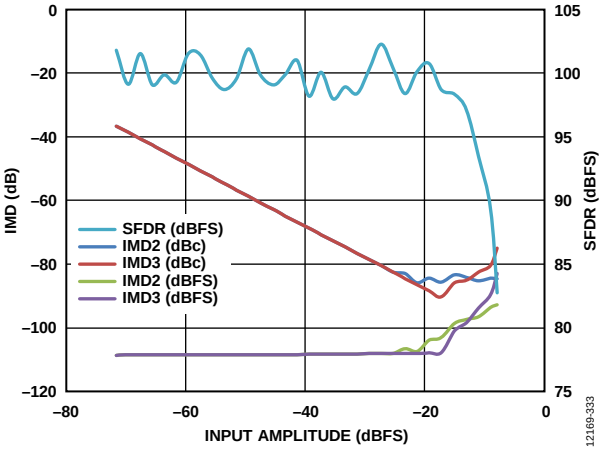

Figure 34. Two Tone SFDR/IMD vs. Input Amplitude, for f_{IN} = 184 MHz and 187 MHz, Dither Enabled, Register 0x22A = 0x01

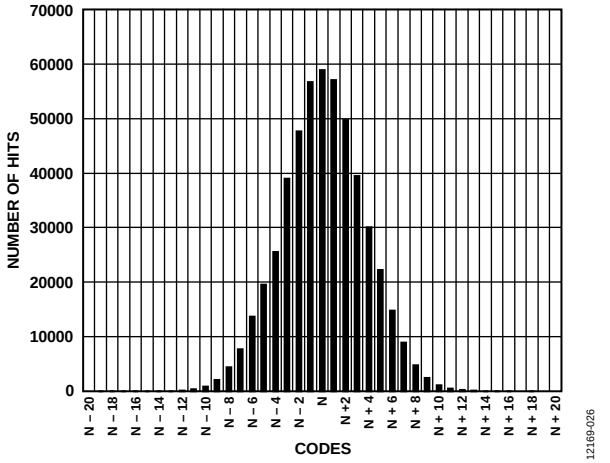

Figure 35. Grounded Input Histogram

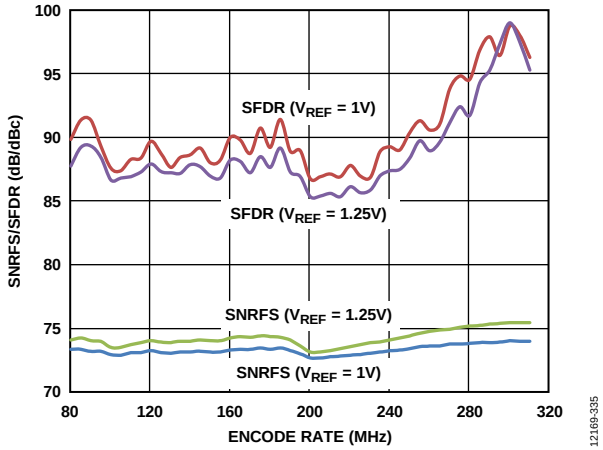

Figure 36. Encode Rate Sweep, f_{IN} = 90.1 MHz at −7 dBFS, V_{REF} = 1.25 V and 1.0 V

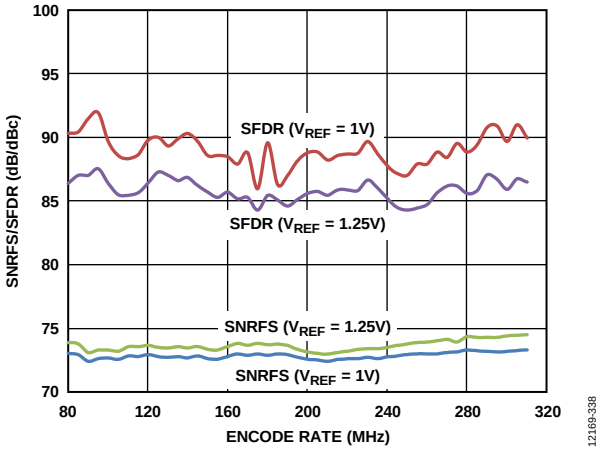

Figure 39. Encode Rate Sweep, f_{IN} = 90.1 MHz at −1 dBFS, V_{REF} = 1.25 V and 1.0 V

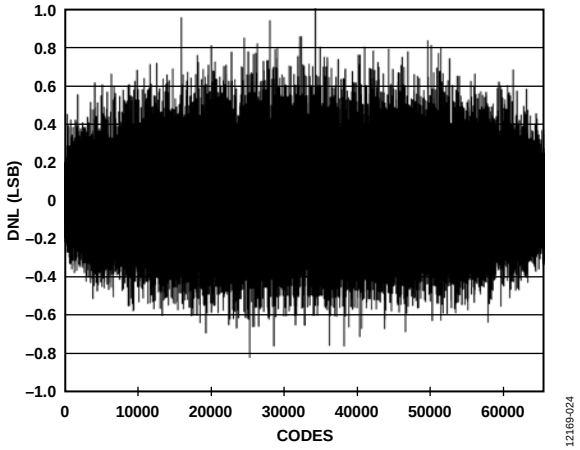

Figure 37. DNL with Dither Off, f_{IN} = 30 MHz

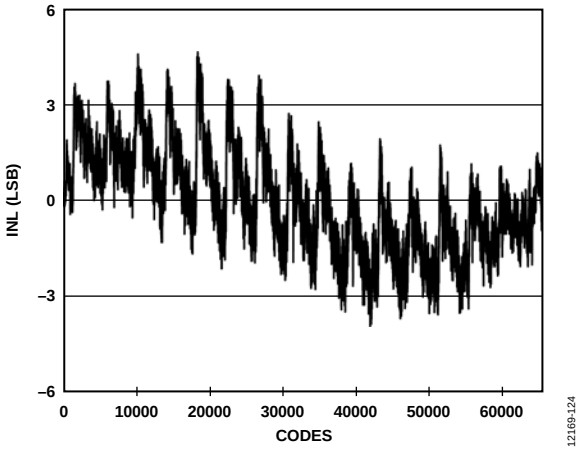

Figure 40. INL with Dither Off, f_{IN} = 30 MHz

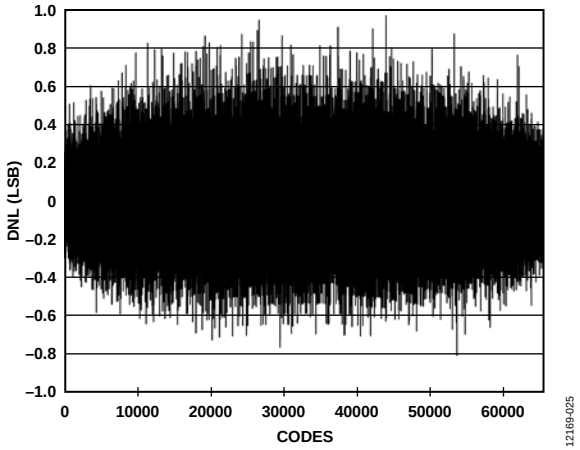

Figure 38. DNL with Dither On, f_{IN} = 30 MHz

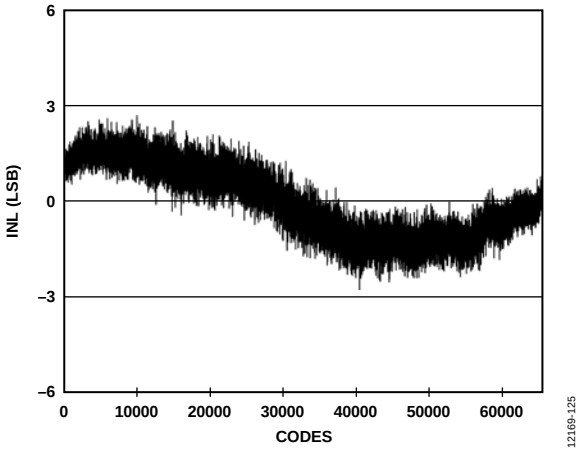

Figure 41. INL with Dither On, f_{IN} = 30 MHz

EQUIVALENT CIRCUITS

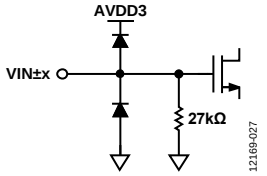

Figure 42. Equivalent Analog Input Circuit

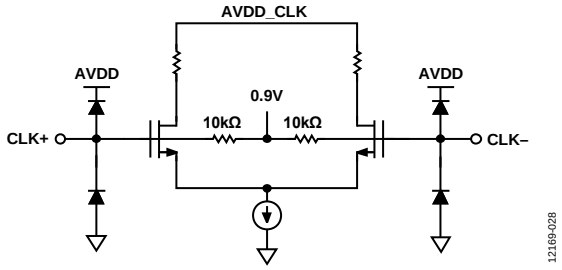

Figure 43. Equivalent Clock Input Circuit

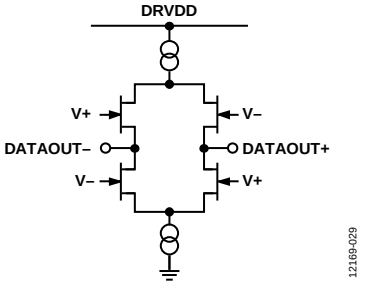

Figure 44. Equivalent LVDS Output Circuit (DCO±, OR±, and D0± to D15±)

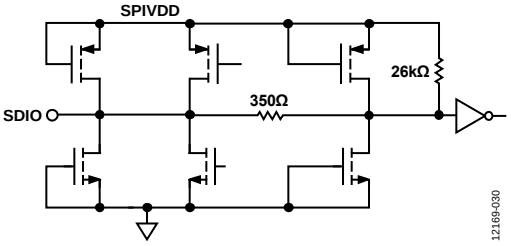

Figure 45. Equivalent SDIO Circuit

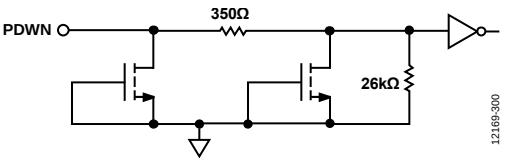

Figure 46. Equivalent PDWN Input Circuit

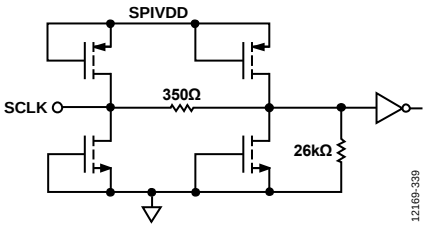

Figure 47. Equivalent SCLK Input Circuit

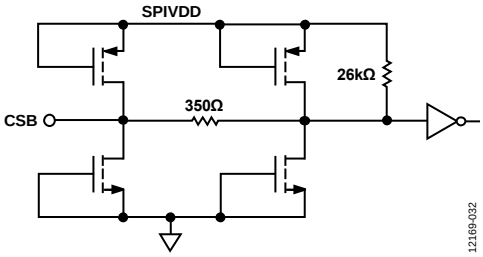

Figure 48. Equivalent CSB Input Circuit

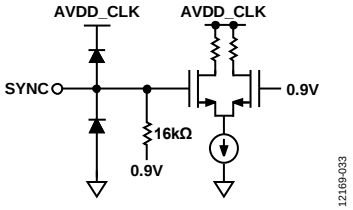

Figure 49. Equivalent SYNC Input Circuit

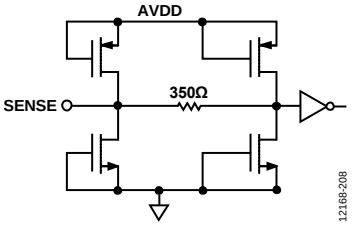

Figure 50. Equivalent SENSE Circuit

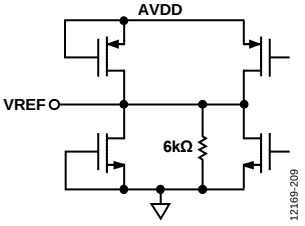

Figure 51. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9652 is a dual, 16-bit ADC with sampling speeds of up to 310 MSPS. The AD9652 is designed to support communications and instrumentation applications where high performance and wide bandwidth are desired.

The dual ADC design can be used for diversity receivers, where the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample frequencies from dc to 310 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. A typical operation of 485 MHz at the analog input is permitted but occurs at the expense of increased ADC noise and distortion.

Synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD9652 are accomplished using a 3-wire, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9652 consists of a dual, buffered front-end sample-and-hold circuit, followed by a pipelined switched-capacitor ADC. The AD9652 uses a unique architecture that utilizes the benefits of pipelined converters, as well as a novel input circuit to maximize performance of the first stage.

The quantized outputs from each stage are combined to produce a 16-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residual multiplying DAC (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The AD9652 uses internal digital processing to continually track internal errors that occur at each of the pipeline stages and corrects for them to ensure continuous performance over various operating conditions. This requires additional start-up time due to the resetting and collection of correction data.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers enter a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog inputs to the AD9652 are high performance differential buffers that are designed for optimum performance while processing a differential input signal. The input buffer provides a consistent input impedance to ease interface of the analog input.

The differential analog input impedance is approximately 54 kΩ in parallel with a 5.8 pF capacitor. A passive network of discrete components can be used to create a low-pass filter at the ADC input; the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, reduce the shunt capacitors. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

The AD9652 uses internal optimized settings for the various input signal frequencies. Register 0x22A is used to configure the ADC for the desired frequency band.

Table 9. Register 0x22A Settings

Register 0x22A Setting	Input Frequency Range
0 (Default]	0 to 155 MHz (1st Nyquist)
1	155 to 310 MHz (2nd Nyquist)
2	310 MHz and above (3rd Nyquist)

For best dynamic performance, the source impedances driving each of the differential inputs, match VIN±x, and differentially balance the inputs.

Input Common Mode

The analog inputs of the AD9652 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that the common-mode voltage equals 2.0 V is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. The VCM pin must be decoupled to ground with a 0.1 µF capacitor, as described in the Applications Information section. Place this decoupling capacitor close to the pin to minimize the series resistance and inductance between the device and this capacitor.

Common-Mode Voltage Servo

In applications where there may be a voltage loss between the VCM output of the AD9652 and the analog inputs, the common-mode voltage servo can be enabled. When the inputs are ac-coupled and a resistance of >100 Ω is placed between the VCM output and the analog inputs, a significant voltage drop can occur; enable the common-mode voltage servo. Setting Bit 0 in Register 0x0F to a logic high enables the VCM servo mode. In this mode, the AD9652 monitors the common-mode

input level at the analog inputs and adjusts the VCM output level to keep the common-mode input voltage at an optimal level. If both channels are operational, Channel A is monitored. However, if Channel A is in power-down or standby mode, then Channel B input is monitored.

Dither

The AD9652 has an optional internal dither circuitry that can be used to improve SFDR, particularly for small signals. Dithering is the act of injecting a known but random amount of white noise into the input of the AD9652. Dithering has the effect of improving the local linearity within the ADC transfer function. The AD9652 allows dither to be added to either ADC input independently. The full scale of the dither DAC is small enough that enabling dither does not limit the external input signal amplitude.

As shown in Figure 52, the dither that is added to the input of the ADC through the dither DAC is precisely subtracted out digitally to minimize SNR degradation. When dithering is enabled, the dither DAC is driven by a pseudorandom number generator (PN gen). In the AD9652, the dither DAC is precisely calibrated to result in only a very small degradation in SNR and SINAD when dither is enabled.

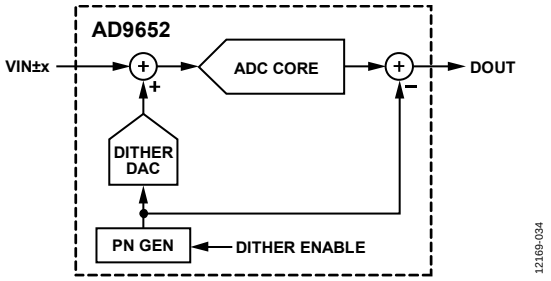

Figure 52. Dither Block Diagram

The SFDR improvement comes at the expense of SNR degradation, but because the dither is internal and can be correlated, the impact on SNR is typically limited to less than 0.5 dB in the first Nyquist zone. Enabling internal dither does not impact full-scale dynamic range. The magnitude of dither is controllable, which allows the user to select the desired trade-off between SFDR improvement vs. SNR degradation.

To enable dither, set Bit 4 of Register 0x30. To modify the dither gain, use Register 0x212[7:4].

Table 10. Dither Gain

Register 0x212[7:4] Setting	Gain Ratio	Gain (%)
0b0000 (default)	Maximum dither	100
0b0001	255/256 × max	99.6
0b0010	254/256 × max	99.2
0b0011	252/256 × max	98.4
0b0100	248/256 × max	96.8
0b0101	240/256 × max	93.75
0b0110	224/256 × max	87.5
0b0111	192/256 × max	75
0b1000	Minimum dither	50

Large Signal Fast Fourier Transform

In most cases, dithering does not improve SFDR for large signal inputs close to full scale, for example, with a −1 dBFS input. For large signal inputs, the SFDR is typically limited by front-end sampling distortion, which dithering cannot improve. However, even for such large signal inputs, dithering may be useful for certain applications because it makes the noise floor whiter. As is common in pipeline ADCs, the AD9652 contains small DNL errors caused by random component mismatches that produce spurs or tones that make the noise floor somewhat randomly colored device-to-device. Although these tones are typically at very low levels and do not limit SFDR when the ADC is quantizing large signal inputs, dithering converts these tones to noise and produces a whiter noise floor.

Small Signal FFT

For small signal inputs, the front-end sampling circuit typically contributes very little distortion, and the SFDR is likely to be limited by tones caused by DNL errors due to random component mismatches. Therefore, for small signal inputs (typically, those below −6 dBFS), dithering can significantly improve SFDR by converting these DNL tones to white noise.

Static Linearity

Dithering also removes sharp local discontinuities in the INL transfer function of the ADC and reduces the overall peak-to-peak INL.

Utilizing dither randomizes local small signal DNL errors that produce the discontinuities in the INL transfer function and therefore improve the peak-to-peak INL performance.

Differential Input Configurations

Optimum performance is achieved by driving the AD9652 in a differential input configuration. For baseband applications, the ADL5566, AD8138, ADA4937-2, ADA4938-2, and ADA4930-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-2 is easily set with the VCM pin of the AD9652 (see Figure 53), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

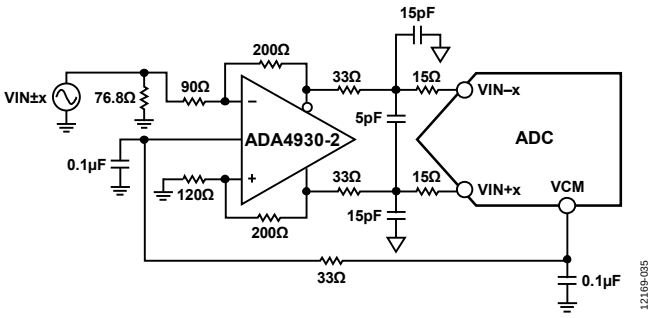

Figure 53. Differential Input Configuration Using the ADA4930-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input

configuration. An example is shown in Figure 54. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

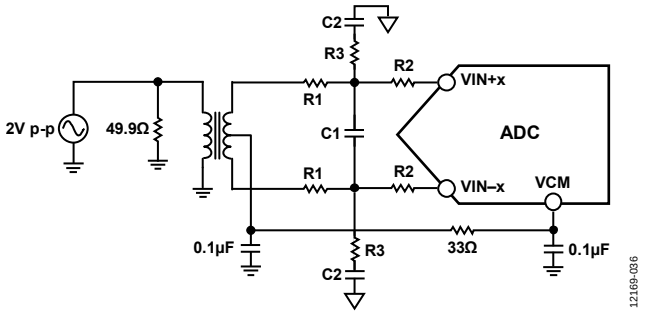

Figure 54. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9652. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 56). In this configuration, the input is ac-coupled and the VCM voltage is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted, or some components may need to be removed. Table 11 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal; use the bandwidth only as a starting guide. Note that the values given in Table 11 are for each R1, R2, C1, C2, and R3 component shown in Figure 54 and Figure 56.

Table 11. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	Open	0	15	49.9
100 to 300	15	Open	15	2.7	0

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 or AD8376 digital variable gain amplifier (DVGA) provides good performance for driving the AD9652. Figure 55 shows an example of the AD8376 driving the AD9652 through a band-pass antialiasing filter.

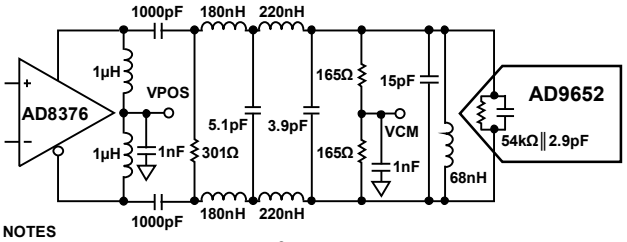

Figure 55. Differential Input Configuration Using the AD8376

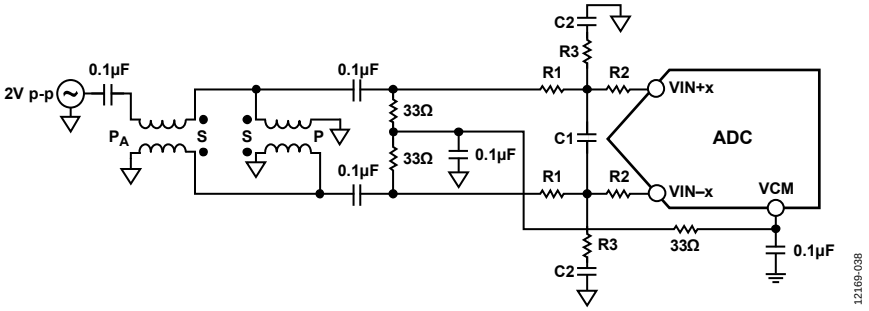

Figure 56. Differential Double Balun Input Configuration

Table 12. V_{REF} Configuration Options

Selected Mode	SENSE Voltage	Resulting ADC Reference Voltage (V)	Resulting Input Span (Differential V p-p)
External Reference	AVDD	N/A[1]	2 × external reference
Internal Fixed Reference	GND	V_{REF}[2]	2 × V_{REF}[2]

[1] N/A = not applicable.
[2] V_{REF} is set via Register 0x18. The default V_{REF} is 1.25 V.

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9652. The full-scale input range can be adjusted by varying the reference voltage via the SPI. The input span of the ADC linearly tracks reference voltage changes.

Internal Reference Connection

A stable and accurate programmable reference is built into the AD9652, allowing a voltage reference from 1.0 V to 1.25 V to provide up to a 2.5 V p-p differential full-scale input. By default the V_{REF} voltage is set 1.25 V, but can be modified using Register 0x18[2:0], V_{REF} select.

To configure the AD9652 for an internal reference, the SENSE pin must be tied low. When SENSE is tied low, the ADC uses V_{REF} directly and provides a differential input voltage of two times the V_{REF} value.

To achieve optimal noise performance when using the internal reference, it is recommended that the VREF pin be decoupled by 1.0 µF and 0.1 µF capacitors close to the pin. Figure 57 shows the configuration for the internal reference connection resulting in a input voltage set by VREF, that is, a 2.5 V p-p differential full-scale input.

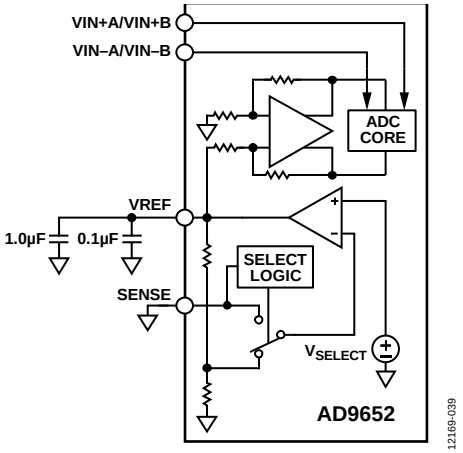

Figure 57. Internal Reference Configuration

If the internal reference of the AD9652 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 58 shows how the internal reference voltage is affected by loading.

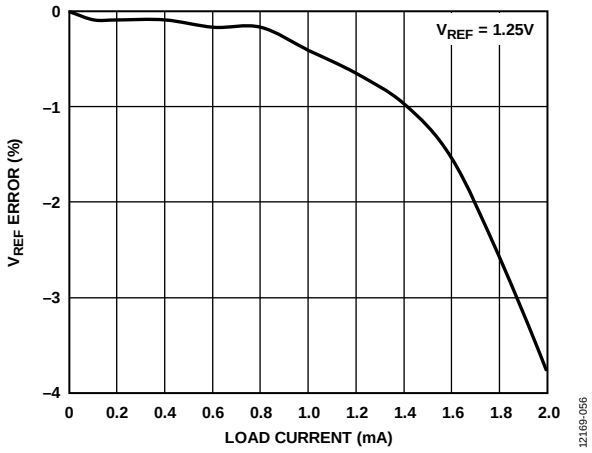

Figure 58. Reference Voltage Error vs. Load Current

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics.

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference that is applied to the VREF pin. An internal reference buffer loads the external reference with an equivalent 6 kΩ load. The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.25 V to maintain an input voltage of 2.5 V p-p differential full-scale input or less.

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9652 sample clock inputs, CLK+ and CLK–, with a differential signal with a high slew rate. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or via capacitors. These pins are biased internally (see Figure 59) and require no external bias. If the inputs are floated, the CLK– pin is intentionally biased slightly lower than CLK+ to prevent spurious clocking (this is not shown in Figure 59).

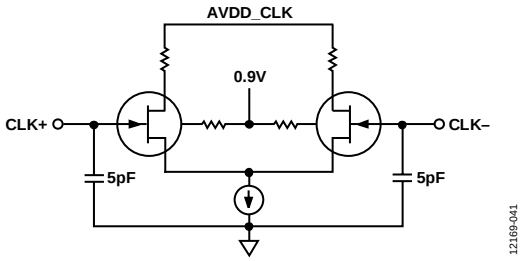

Figure 59. Simplified Equivalent Clock Input Circuit

Clock Input Options

The AD9652 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section.

Figure 60 and Figure 61 show two preferable methods for clocking the AD9652 (at clock rates of up to 1240 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using an RF balun or RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1240 MHz, and the RF transformer is recommended for clock frequencies from 80 MHz to 200 MHz. The back-to-back Schottky diodes are used across the transformer secondary or the balun balanced side to limit clock amplitude excursions into the AD9652 to approximately 0.8 V p-p differential. This limit helps prevent large voltage swings of the clock from feeding through to other portions of the AD9652, while preserving fast rise and fall times of the clock, which are critical to low jitter performance.

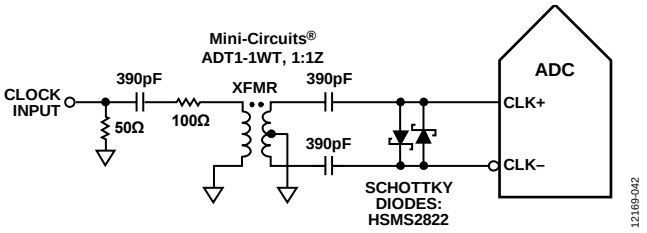

Figure 60. Transformer-Coupled Differential Clock (Up to 200 MHz)

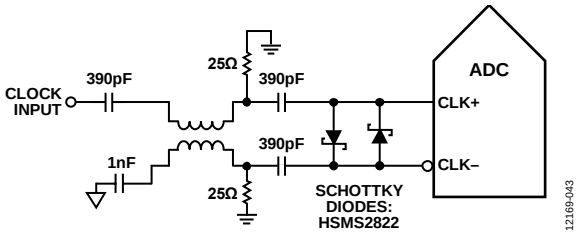

Figure 61. Balun-Coupled Differential Clock (Up to 1240 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins as shown in Figure 62. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, AD9524, and ADCLK905/ADCLK907/ ADCLK925 clock drivers offer excellent jitter performance.

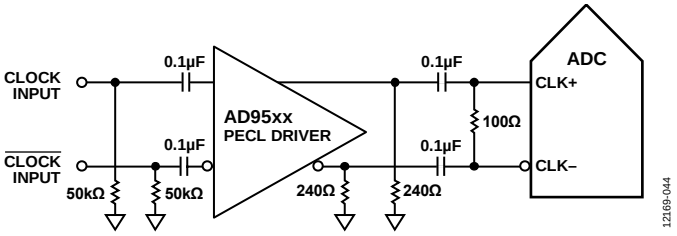

Figure 62. Differential PECL Sample Clock (Up to 1240 MHz)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 63. The AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, and AD9524 clock drivers offer excellent jitter performance.

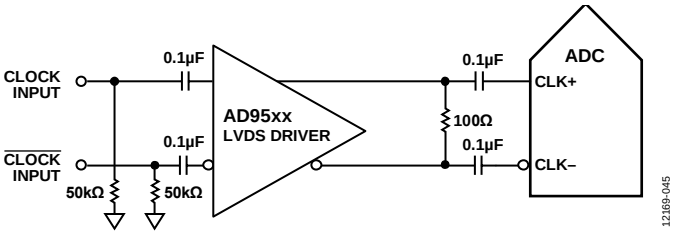

Figure 63. Differential LVDS Sample Clock (Up to 625 MHz)

Input Clock Divider

The AD9652 contains an input clock divider with the ability to divide the input clock by integer values of 1, 2, 4 or 8. In these cases, the DCS is enabled by default on power-up. The clock divide ratio is set in Register 0x0B.

The AD9652 clock divider can be synchronized using the external SYNC input. Bit 1 and Bit 2 of Register 0x100 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling. With the divider enabled and the SYNC option used, the ADC clock divider output phase can be adjusted after synchronization in increments of input clock cycles using Register 0x16.

Drive the SYNC input using a single-ended CMOS type signal. If not used, connect the SYNC pin to ground.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9652 contains a clock DCS that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9652.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the duty cycle stabilizer. The DCS control loop does not function for clock rates less than 80 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate changes dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input clock. During that time period, the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock

signal. In some cases, it may be appropriate to disable the duty cycle stabilizer, for example, if a high quality RF clock is available to be used to drive the AD9652 clock input and does not need adjustment in duty cycle correction. In most other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which includes the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 64.

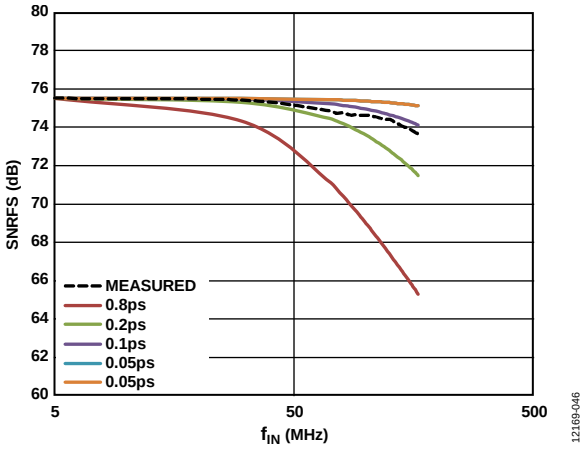

Figure 64. SNRFS vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9652.

Drive external clock sources and buffers from a clean ADC output driver supply to avoid modulating the ADC clock with noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), retime it by the original clock at the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 65, the power dissipated by the AD9652 is proportional to its sample rate. The data in Figure 65 was taken using the same operating conditions as those used for the Typical Performance Characteristics section.

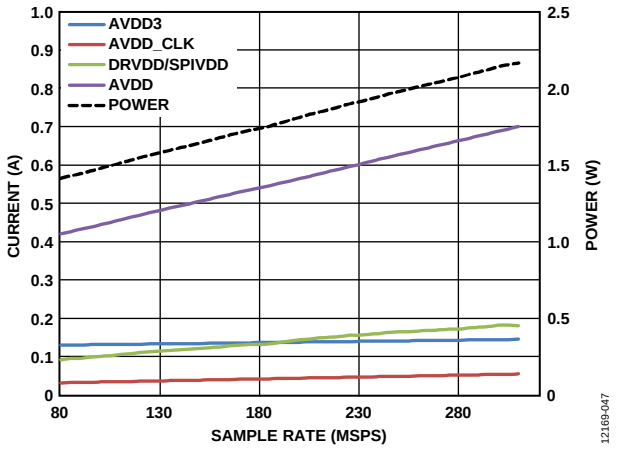

Figure 65. Power and Current vs. Sample Rate

By asserting power-down (either through setting Register 0x08 or by asserting the PDWN pin high), the AD9652 is placed in power-down mode. In this state, the ADC typically dissipates less than 1 mW. During power-down, the output drivers are placed in a high impedance state. Deasserting the PDWN pin (forcing it low) returns the AD9652 to its normal operating mode. Note that the level on PDWN is referenced to the digital output driver supply (DRVDD) and cannot exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional details.

INTERNAL BACKGROUND CALIBRATION

The AD9652 uses a background calibration to continually correct errors between internal analog circuits to maintain the high level of noise performance over varying conditions. The calibration correction digitally monitors the errors in the various analog blocks, calculates the error, and applies corrections. The background correction is calculated every 3×2^{33} samples; therefore, when running at 310 MSPS, the update rate is about 83 seconds. Each calibration cycle is independent from previous calibrations to improve tracking. There are no requirements on the input signal for the background calibration.

The calibration occurs independently for each ADC path. The background calibration continually operates but does not update if the input signal is significantly out of range (beyond the OTR) because this can cause errors in the calibration calculation. The calibration engine monitors any errors and

resets the calibration cycle if the input signal exceeds the input range for 1000 samples within a single calibration cycle.

At startup, when the AD9652 is first powered and a valid clock is applied, a fast start-up background calibration is performed and converges 64 times faster than the normal calibration cycle. At 310 MSPS, the fast start-up calibration updates after 1.3 seconds. The fast start-up calibration allows the AD9652 to be used sooner than waiting for a full calibration cycle and typically degrades SNR performance by less than 0.5 dB. This degradation lasts until a full calibration cycle completes.

In cases where configuration of the AD9652 changes and a recalibration is needed, a fast start-up calibration can be initiated by an SPI register write or by asserting and deasserting the PDWN pin.

To initiate using the SPI register, use Register 0x08[1:0]. To start a new fast calibration, put either or both ADC channels in standby and then return them to normal operation mode by writing 0x2 and then 0x0 to Register 0x08[1:0]. After returning to normal operation mode, the fast calibration is initiated one time followed by the normal, full calibration cycle. In addition to standby, this is also the case for power-down. Writing a 0x1 followed by a 0x0 initiates a fast calibration. Alternatively, a fast start-up calibration can be initiated by writing 0x0C and then 0x08 to Register 0x4FB.

The PDWN pin can be configured to put the device in power-down or standby mode based on the setting in Register 0x08[1:0]. Transitioning from either power-down or standby into normal mode causes a fast calibration to be initiated. Configuration changes that require a new calibration include, but are not limited to, changes of setting for VREF, dither enable/disable, clock input changes, and DCS state changes.

There are various advanced configuration options associated with the background calibration for applications that require special treatment. The options include an optional recovery mode for standby and a pausing background calibration.

If standby is used in an application, by default, the AD9652 keeps the current corrections, but initiates a new fast calibration when returning to normal operation mode. For standby, if conditions have not significantly changed, the AD9652 can be configured to retain the last correction coefficients by writing 0x00 to Register 0x4FA before entering the standby mode. This returns the device to the same operation as when it entered standby, retaining previous calibration values in standby mode and continuing the normal calibration cycle when returned to normal operation mode.

Although this is not recommended, in some instances such as when all the environmental, clocking, and input signals are very stable, the calibration can be paused. Pausing the background calibration causes a slight degradation in performance, but can be accomplished by writing 0x1 to Register 0x4FB, Bit 0. To re-enable the background calibration, write 0x0 to Register 0x4FB, Bit 0. Note: Register 0x4FB has reserved bits that must be preserved when accessing that and similar registers.

DIGITAL OUTPUTS

The AD9652 output drivers are for standard ANSI LVDS, but optionally the drive current can be reduced using Register 0x15. The reduced drive current for the LVDS outputs potentially reduce the digitally induced noise.

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

The AD9652 has a flexible three-state ability for the digital output pins. The three-state mode is enabled when the device is set for power-down mode.

Timing

The AD9652 provides latched data with a pipeline delay of 26 input sample clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines and the corresponding loads to reduce transients within the AD9652. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD9652 is 80 MSPS. At clock rates below 80 MSPS, dynamic performance may degrade.

Data Clock Output

The AD9652 also provides a data clock output (DCO) intended for capturing the data in an external register. Figure 2 shows a timing diagram of the AD9652 output modes. The DCO relative to the data output can be adjusted using Register 0x17. There are 32 delay settings with approximately 81 ps per step. Data is output in a DDR format and is aligned to the rising and falling edges of the clock derived from DCO±.

ADC OVERRANGE

The ADC overrange (OR) indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 26 ADC clocks. An overrange at the input is indicated by this bit, 26 clock cycles after it occurs.

Table 13. Output Data Format

Differential Input Voltage (V): (VIN+x) – (VIN–x) Input Span = 2.5 V p-p (V)	Offset Binary Output Mode	Twos Complement Mode (Default)	OR± Pin Logic Level
<–1.25	00 0000 0000 0000	10 0000 0000 0000	1
–1.25	00 0000 0000 0000	10 0000 0000 0000	0
0	10 0000 0000 0000	00 0000 0000 0000	0
+1.25	11 1111 1111 1111	01 1111 1111 1111	0
>+1.25	11 1111 1111 1111	01 1111 1111 1111	1

FAST THRESHOLD DETECTION (FDA/FDB)

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overflow indicator on the OR± pins provide delayed information, which is synchronized with the output data. The delayed indicator is of limited value in preventing clipping in this case. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce external gain before the clip occurs. In addition, because input signals can have significant slew rates, latency of this function is of concern.

Using the SPI port, the user can provide a threshold above which the fast detect (FD) output is active. Bit 0 of Register 0x45 enables the FD feature. Register 0x47 to Register 0x4C allow the user to set the threshold levels and timing. As long as the signal is below the selected threshold, the FD output remains low. In this mode, the magnitude of the data is considered in the calculation of the condition, but the sign of the data (either positive or negative) is not considered. The threshold detection responds identically to positive and negative signals outside the desired range (magnitude).

The fast detect indicators, FDA for Channel A and FDB for Channel B, are asserted when the input magnitude exceeds the value programmed in the fast detect upper threshold register, Register 0x47. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of seven clock cycles. The approximate upper threshold is a 4-bit value defined by

Upper Threshold (% *Full Scale*) =
((*Register 0x47 value*)/8) × 100%

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, Register 0x49 and Register 0x4A. The fast detect lower threshold register is a 15-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency but is accurate in terms of converter resolution. The lower threshold is defined by

Lower Threshold (% *Full Scale*) =
((*Register 0x49*/*Register 0x4A value*)/32767) × 100%

For example, to set an upper threshold of 50% full scale, write 0x04 to Register 0x47, and to set a lower threshold of 40% full scale, write 0x3333 to Register 0x49 and Register 0x4A.

The dwell time can be programmed from 1 sample clock cycle to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, Register 0x4B and Register 0x4C (see Figure 66).

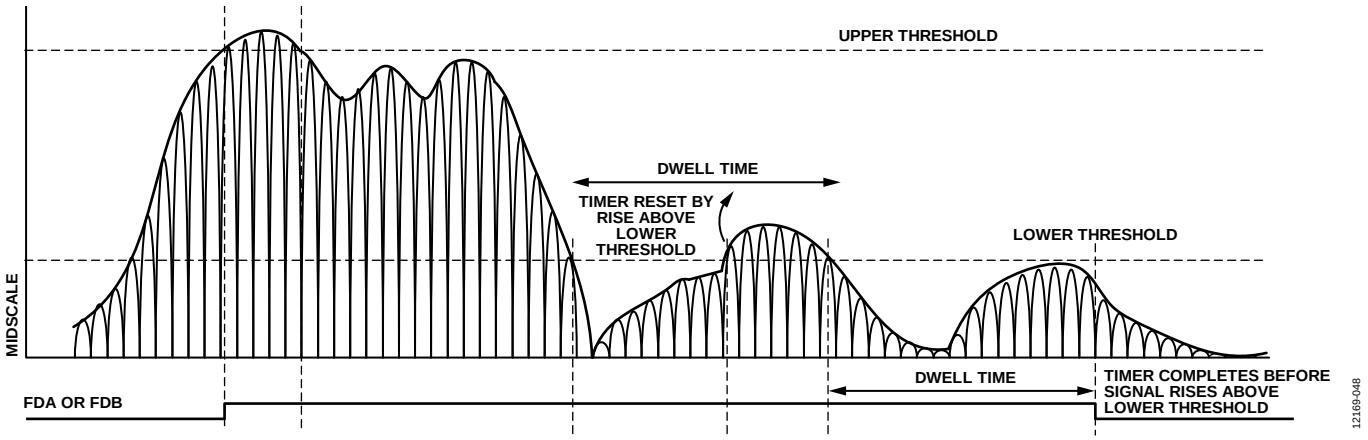

Figure 66. Threshold Settings for FDA and FDB Signals

SERIAL PORT INTERFACE

The AD9652 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 14). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 14. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles. Must be pulled to logic high during power up.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Table 5 and Figure 4.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB pin can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and the W1 bits.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO/DCS) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note.

HARDWARE INTERFACE

The pins described in Table 14 comprise the physical interface between the user programming device and the serial port of the AD9652. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either field-programmable grid arrays (FPGAs) or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port must not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9652 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO pin and the SCLK pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the DCS and output data format feature control. In this mode, connect CSB to AVDD, which disables the serial port interface.

Table 15. Mode Selection

Pin	External Voltage	Configuration
SDIO	AVDD (default)	DCS enabled
	AGND	DCS disabled
SCLK	AVDD	Twos complement enabled
	AGND (default)	Offset binary enabled

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note.

Table 16. Features Accessible Using the SPI

Feature Name	Description
Power Modes	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS via the SPI
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the delay of the clock derived from DCO±
VREF	Allows the user to set the reference voltage

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the channel index and transfer registers (Address 0x05 and Address 0xFF); and the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x4FB).

The memory map register table (see Table 17) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x09, the global clock register, has a hexadecimal default value of 0x01. This means that the LSB or Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on the functions controlled by Register 0x00 to Register 0x17, see the AN-877 Application Note. This application note also details the functions controlled by all remaining registers.

Open and Reserved Locations

All address and bit locations that are not included in Table 17 are not currently supported for this device. Unused bits of a valid address location must be written with 0s, unless otherwise noted. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open/unused/undocumented (for example, Address 0x13), this address location must not be written.

Default Values

After the AD9652 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 17.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

The 0x08, 0x09, 0x0B, 0x0D, 0x0F, 0x10, 0x14, 0x16, 0x17, and 0x30 registers are shadowed. Writes to these addresses do not affect device operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update occurs when the transfer bit is set, and then the bit autoclears.

Channel Specific Registers

Some channel setup functions, such as the signal monitor thresholds, can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 17 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x05. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, only Channel A or Channel B are set to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. Registers and bits designated as global in Table 17 affect the entire device and the channel features for which independent settings are not allowed. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 17 are not currently supported for this device.

Table 17. Memory Map Registers

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
0x00	SPI port configuration (global)[1]	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	The nibbles are mirrored so that LSB first mode or MSB first mode registers correctly, regardless of shift mode
0x01	Chip ID (global)	8-Bit Chip ID[7:0], (AD9652 = 0xC1) (default)								0xC1	Read only
0x02	Chip grade (global)			Speed grade ID, 0x00: default						0x00	Speed grade ID used to differentiate devices; read only
Channel Index and Transfer Registers											
0x05	Channel index (global)							Channel B (default)	Channel A (default)	0x03	Bits are set to determine which device on the chip receives the next write command; applies to local registers only
0xFF	Transfer (global)								Transfer	0x00	Synchronously transfers data from the master shift register to the slave
ADC Functions											
0x08	Power modes (local)	Reserved, set to 1		External power-down pin function (local) 0 = power-down 1 = standby				Internal power-down mode (local) 00 = normal operation 01 = full power-down 10 = standby 11 = reserved		0x80	Controls power-down options
0x09	Global clock (global)								Enable DCS (default)	0x01	

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x0B	Clock divide (global)						Clock divide ratio 000 = divide by 1 001 = divide by 2 010 = reserved, do not use 011 = divide by 4 100 = divide by 8			0x00	
0x0D	Test mode (local)			Reset PN23 long gen PN23: $1 + x^{17} + x^{22}$	Reset PN9 short gen PN9: $1 + x^3 + x^8$	Output test mode 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN23 long sequence 0110 = PN9 short sequence 0111 = one/zero word toggle				0x00	When this register is set, the test data is placed on the output pins (D0± to D15±) in place of normal data
0x0F	Common-mode servo (global)								Enable common-mode servo	0x00	
0x10	Offset adjust (local)	Offset adjust in LSBs from +127 (0111 1111) to −128 (1000 0000) (twos complement format)								0x00	
0x14	Output mode (local)							Output format 00 = offset binary (default) 01 = twos complement 10 = gray code 11 = reserved		0x00	Configures the outputs and the format of the data
0x15	Output LVDS control (global)						LVDS output drive current adjust 000 = 3.72 mA (ANSI-LVDS, default) 001 = 3.50 mA 010 = 3.30 mA 011 = 2.96 mA 100 = 2.82 mA 101 = 2.57 mA 110 = 2.27 mA 111 = 2.00 mA (reduced swing LVDS)			0x00	
0x16	Clock phase adjust (global)						Input clock divider phase adjust 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycle 011 = 3 input clock cycle 100 = 4 input clock cycle 101 = 5 input clock cycle 110 = 6 input clock cycle 111 = 7 input clock cycle			0x00	
0x17	DCO± output delay (global)				DCO± clock delay (Delay = (2500 ps × register value/31)) 00000 = 0 ps 00001 = 81 ps 00010 = 161 ps … 11110 = 2419 ps 11111 = 2500 ps					0x00	
0x18	Input span select (global)	Reserved, set to 1	Reserved, set to 1				V_{REF} select 000 = 1.25 V (2.5 V p-p input), default 001 = 1.125 V (2.25 V p-p input) 010 = 1.20 V (2.4 V p-p input) 011 = 1.25 V (2.5 V p-p input) 100 = do not use 101 = 1.0 V (2.0 V p-p input)			0xC0	
0x30	Dither (local)				Dither enable					0x00	

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x45	Fast detect (FD) control								Enable fast detect output	0x00	
0x47	FD upper threshold	Fast Detect Upper Threshold[3:0] Valid programming range = 0x1 to 0x8 Threshold = midscale ± (register value) × (1/8) × (full scale)								0x08	
0x49	FD lower threshold	Fast Detect Lower Threshold[7:0]								0x00	
0x4A	FD lower threshold		Fast Detect Lower Threshold[14:8]							0x02	
0x4B	FD dwell time	Fast Detect Dwell Time[7:0]								0x00	
0x4C	FD dwell time	Fast Detect Dwell Time[15:8]								0x08	
0x100	SYNC control (global)						Clock divider next SYNC only	Clock divider SYNC enable	Master SYNC buffer enable	0x00	
0x212	Dither gain (global)	0b0000: 100% dither applied 0b0001: 99.6% dither applied 0b0010: 99.2% dither applied 0b0011: 98.4% dither applied 0b0100: 96.8% dither applied 0b0101: 93.75% dither applied 0b0110: 87.5% dither applied 0b0111: 75% dither applied 0b1000: 50% dither applied				Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	0x08	
0x22A	Input frequency settings (global)							0: f_{IN} in 1st Nyquist 1: f_{IN} in 2nd Nyquist 2: f_{IN} in 3rd Nyquist or higher		0x00	
0x4FA	Calibration power-down config-uration (global)	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Power down/standby initial calibration action: 0b00: use previous calibration correction 0b11: initiate a fast calibration		0x03	
0x4FB	Calibration power-down configura-tion (global)	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Reserved, set to 0	Reserved, set to 1	Reset back-ground calibration, set high then low	Reserved, set to 0	Pause back-ground calibration	0x08	

[1] Set the channel index register at Address 0x05 to 0x03 (default) when writing to Address 0x00.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting system level design and layout of the AD9652, it is recommended that the designer become familiar with these guidelines, which describes the special circuit connections and layout requirements needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD9652, it is recommended that three separate power supplies be used. AVDD3 requires a 3.3 V supply, AVDD_CLK and AVDD require a 1.8 V supply, and DRVDD requires a 1.8 V supply. SPIVDD is typically connected to the same supply as DRVDD, but can be connected to a separate supply between 1.8 V and 3.3 V to ease the interface to the logic device that connects to the SPI pins (CLK, SDIO, and CSB).

The AVDD3 supply must be supplied from a clean 3.3 V power source. Decoupling must be a combination of PCB plane capacitance and decoupling capacitors to cover both high and low frequency noise sources. Typical capacitors of 0.1 µF and 1 µF near the AD9652 AVDD3 pins are advised.

The AVDD and AVDD_CLK supply connection must be powered up simultaneously to achieve proper on-chip biasing; therefore, it is recommended to connect the two supply voltages to a single source. Similar to the AVDD3 supply, decoupling must be a combination of PCB plane capacitance and decoupling capacitors to cover both high and low frequency noise sources. Typical capacitors of 0.1 µF and 1 µF near the AD9652 AVDD and AVDD_CLK pins is advised.

The DRVDD and SPIVDD supply connection must also have decoupling but these can be placed slightly further away from the AD9652. DRVDD and SPIVDD can be tied together for applications that can use a 1.8 V SPI interface logic. Optionally, SPIVDD can be driven with a supply of up to 3.3 V to support higher voltage logic interfaces.

Multiple large area PCB ground planes are recommended and provide many benefits. Low impedance power and ground planes are needed to maintain performance. Stacking power and ground planes in the PCB provides high frequency decoupling. Ground planes and thermal vias help dissipate heat generated by the device. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

VCM

The VCM pin must be decoupled to ground with a 0.1 µF capacitor, as shown in Figure 54. For optimal channel-to-channel isolation, a 33 Ω resistor must be included between the AD9652 VCM pin and the Channel A analog input network connection, as well as between the AD9652 VCM pin and the Channel B analog input network connection.

RBIAS

The AD9652 requires that a 10 kΩ resistor be placed between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and must have at least a 1% tolerance.

Reference Decoupling

Decouple the VREF pin externally to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

SPI Port

The SPI port must not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9652 to keep these signals from transitioning at the converter input pins during critical sampling periods.

OUTLINE DIMENSIONS

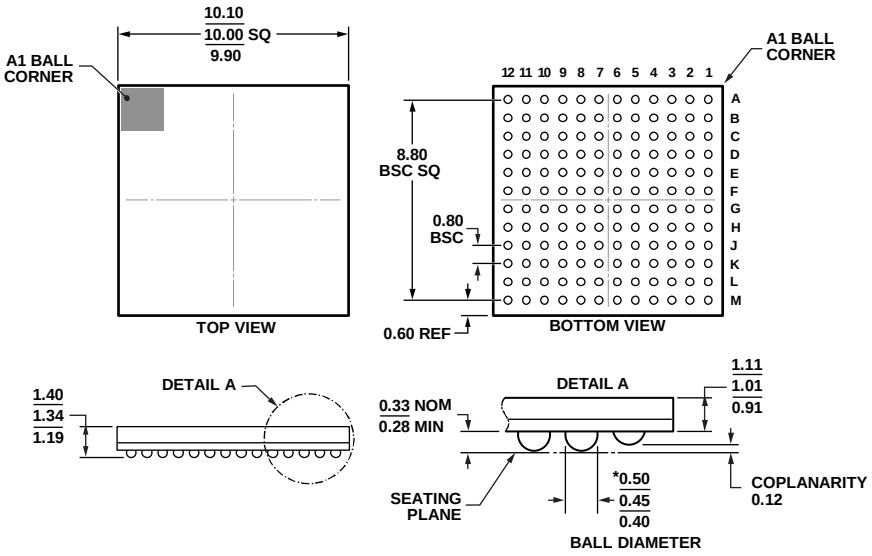

Figure 67. 144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-144-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9652BBCZ-310	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-6
AD9652BBCZRL7-310	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-6
AD9652-310EBZ	−40°C to +85°C	Evaluation Board with AD9652	

[1] Z = RoHS Compliant Part.