KSZ8081MLX / KSZ8091MLX

10Base-T/100Base-TX
Physical Layer Transceiver

Evaluation Board User's Guide

Revision 1.0 / August 2012

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Revision History

Revision	Date	Summary of Changes
1.0	8/17/2012	Initial Release

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1.0 Introduction

The KSZ8081MLX / KSZ8091MLX is a 10Base-T/100Base-TX Physical Layer Transceiver with an MII MAC interface, and Micrel LinkMD® TDR-based cable diagnostics for identification of faulty copper cabling. It utilizes a unique mixed-signal design to extend signaling distance while reducing power consumption, and offers HP Auto MDI/MDI-X for reliable detection of and correction for crossover and straight-through cables, eliminating the need to differentiate between crossover and straight-through cables.

The KSZ8091MLX has all the identical rich features of the KSZ8081MLX plus support for Energy Efficient Ethernet (EEE) and Wake-on-LAN (WOL).

The KSZ8081MLX and KSZ8091MLX Eval Boards (KSZ8081MLX-EVAL and KSZ8091MLX-EVAL) provide a convenient platform to evaluate the features of the device. All configuration pins are accessible either by jumpers, test points or interface connectors.

2.0 Board Features

- Micrel KSZ8081MLX or KSZ8091MLX 10Base-T/100Base-TX Physical Layer Transceiver
- RJ-45 Jack for Fast Ethernet cable interface
- HP Auto-MDI/MDI-X for automatic detection and correction for straight-through and crossover cables
- MII (Media Independent Interface) Connector to interface with a MAC controller
- 2 LED Indicators for status and activity
- Jumpers to configure strapping pins
- Manual Reset Button for quick reboot after re-configuration of strapping pins

3.0 Evaluation Kit Contents

The KSZ8081MLX and KSZ8091MLX Evaluation Kit includes the following hardware:

- KSZ8081MLX or KSZ8091MLX Evaluation Board

A design package with the following collaterals that can be downloaded from Micrel's website at http://www.micrel.com

- KSZ8081MLX / KSZ8091MLX Eval Board Schematic (PDF and OrCAD DSN file)
- KSZ80x1 (48-LQFP) Eval Boards Gerber Files (PDF version included)
- KSZ8081MLX / KSZ8091MLX Eval Board User's Guide (this document)
- KSZ8081MLX and KSZ8091MLX IBIS Models

and the KSZ8081MLX and KSZ8091MLX Datasheets which are also available from Micrel's website.

4.0 Hardware Description

The KSZ8081MLX-EVAL / KSZ8091MLX-EVAL (shown in Figure 1) come in a compact form factor and plugs directly into boards with Ethernet MACs that expose the MII interface. Configuration of the KSZ8081MLX / KSZ8091MLX is accomplished through on-board jumper selections and/or by PHY register access via the MDC/MDIO management pins of the MII Interface.

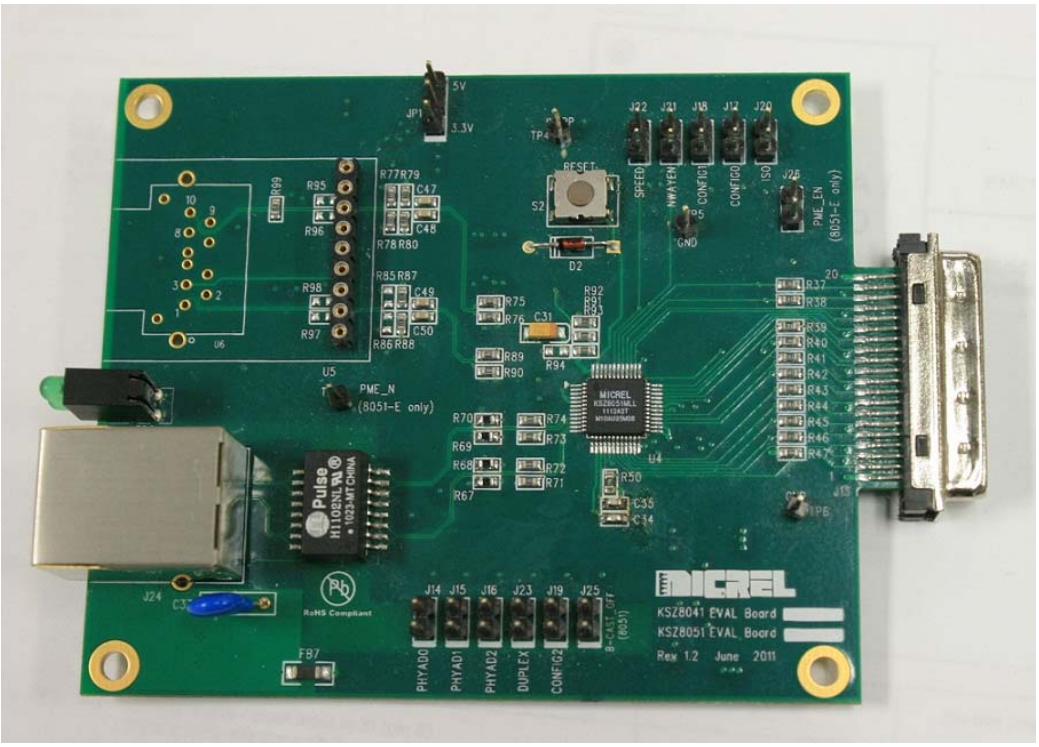

Figure 1. KSZ8081MLX Evaluation Board

Features include an RJ-45 Jack for Fast Ethernet cable connection, programmable LED indicators for reporting link status and activity, and a manual reset button for quick reboot after re-configuration of strapping pins.

The KSZ8081MLX-EVAL / KSZ8091MLX-EVAL receive +5V DC input power through its MII connector.

4.1 MII (Media Independent Interface)

The KSZ8081MLX-EVAL / KSZ8091MLX-EVAL receives power and accesses MII data and management information from the MII connector, J13. Figure 2 shows the KSZ8081MLX-EVAL connected to the Micrel KSZ8463MLI Evaluation Board.

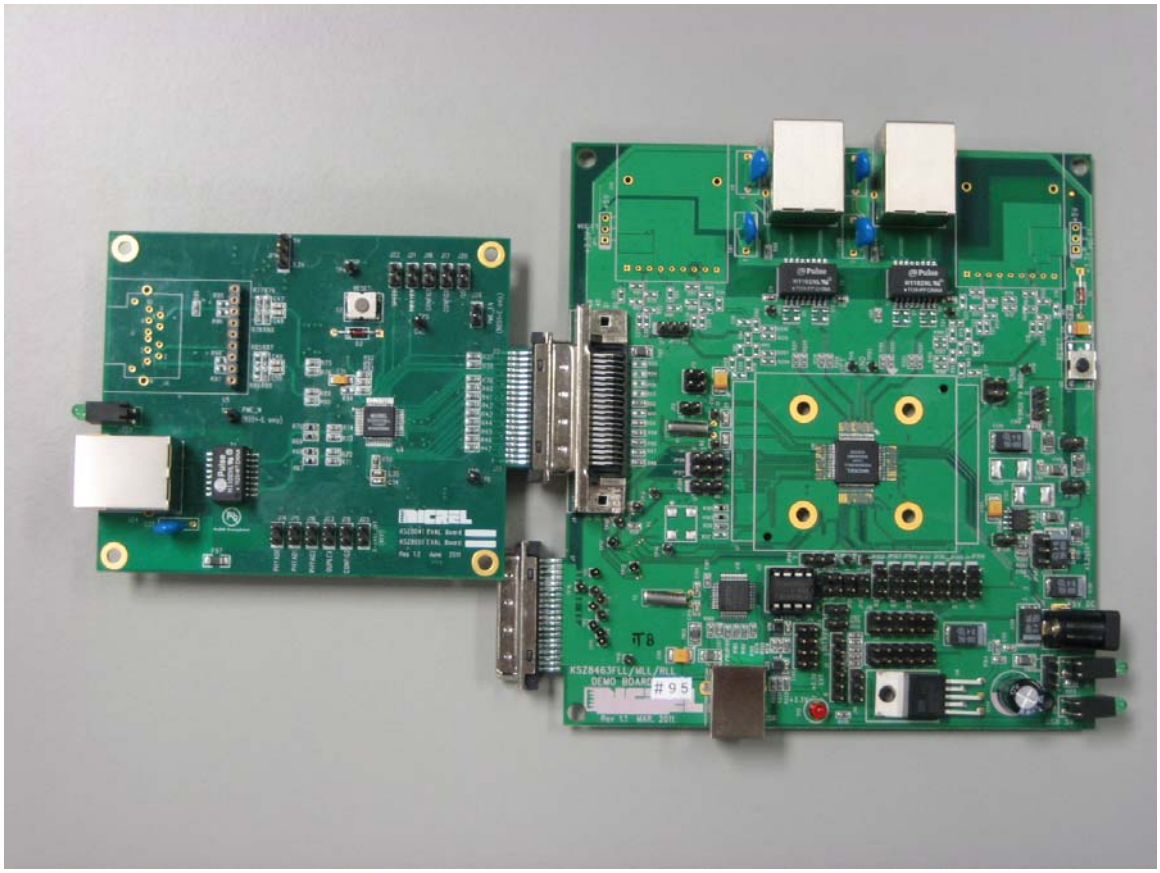

Figure 2. KSZ8081MLX-EVAL interfacing with KSZ8463MLI Evaluation Board

The MII interface is defined by Clause 22 of the IEEE 802.3 Specification. MII Management (MIIM) is conducted thru pins MDC (clock line) and MDIO (data line). MIIM allows upper-layer devices to monitor and control the states of the KSZ8081MLX / KSZ8091MLX. An external device with MDC/MDIO capability can be used to read the PHY status or configure the PHY registers. The MIIM frame format and timing information can be found in the KSZ8081MLX and KSZ8091MLX datasheets and in Clause 22 of the IEEE 802.3 Specification.

The Eval Board has a 40-pin male edge connector that interfaces with and plugs directly into Fast Ethernet MAC boards with the mating AMP 787170-4 (40-pin, right angle, female) connector. Table 1 lists the pin outs for the MII interface on connector J13.

Pin #	Signal	Pin #	Signal
1	+5V	21	+5V
2	MDIO	22	Ground
3	MDC	23	Ground
4	RXD3	24	Ground
5	RXD2	25	Ground
6	RXD1	26	Ground
7	RXD0	27	Ground
8	RXDV	28	Ground
9	RXCLK	29	Ground
10	RXER	30	Ground
11	TXER	31	Ground
12	TXCLK	32	Ground
13	TXEN	33	Ground
14	TXD0	34	Ground
15	TXD1	35	Ground
16	TXD2	36	Ground
17	TXD3	37	Ground
18	COL	38	Ground
19	CRS	39	Ground
20	+5V	40	+5V

Table 1. Connector J13 - MII Pin Definition

4.2 Jumper Setting & Definition

The KSZ8081MLX-EVAL / KSZ8091MLX-EVAL do not require any jumper for normal operation. At power-up, the KSZ8081MLX / KSZ8091MLX are configured using the chip's internal pull-up and pull-down resistors with its default strapping pin values. Jumpers are provided to override the default settings, allowing for quick configuration and re-configuration of the board. To override the default settings, simply select and close the desired jumper setting(s) and toggle the on-board manual reset button (S2) for the new setting(s) to take effect.

The KSZ8081MLX-EVAL / KSZ8091MLX-EVAL strapping jumper settings are defined in Table 2 below.

<table>
<tr><th>Jumper</th><th>Definition</th><th>Open (default)</th><th>Close</th></tr>
<tr><td>J14</td><td>PHYAD0</td><td>1</td><td>0</td></tr>
<tr><td>J15</td><td>PHYAD1</td><td>0</td><td>1</td></tr>
<tr><td>J16</td><td>PHYAD2</td><td>0</td><td>1</td></tr>
<tr><td>J17</td><td>CONFIG0</td><td colspan="2" rowspan="3"><table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>[open, open, open]</td><td>MII (default)</td></tr><tr><td>[close, close, open]</td><td>MII Back-to-Back</td></tr></table>All other CONFIG[2:0] settings not listed are reserved or not used by the KSZ8081MLX / KSZ8091MLX.</td></tr>
<tr><td>J18</td><td>CONFIG1</td></tr>
<tr><td>J19</td><td>CONFIG2</td></tr>
<tr><td>J20</td><td>Isolate Mode</td><td>Disable</td><td>Enable</td></tr>
<tr><td>J21</td><td>NWay Auto-Negotiation</td><td>Enable</td><td>Disable</td></tr>
<tr><td>J22</td><td>Forced Speed</td><td>100Base-TX</td><td>10Base-T</td></tr>
<tr><td>J23</td><td>Forced Duplex</td><td>Half</td><td>Full</td></tr>
<tr><td>J25</td><td>Broadcast Off – for PHY Address 0</td><td>Broadcast PHY address</td><td>Unique PHY address</td></tr>
<tr><td>J26</td><td>PME_N Pin Enable (KSZ8091 only)</td><td>Disable</td><td>Enable</td></tr>
</table>

Table 2. KSZ8081MLX-EVAL / KSZ8091MLX-EVAL Jumper Definition

Table 3 lists the strapping pin definitions for the KSZ8081MLX-EVAL / KSZ8091MLX-EVAL jumpers.

<table>
<tr><th>Jumper</th><th>Pin</th><th>Pin Name</th><th>Pin Function</th></tr>
<tr><td>J16
J15
J14</td><td>22
21
20</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to '00'.</td></tr>
<tr><td>J19
J18
J17</td><td>27
41
40</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:

<table><tr><td>CONFIG[2:0]</td><td>Mode</td></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>100</td><td>PCS Loopback</td></tr></table>
All other CONFIG[2:0] settings not listed are reserved or not used.</td></tr>
<tr><td>J26</td><td>33</td><td>PME_EN
(KSZ8091 only)</td><td>PME_N Output Pin for Wake-On-LAN Function
Pull-up = Enable
Pull-down (default) = Disable
At the de-assertion of reset, this pin value is latched into the chip.</td></tr>
<tr><td>J20</td><td>29</td><td>ISO</td><td>ISOLATE mode
Pull-up = Enable
Pull-down (default) = Disable
During power-up / reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>J22</td><td>43</td><td>SPEED</td><td>SPEED mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>J23</td><td>23</td><td>DUPLEX</td><td>DUPLEX mode
Pull-up (default) = Half Duplex
Pull-down = Full Duplex
During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.</td></tr>
<tr><td>J21</td><td>42</td><td>NWAYEN</td><td>Nway Auto-Negotiation Enable
Pull-up (default) = Enable Auto-Negotiation
Pull-down = Disable Auto-Negotiation
During power-up / reset, this pin value is latched into register 0h bit 12.</td></tr>
</table>

Jumper	Pin	Pin Name	Pin Function
J25	28	B-CAST_OFF	Broadcast Off – for PHY Address 0 Pull-up = PHY Address 0 is set as a unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.
N/A	32	NAND_Tree#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.

Table 3. Strapping Pin Definitions for KSZ8081MLX-EVAL / KSZ8091MLX-EVAL Jumpers

4.3 Test Point Definition

The KSZ8081MLX-EVAL / KSZ8091MLX-EVAL have four test points. They are defined in the following table.

Test Point	Definition
TP4	Pin 32 (with external pull-up) KSZ8081MLX: Interrupt KSZ8091MLX: Interrupt or PME_N2
TP5	Signal Ground
TP6	Signal Ground
TP7	Pin 42 KSZ8081MLX: LED0 KSZ8091MLX: LED0 or PME_N1

Table 4. KSZ8081MLX-EVAL / KSZ8091MLX-EVAL Test Point Definition

4.4 UTP Cable Interface

The RJ-45 Connector (J24) connects to standard CAT-5 Ethernet cable to interface with 10Base-T/100Base-TX Ethernet devices.

J24 also supports Auto-MDIX and Auto-Negotiation / Forced Modes.

The KSZ8081MLX / KSZ8091MLX do not support a fiber optic interface, so the fiber module and related components are not installed on the evaluation board.

4.5 LED Indicators

A dual LED indicator (LED2) is located next to the RJ-45 Connector. The top LED and bottom LED are connected to LED1 (pin 43) and LED0 (pin 42) of the KSZ8081MLX / KSZ8091MLX, respectively.

The two LEDs are programmable to LED mode '00' or '01' via register 1Fh bits [5:4], and are defined in the following table.

<table>
<tr><th>LED Mode</th><th>LED1 (pin 43)</th><th>LED0 (pin 42)</th></tr>
<tr><td>00</td><td>
<table>
<tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>10BT</td><td>H</td><td>OFF</td></tr>
<tr><td>100BT</td><td>L</td><td>ON</td></tr>
</table>
</td><td>
<table>
<tr><th>Link/ Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
</td></tr>
<tr><td>01</td><td>
<table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
</td><td>
<table>
<tr><th>Link</th><th>Pin State</th><th>Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>
</td></tr>
<tr><td>10</td><td>Reserved – not used</td><td>Reserved – not used</td></tr>
<tr><td>11</td><td>Reserved – not used</td><td>Reserved – not used</td></tr>
</table>

Table 5. KSZ8081MLX-EVAL / KSZ8091MLX-EVAL LED Definition

5.0 Bill of Materials

KSZ8081MLX-EVAL / KSZ8091MLX-EVAL Eval Board Revision 1.0

Item	Quantity	Reference	Description	Package
1	2	C20,C21	47uF / Tantalum	C-size
2	1	C18	2.2uF / Tantalum	B-size
3	2	C19,C32	22uF / Tantalum	B-size
4	9	C23,C24,C25,C27,C28 C30,C33,C57,C58	0.1uF	0603
5	1	C26	10uF / Tantalum	A-size
6	1	C37	1000pF / 2kV	radial lead
7	2	C34,C35	22pF	0603
8	1	D2	1N4148	DO-35 / axial lead
9	2	FB2,FB3	0 Ohm	1206
10	2	FB4,FB7	Ferrite Bead	1206
11	1	J13	Male MII Connector	
12	12	J14,J15,J16,J17,J18,J19, J20,J21,J22,J23,J25,J26	Header 2X1	thru hole / 0.1" pitch
13	1	J24	RJ-45 Jack	
14	1	LED2	LEDx2 / Green	thru hole / 0.1" pitch
15	1	R34	100K	0603
16	1	R35	10K	0603
17	9	R36,R53,R55,R56,R57, R58,R59,R102,R103	4.7K	0603
18	10	R37,R38,R39,R40,R41, R42,R43,R44,R45,R46	33	0603
19	8	C22,C29,C54,R48,R49	NC	0603
20	1	R50	6.49K	0603
21	2	R52,R54	220	0603
22	5	R47,R51,R60,R61,R62	1K	0603
23	4	R63,R64,R65,R66	75	0603
24	4	R71,R72,R73,R74	0	0603
25	1	S2	SW PUSHBUTTON	SMT
26	4	TP4,TP5,TP6,TP7	TestPoint	thru hole / 0.1" pitch
27	1	T1	Pulse H1102	
28	1	U3	MIC5216-3.3YM5	SOT-23-5
29	1	U4	KSZ8081MLX or KSZ8091MLX	48-pin TQFP
30	1	Y2	25MHz +/-50ppm	cylinder
31	5	C22,C29,C54,R48,R49	NC	0603