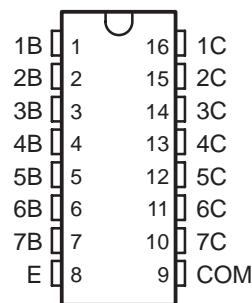


ULN2004AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SLRS055 – APRIL 2004

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

D, N, OR NS PACKAGE
(TOP VIEW)



description/ordering information

The ULN2004AI is a high-voltage, high-current Darlington transistor array. This device consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher-current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULN2004AI has a 10.5-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------|--------------|-----------------------|------------------|
| -40°C to 105°C | PDIP (N) | Tube of 25 | ULN2004AIN | ULN2004AIN |
| | SOIC (D) | Tube of 40 | ULN2004AID | ULN2004AI |
| | | Reel of 2500 | ULN2004AIDR | |
| | SOP (NS) | Reel of 2000 | ULN2004AINSR | ULN2004AI |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

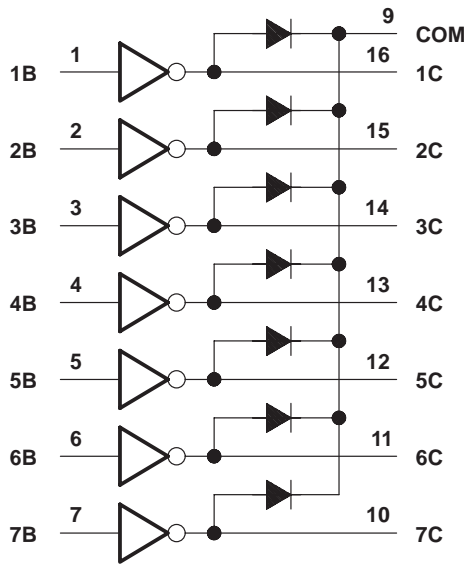
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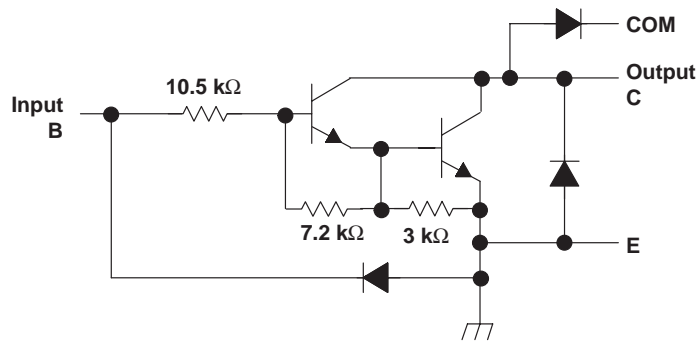
ULN2004AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SLRS055 – APRIL 2004

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

ULN2004AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SLRS055 – APRIL 2004

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

| | |
|---|----------------|
| Collector-emitter voltage | 50 V |
| Clamp diode reverse voltage (see Note 1) | 50 V |
| Input voltage, V_I (see Note 1) | 30 V |
| Peak collector current (see Notes 2 and 4) | 500 mA |
| Output clamp current, I_{OK} | 500 mA |
| Total emitter-terminal current | –2.5 A |
| Operating free-air temperature range, T_A | –40°C to 105°C |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): | |
| D package | 73°C/W |
| N package | 67°C/W |
| NS package | 64°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
 2. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

electrical characteristics, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST FIGURE | TEST CONDITIONS | MIN TYP MAX | | | UNIT |
|--|-------------|--|-----------------------|-------|---------------|------|
| | | | | | | |
| $V_{I(on)}$ On-state input voltage | 6 | $V_{CE} = 2\text{ V}$ | $I_C = 125\text{ mA}$ | | 5 | V |
| | | | $I_C = 200\text{ mA}$ | | 6 | |
| | | | $I_C = 275\text{ mA}$ | | 7 | |
| | | | $I_C = 350\text{ mA}$ | | 8 | |
| $V_{CE(sat)}$ Collector-emitter saturation voltage | 5 | $I_I = 250\ \mu\text{A}$, $I_C = 100\text{ mA}$ | 0.9 | 1.1 | V | |
| | | $I_I = 350\ \mu\text{A}$, $I_C = 200\text{ mA}$ | 1 | 1.3 | | |
| | | $I_I = 500\ \mu\text{A}$, $I_C = 350\text{ mA}$ | 1.2 | 1.6 | | |
| I_{CEX} Collector cutoff current | 1 | $V_{CE} = 50\text{ V}$, $I_I = 0$ | | 50 | μA | |
| V_F Clamp forward voltage | 8 | $I_F = 350\text{ mA}$ | | 1.7 2 | V | |
| I_I Input current | 4 | $V_I = 5\text{ V}$ | 0.35 | 0.5 | mA | |
| | | $V_I = 12\text{ V}$ | 1 | 1.45 | | |
| I_R Clamp reverse current | 7 | $V_R = 50\text{ V}$ | | 50 | μA | |
| C_i Input capacitance | | $V_I = 0$, $f = 1\text{ MHz}$ | | 15 25 | pF | |



ULN2004AI

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SLRS055 – APRIL 2004

electrical characteristics, $T_A = -40^{\circ}\text{C}$ to 105°C

| PARAMETER | | TEST FIGURE | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------|--------------------------------------|-------------|---|---------------------------------|------|------------|---------------|------|
| $V_{I(on)}$ | On-state input voltage | 6 | $V_{CE} = 2\text{ V}$ | $I_C = 125\text{ mA}$ | | | 5 | V |
| | | | | $I_C = 200\text{ mA}$ | | | 6 | |
| | | | | $I_C = 275\text{ mA}$ | | | 7 | |
| | | | | $I_C = 350\text{ mA}$ | | | 8 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | 5 | $I_I = 250\text{ }\mu\text{A}$, $I_C = 100\text{ mA}$ | | 0.9 | 1.1 | V | |
| | | | $I_I = 350\text{ }\mu\text{A}$, $I_C = 200\text{ mA}$ | | 1 | 1.3 | | |
| | | | $I_I = 500\text{ }\mu\text{A}$, $I_C = 350\text{ mA}$ | | 1.2 | 1.6 | | |
| I_{CEX} | Collector cutoff current | 1 | $V_{CE} = 50\text{ V}$, $I_I = 0$ | | | 50 | μA | |
| | | 2 | $V_{CE} = 50\text{ V}$ | $I_I = 0$ $V_I = 1\text{ V}$ | | 100 500 | | |
| V_F | Clamp forward voltage | 8 | $I_F = 350\text{ mA}$ | | 1.7 | 2 | V | |
| $I_{I(off)}$ | Off-state input current | 3 | $V_{CE} = 50\text{ V}$, $I_C = 500\text{ }\mu\text{A}$ | | 50 | 65 | μA | |
| I_I | Input current | 4 | $V_I = 5\text{ V}$ | | 0.35 | 0.5 | mA | |
| | | | $V_I = 12\text{ V}$ | | 1 | 1.45 | | |
| I_R | Clamp reverse current | 7 | $V_R = 50\text{ V}$ | | | 100 | μA | |
| C_i | Input capacitance | | $V_I = 0$, $f = 1\text{ MHz}$ | | 15 | 25 | pF | |

switching characteristics, $T_A = 25^{\circ}\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|---|------------|------|-----|---------------|
| t_{PLH} | Propagation delay time, low- to high-level output | See Figure 8 | | 0.25 | 1 | μs |
| t_{PHL} | Propagation delay time, high- to low-level output | See Figure 8 | | 0.25 | 1 | μs |
| V_{OH} | High-level output voltage after switching | $V_S = 50\text{ V}$, See Figure 9 $I_O \approx 300\text{ mA}$, | $V_S - 20$ | | | mV |

switching characteristics, $T_A = -40^{\circ}\text{C}$ to 105°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|---|-------------|-----|-----|---------------|
| t_{PLH} | Propagation delay time, low- to high-level output | See Figure 8 | | 1 | 10 | μs |
| t_{PHL} | Propagation delay time, high- to low-level output | See Figure 8 | | 1 | 10 | μs |
| V_{OH} | High-level output voltage after switching | $V_S = 50\text{ V}$, See Figure 9 $I_O \approx 300\text{ mA}$, | $V_S - 500$ | | | mV |

PARAMETER MEASUREMENT INFORMATION

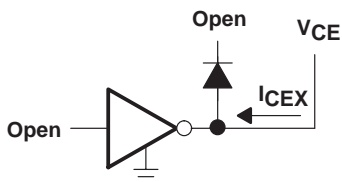


Figure 1. I_{CEX} Test Circuit

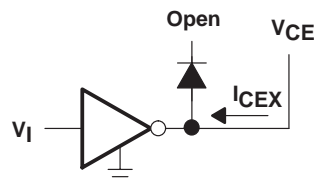


Figure 2. I_{CEX} Test Circuit

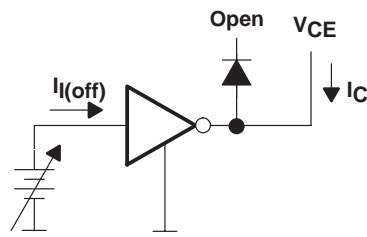


Figure 3. $I_{I(off)}$ Test Circuit

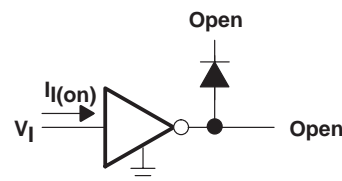
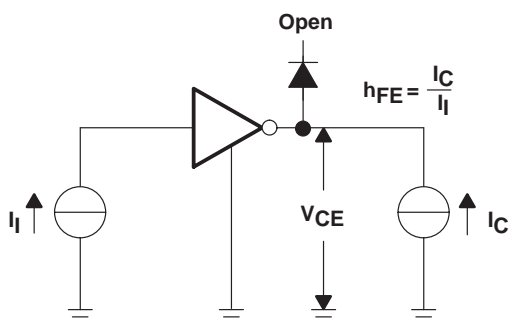


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

Figure 5. h_{FE} , $V_{CE(sat)}$ Test Circuit

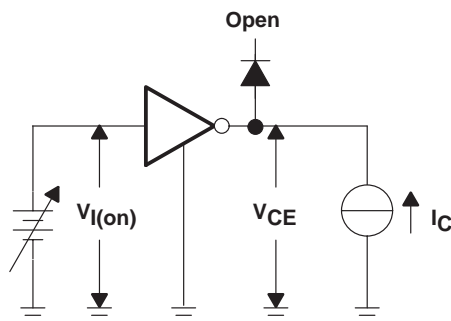


Figure 6. $V_{I(on)}$ Test Circuit

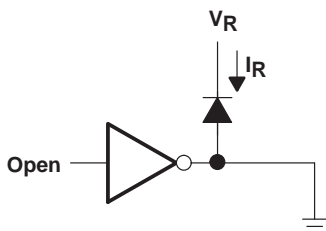


Figure 7. I_R Test Circuit

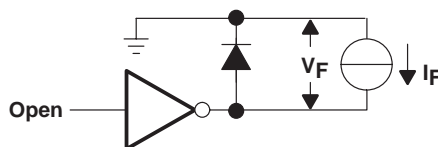


Figure 8. V_F Test Circuit

ULN2004AI
HIGH-VOLTAGE HIGH-CURRENT DARLINGTON
TRANSISTOR ARRAY

SLRS055 – APRIL 2004

PARAMETER MEASUREMENT INFORMATION

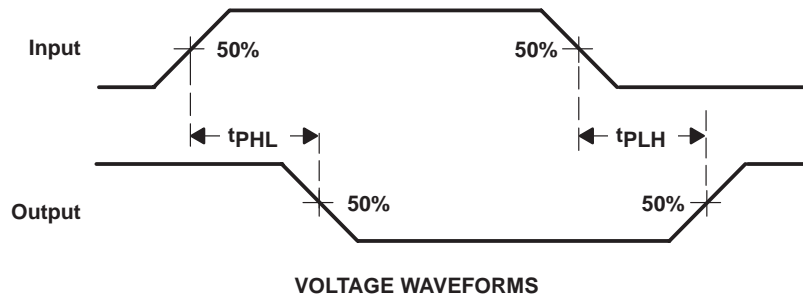
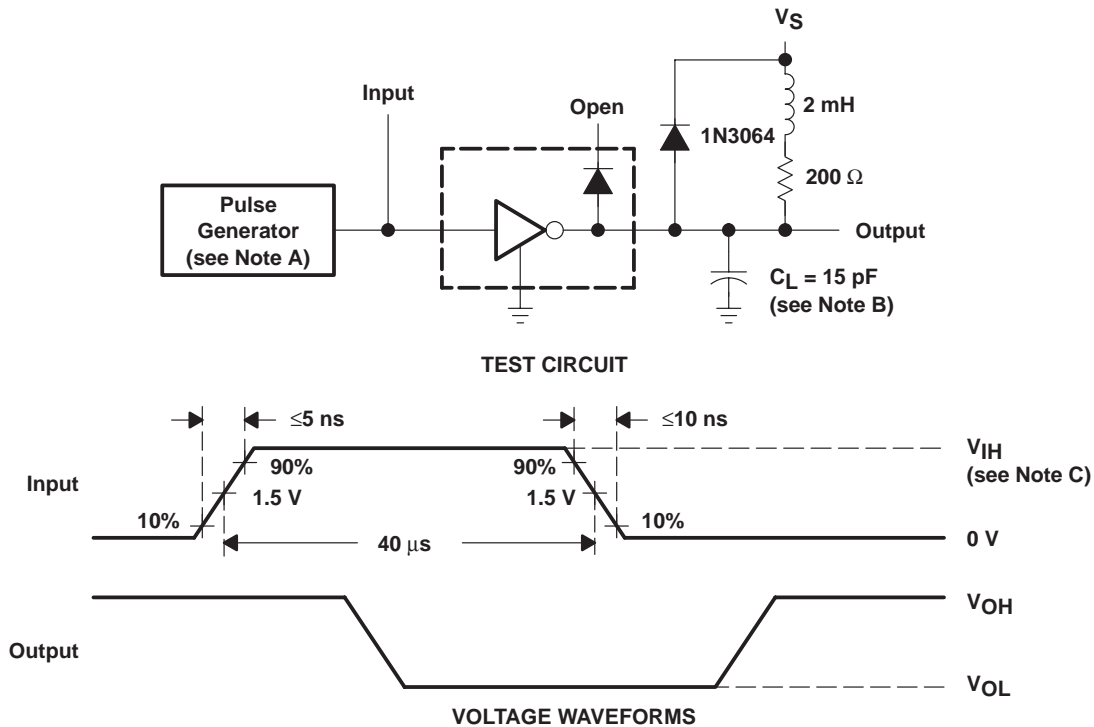


Figure 9. Propagation Delay-Time Waveforms



- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. For testing, $V_{IH} = 3 \text{ V}$

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER
 SATURATION VOLTAGE
 vs
 COLLECTOR CURRENT
 (ONE DARLINGTON)

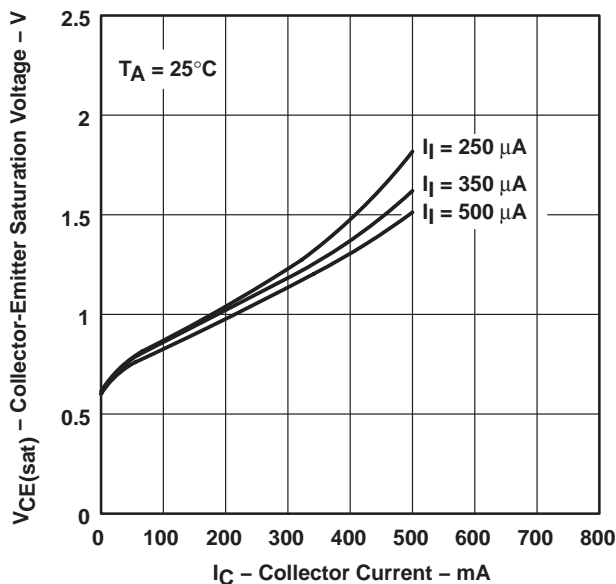


Figure 11

COLLECTOR-EMITTER
 SATURATION VOLTAGE
 vs
 TOTAL COLLECTOR CURRENT
 (TWO DARLINGTONS IN PARALLEL)

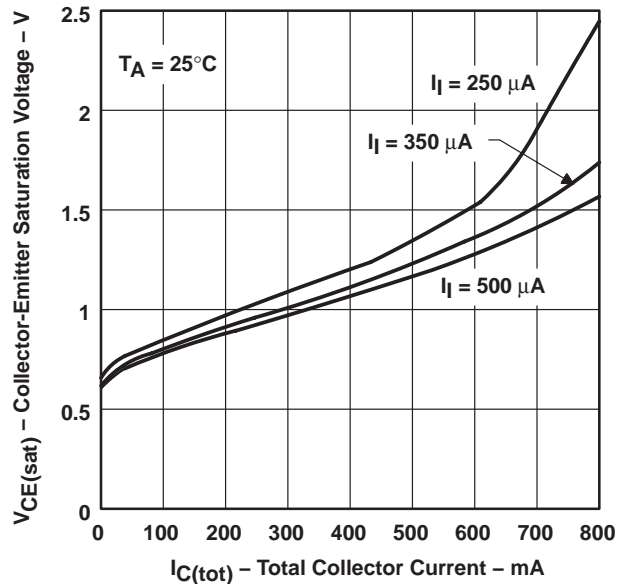


Figure 12

COLLECTOR CURRENT
 vs
 INPUT CURRENT

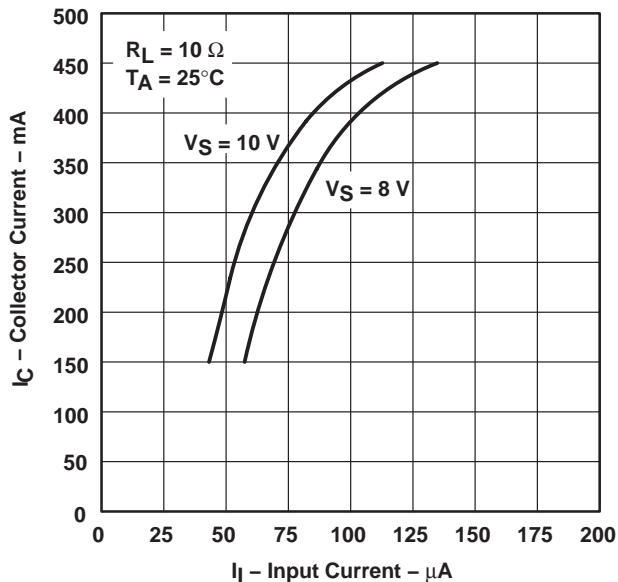


Figure 13

ULN2004AI HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SLRS055 – APRIL 2004

APPLICATION INFORMATION

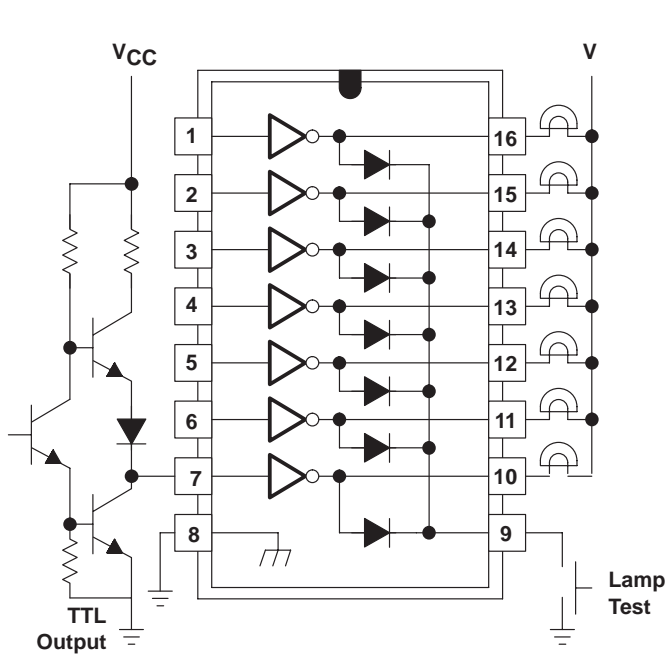


Figure 14. TTL to Load

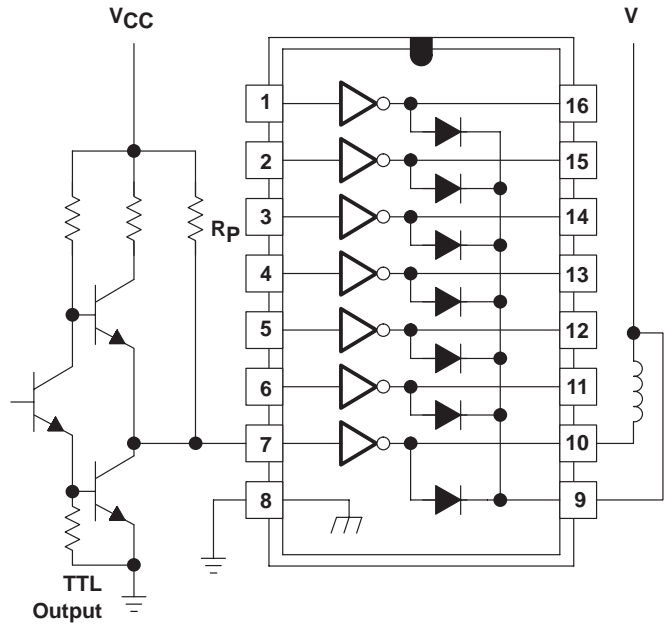


Figure 15. Use of Pullup Resistors to Increase Drive Current

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ULN2004AID | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2004AI | Samples |
| ULN2004AIDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2004AI | Samples |
| ULN2004AIDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2004AI | Samples |
| ULN2004AIN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 105 | ULN2004AIN | Samples |
| ULN2004AINSRR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2004AI | Samples |
| ULN2004AINSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2004AI | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ULN2004AIDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004AINSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ULN2004AIDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2004AINSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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