



FDZ197PZ

P-Channel 1.5 V Specified PowerTrench[®] Thin WL-CSP MOSFET -20 V, -3.8 A, 64 mΩ

Features

- Max $r_{DS(on)}$ = 64 mΩ at $V_{GS} = -4.5$ V, $I_D = -2.0$ A
- Max $r_{DS(on)}$ = 71 mΩ at $V_{GS} = -2.5$ V, $I_D = -2.0$ A
- Max $r_{DS(on)}$ = 79 mΩ at $V_{GS} = -1.8$ V, $I_D = -1.0$ A
- Max $r_{DS(on)}$ = 95 mΩ at $V_{GS} = -1.5$ V, $I_D = -1.0$ A
- Occupies only 1.5 mm² of PCB area. Less than 50% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.65 mm height when mounted to PCB
- HBM ESD protection level > 4400V (Note3)
- RoHS Compliant

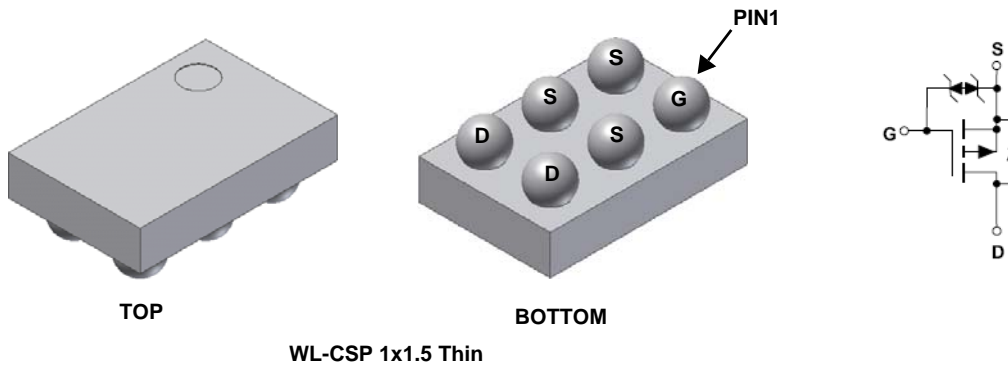


General Description

Designed on Fairchild's advanced 1.5 V PowerTrench[®] process with state of the art "fine pitch" WLCSP packaging process, the FDZ197PZ minimizes both PCB space and $r_{DS(on)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $r_{DS(on)}$.

Applications

- Battery management
- Load switch
- Battery protection



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	-3.8
	-Pulsed		-15
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	1.9
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1b)	0.9
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	65	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	133	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
7	FDZ197PZ	WL-CSP 1x1.5 Thin	7"	8 mm	5000 units

FDZ197PZ P-Channel 1.5 V Specified PowerTrench[®] Thin WL-CSP MOSFET

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-10		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\text{ }\mu\text{A}$	-0.4	-0.5	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		2.7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{ V}$, $I_D = -2.0\text{ A}$		46	64	m Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -2.0\text{ A}$		53	71	
		$V_{GS} = -1.8\text{ V}$, $I_D = -1.0\text{ A}$		59	79	
		$V_{GS} = -1.5\text{ V}$, $I_D = -1.0\text{ A}$		68	95	
		$V_{GS} = -4.5\text{ V}$, $I_D = -2.0\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		54	84	
g_{FS}	Forward Transconductance	$V_{DD} = -5\text{ V}$, $I_D = -3.8\text{ A}$		21		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		1180	1570	pF
C_{oss}	Output Capacitance			190	255	pF
C_{rss}	Reverse Transfer Capacitance			160	225	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}$, $I_D = -3.8\text{ A}$, $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		5.8	12	ns
t_r	Rise Time			5.9	12	ns
$t_{d(off)}$	Turn-Off Delay Time			311	498	ns
t_f	Fall Time			280	448	ns
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to } -4.5\text{ V}$		18	25
Q_{gs}	Gate to Source Charge	$V_{DD} = -10\text{ V}$, $I_D = -3.8\text{ A}$		1.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			4.7		nC

Drain-Source Diode Characteristics

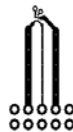
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -1.1\text{ A}$ (Note 2)		-0.6	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -3.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		194	310	ns
Q_{rr}	Reverse Recovery Charge			344	550	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $65\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper.



b. $133\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

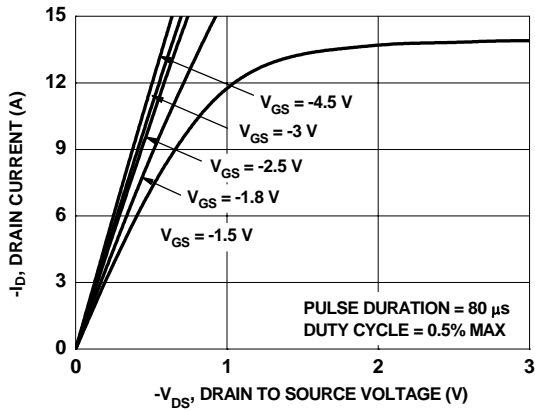


Figure 1. On-Region Characteristics

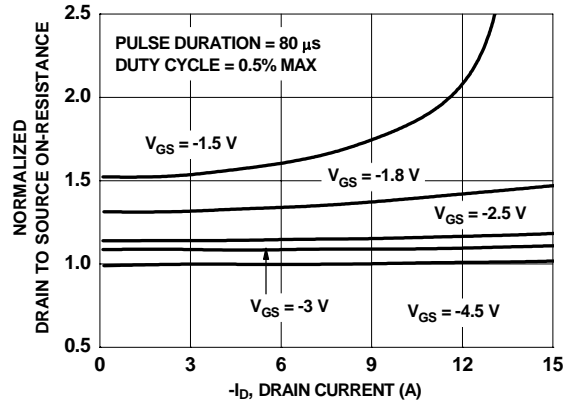


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

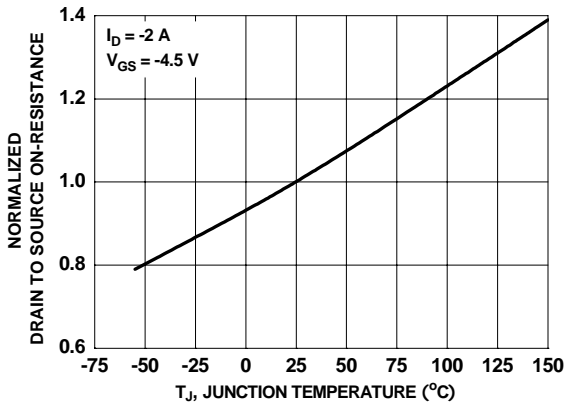


Figure 3. Normalized On-Resistance vs Junction Temperature

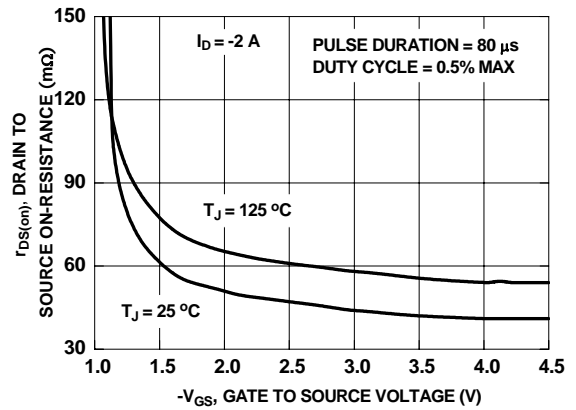


Figure 4. On-Resistance vs Gate to Source Voltage

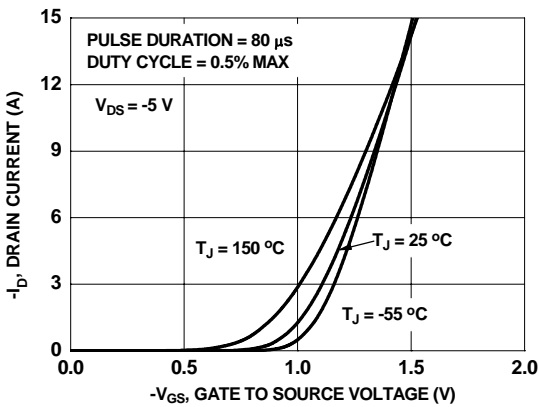


Figure 5. Transfer Characteristics

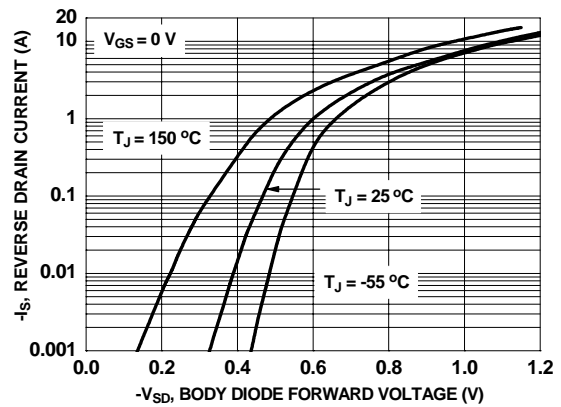


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

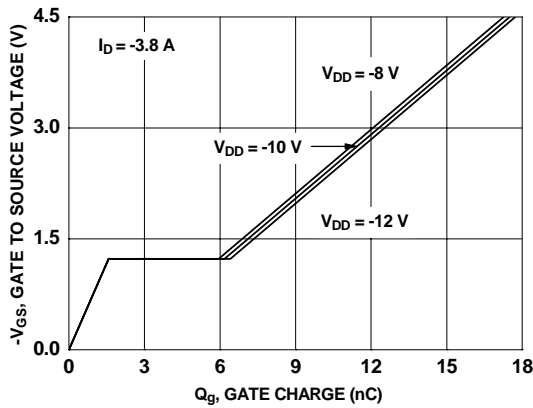


Figure 7. Gate Charge Characteristics

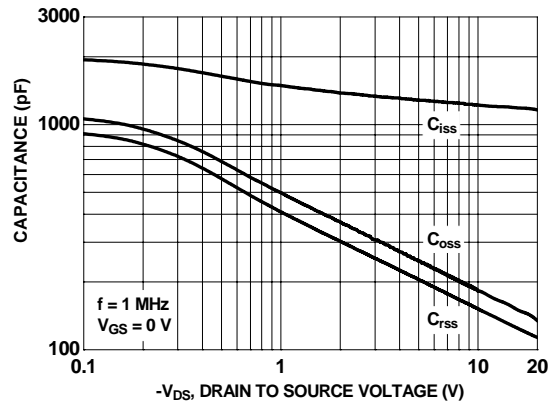


Figure 8. Capacitance vs Drain to Source Voltage

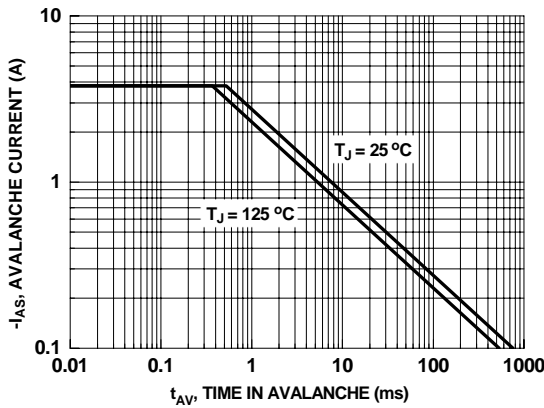


Figure 9. Unclamped Inductive Switching Capability

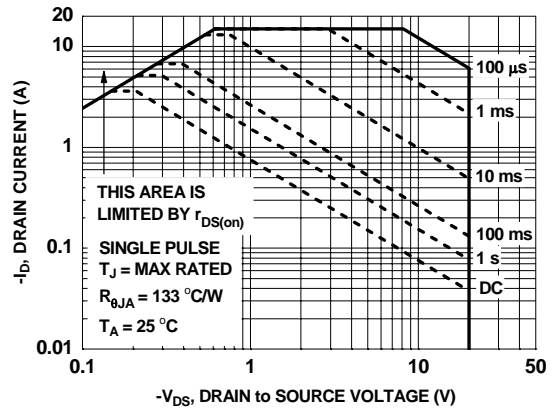


Figure 10. Forward Bias Safe Operating Area

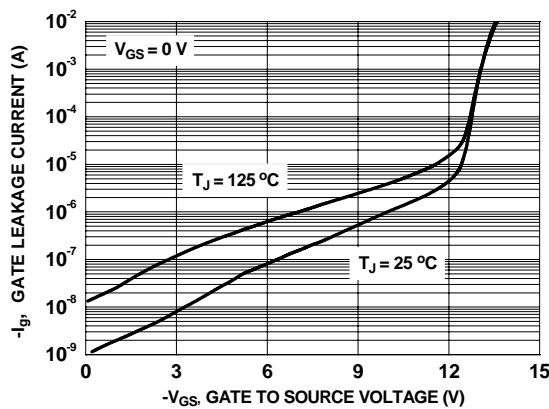


Figure 11. Gate Leakage Current vs Gate to Source Voltage

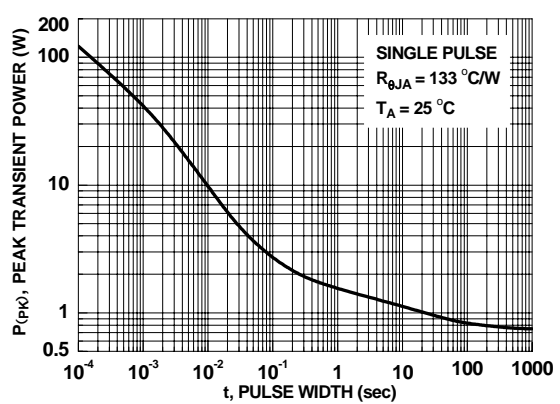


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

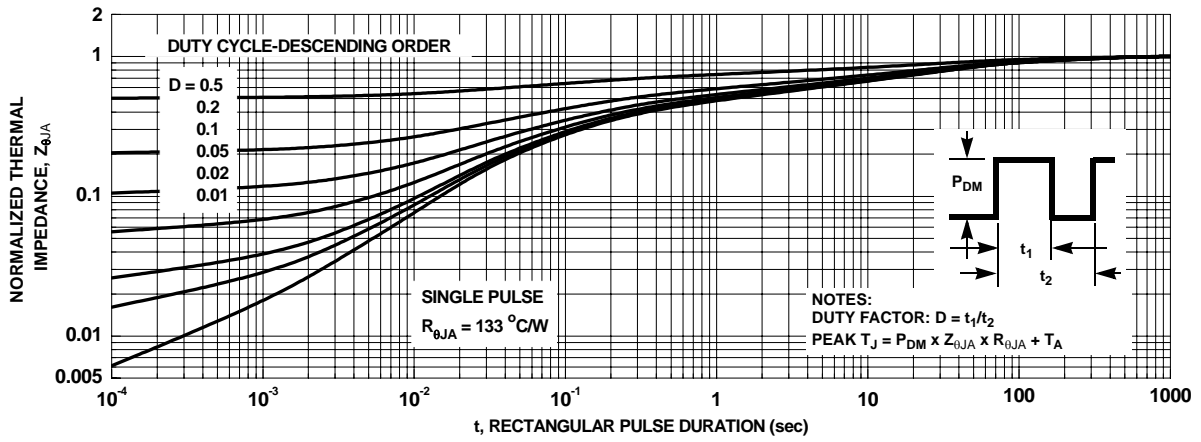
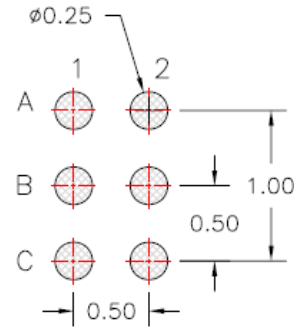
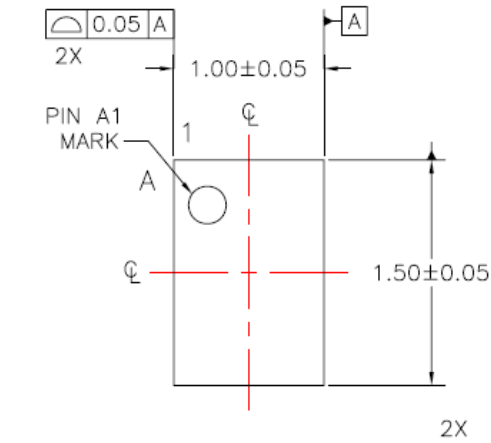
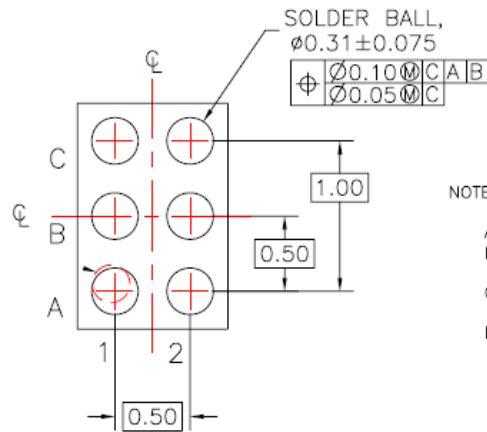
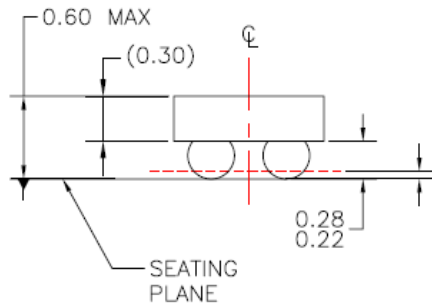


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) NO JEDEC REGISTRATION REFERENCE AS OF OCTOBER 2005.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994
- D) TERMINAL CONFIGURATION TABLE.

GATE	SOURCE	DRAIN
A1	A2, B1, B2	C1, C2

E) DRAWING FILENAME: MKT-UC006AArev4



Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/package/packageDetails.html?id=PN_UCBAU-006



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|--|---|------------------------------------|---|
| AccuPower™ | F-PFST™ | | |
| AX-CAP®* | FRFET® | | |
| BitSiC™ | Global Power Resource SM | PowerTrench® | SYSTEM GENERAL® |
| Build it Now™ | GreenBridge™ | PowerXS™ | TinyBoost® |
| CorePLUS™ | Green FPS™ | Programmable Active Droop™ | TinyBuck® |
| CorePOWER™ | Green FPS™ e-Series™ | QFET® | TinyCalc™ |
| CROSSVOLT™ | Gmax™ | QS™ | TinyLogic® |
| CTL™ | GTO™ | Quiet Series™ | TINYOPTO™ |
| Current Transfer Logic™ | IntelliMAX™ | RapidConfigure™ | TinyPower™ |
| DEUXPEED® | ISOPLANAR™ | | TinyPWM™ |
| Dual Cool™ | Marking Small Speakers Sound Louder and Better™ | | TinyWire™ |
| EcoSPARK® | MegaBuck™ | ing our world, 1mW/W/kW at a time™ | TranSiC™ |
| EfficientMax™ | MICROCOUPLER™ | SignalWise™ | TriFault Detect™ |
| ESBC™ | MicroFET™ | SmartMax™ | TRUECURRENT® |
|  Fairchild® | MicroPak™ | SMART START™ | μSerDes™ |
| Fairchild Semiconductor® | MicroPak2™ | Solutions for Your Success™ |  SerDes™ |
| FACT Quiet Series™ | MillerDrive™ | SPM® | UHC® |
| FACT® | MotionMax™ | STEALTH™ | Ultra FRFET™ |
| FAST® | mWSaver® | SuperFET® | UniFET™ |
| FastvCore™ | OptoHiT™ | SuperSOT™-3 | VCX™ |
| FETBench™ | OPTOLOGIC® | SuperSOT™-6 | VisualMax™ |
| FPS™ | OPTOPLANAR® | SuperSOT™-8 | VoltagePlus™ |
| | | SupreMOS® | XST™ |
| | | SyncFET™ | 仙童™ |
| | | Sync-Lock™ | |

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I68