

LTM4630EV

High Efficiency, Dual 18A Step-Down Power μModule Regulator

DESCRIPTION

Demonstration circuit 1892A features the LTM[®]4630EV, the high efficiency, high density, dual 18A, switch mode step-down power module regulator. The input voltage is from 4.5V to 15V. The output voltage is programmable from 0.6V to 1.8V. DC1892A can deliver up to 18A maximum in each channel. As explained in the LTM4630 data sheet, output current derating is necessary for certain V_{IN} , V_{OUT} and thermal conditions. The board operates in continuous conduction mode in heavy load conditions. For high efficiency at low load currents, the MODE jumper (JP1) selects pulse-skipping mode for noise-sensitive applications or Burst Mode[®] operation in less noise-sensitive applications.

Two outputs can be connected in parallel for a single 36A output solution with optional jumper resistors. The board

allows the user to program how its output ramps up and down through the TRACK/SS pin. The output can be set up to either coincidentally or ratiometrically track with another supply's output. Remote output voltage sensing is available for improved output voltage regulation at the load point. These features and the availability of the LTM4630EV in a compact 16mm × 16mm × 4.41mm LGA package make it ideal for use in many high density point-of-load regulation applications. The LTM4630 data sheet must be read in conjunction with this demo manual for working on or modifying the demo circuit DC1892A.

Design files for this circuit board are available at
<http://www.linear.com/demo/DC1892A>

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BOARD PHOTO

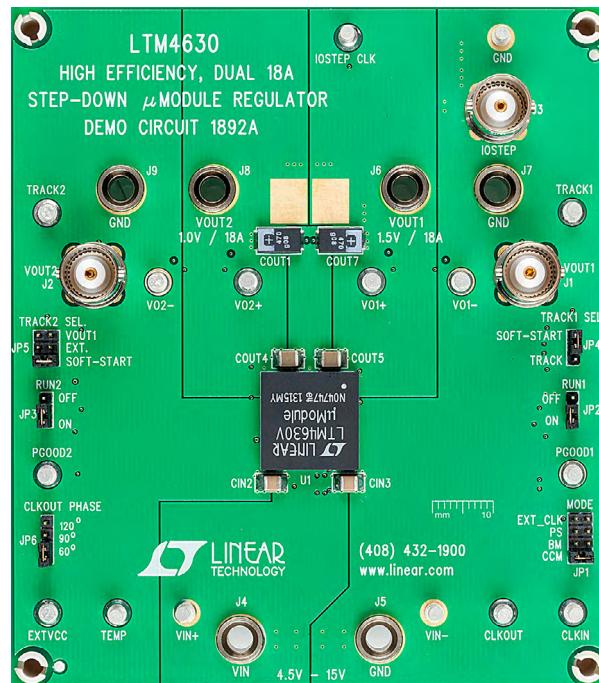


Figure 1. DC1892A

DEMO MANUAL DC1892A

PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$

PARAMETER	CONDITIONS/NOTES	VALUE
Input Voltage Range		4.5V ~ 15V
Output Voltage $V_{\text{OUT}1}$	$V_{\text{IN}} = 4.5 \sim 15\text{V}$, $I_{\text{OUT}1} = 0\text{A} \sim 18\text{A}$, JP1: CCM	$1.5\text{V} \pm 1.5\%$ ($1.4775\text{V} \sim 1.5225\text{V}$)
Output Voltage $V_{\text{OUT}2}$	$V_{\text{IN}} = 4.5 \sim 15\text{V}$, $I_{\text{OUT}2} = 0\text{A} \sim 18\text{A}$, JP1: CCM	$1\text{V} \pm 1.5\%$ ($0.985\text{V} \sim 1.015\text{V}$)
Per Channel Maximum Continuous Output Current	Derating Is Necessary for Certain V_{IN} , V_{OUT} and Thermal Conditions. See the LTM4630 Data Sheet for Details	18A
Default Operating Frequency		500kHz
Resistor Programmable Frequency Range		250kHz to 780kHz
External Clock Sync. Frequency Range		400kHz to 780kHz
Efficiency of Channel 1	$V_{\text{IN}} = 5\text{V}$, $V_{\text{OUT}1} = 1.5\text{V}$, $I_{\text{OUT}1} = 18\text{A}$, $f_{\text{SW}} = 500\text{kHz}$	89.7%, See Figure 3
Efficiency of Channel 2	$V_{\text{IN}} = 5\text{V}$, $V_{\text{OUT}2} = 1\text{V}$, $I_{\text{OUT}2} = 18\text{A}$, $f_{\text{SW}} = 500\text{kHz}$	84.8%, See Figure 4
Load Transient of Channel 1	$V_{\text{IN}} = 12\text{V}$, $V_{\text{OUT}1} = 1.5\text{V}$, $I_{\text{SETP}} = 9 \sim 18\text{A}$	See Figure 5
Load Transient of Channel 2	$V_{\text{IN}} = 12\text{V}$, $V_{\text{OUT}2} = 1\text{V}$, $I_{\text{SETP}} = 9 \sim 18\text{A}$	See Figure 6

QUICK START PROCEDURE

Demonstration circuit DC1892A is easy to set up to evaluate the performance of the LTM4630EV. Please refer to Figure 2 for proper measurement setup and follow the procedure below:

1. Place jumpers in the following positions for a typical application:

JP1	JP2	JP3	JP4	JP5	JP6
MODE	RUN1	RUN2	TRACK1 SEL.	TRACK2 SEL.	CLKOUT PHASE
CCM	ON	ON	SOFT-START	SOFT-START	90°

2. With power off, connect the input power supply, load and meters, as shown in Figure 1. Preset the load to 0A and the V_{IN} supply to 12V.
3. Turn on the power supply at the input. The output voltage in channel 1 should be $1.5\text{V} \pm 1.5\%$ ($1.4775\text{V} \sim 1.5225\text{V}$) and the output voltage in channel 2 should be $1\text{V} \pm 1.5\%$ ($0.985\text{V} \sim 1.015\text{V}$).
4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, output voltage ripple, efficiency and other parameters. Output ripple should be measured at J1 and J2 with BNC cables. 50Ω termination should be set on the oscilloscope or BNC cables.
5. (Optional) For optional load transient test, apply an adjustable pulse signal between the IOSTEP CLK and GND test points. Pulse amplitude (3V ~ 3.5V) sets the load step current amplitude. The output transient current can be monitored at the BNC connector J3 (15mV/A). The pulse signal should have very small duty cycle (< 10%) to limit the thermal stress on the transient load circuit. Switch the jumper resistors R34 or R35 (on the backside of boards) to apply load transient on channel 1 or channel 2, correspondingly.
6. (Optional) LTM4630 can be synchronized to an external clock signal. Place the JP1 jumper on EXT_CLK and apply a clock signal (0 ~ 5V, square wave) on the CLKIN test point.
7. (Optional) The outputs of LTM4630 can track another supply. The jumpers JP4 and JP5 allow choosing soft-start or output tracking. If tracking external voltage is selected, the corresponding test points, TRACK1 and TRACK2, need to be connected to a valid voltage signal.
8. (Optional) LTM4630 can be configured for a 2-phase single output at up to 36A on DC1892A. Install 0Ω resistors on R14, R17, R28, R39 and remove R7, R19. Output voltage is set by R25 based on the equation:

$$V_{\text{OUT}} = 0.6\text{V} \cdot \left(1 + \frac{60.4\text{k}}{R_{25}}\right)$$

dc1892afa

QUICK START PROCEDURE

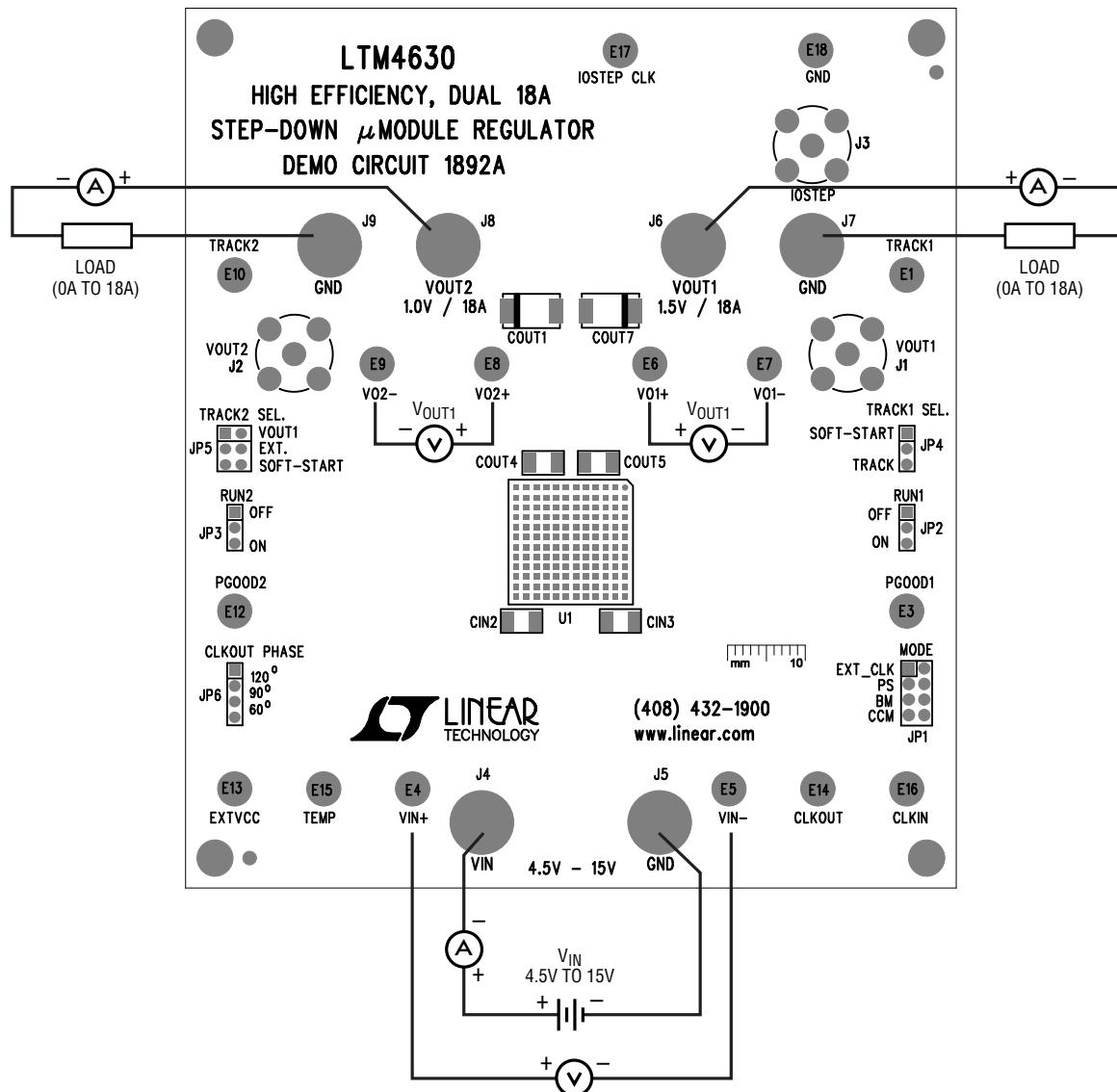


Figure 2. Test Setup of the DC1892A

DEMO MANUAL DC1892A

QUICK START PROCEDURE

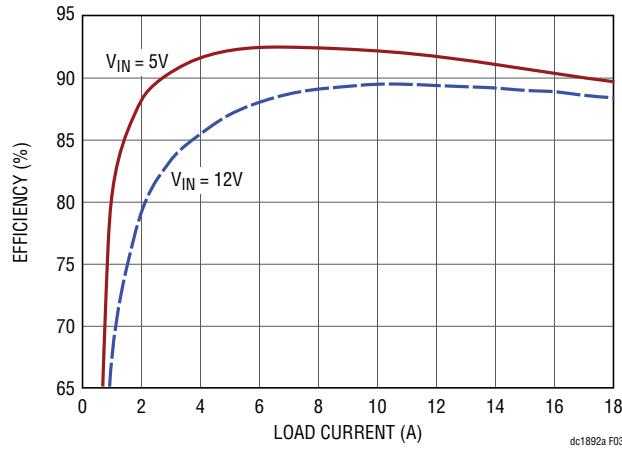


Figure 3. Measured Efficiency on Channel 1. $V_{OUT1} = 1.5V$, $f_{SW} = 500kHz$, Channel 2 Disabled, CCM, 0A to 18A

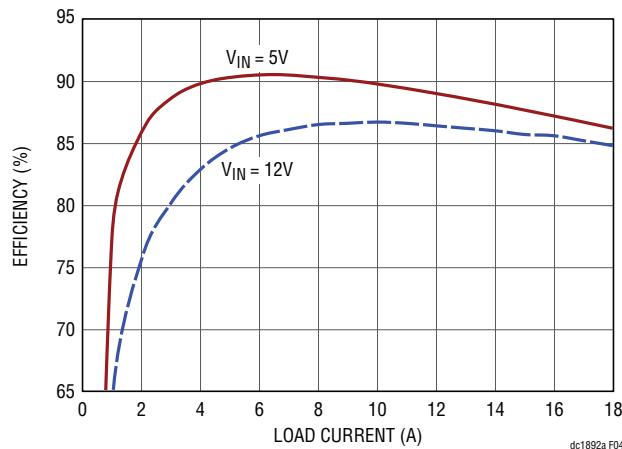
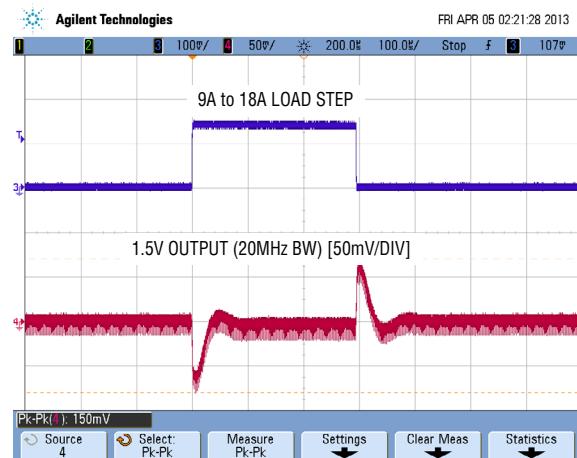
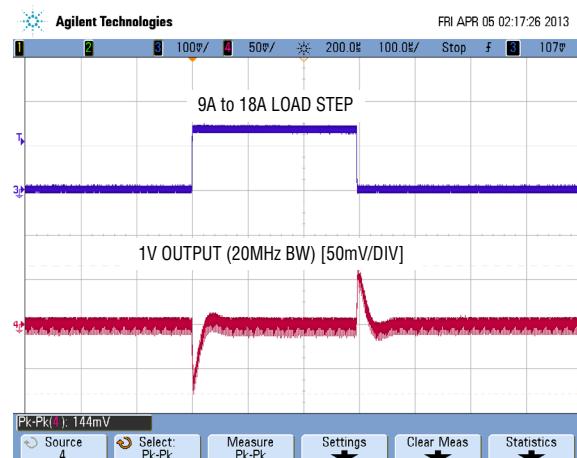


Figure 4. Measured Efficiency on Channel 2. $V_{OUT2} = 1V$, $f_{SW} = 500kHz$, Channel 1 Disabled, CCM, 0A to 18A

QUICK START PROCEDURE



**Figure 5. Measured Channel 1, 9A to 18A Load Transient
($V_{IN} = 12V$, $V_{OUT1} = 1.5V$)**



**Figure 6. Measured Channel 2, 9A to 18A Load Transient
($V_{IN} = 12V$, $V_{OUT2} = 1V$)**

DEMO MANUAL DC1892A

QUICK START PROCEDURE

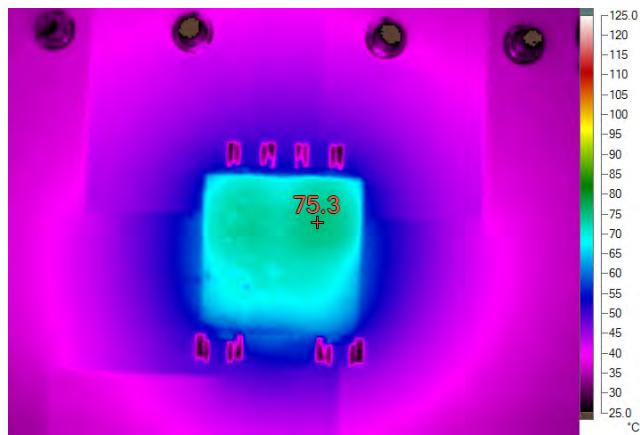


Figure 7. Thermal Capture at $12V_{IN}$, $1.5V_{OUT1}$ at 18A and $1V_{OUT2}$ at 18A ($T_A = 25^{\circ}C$, 200 LFM Airflow and No Heat Sink)

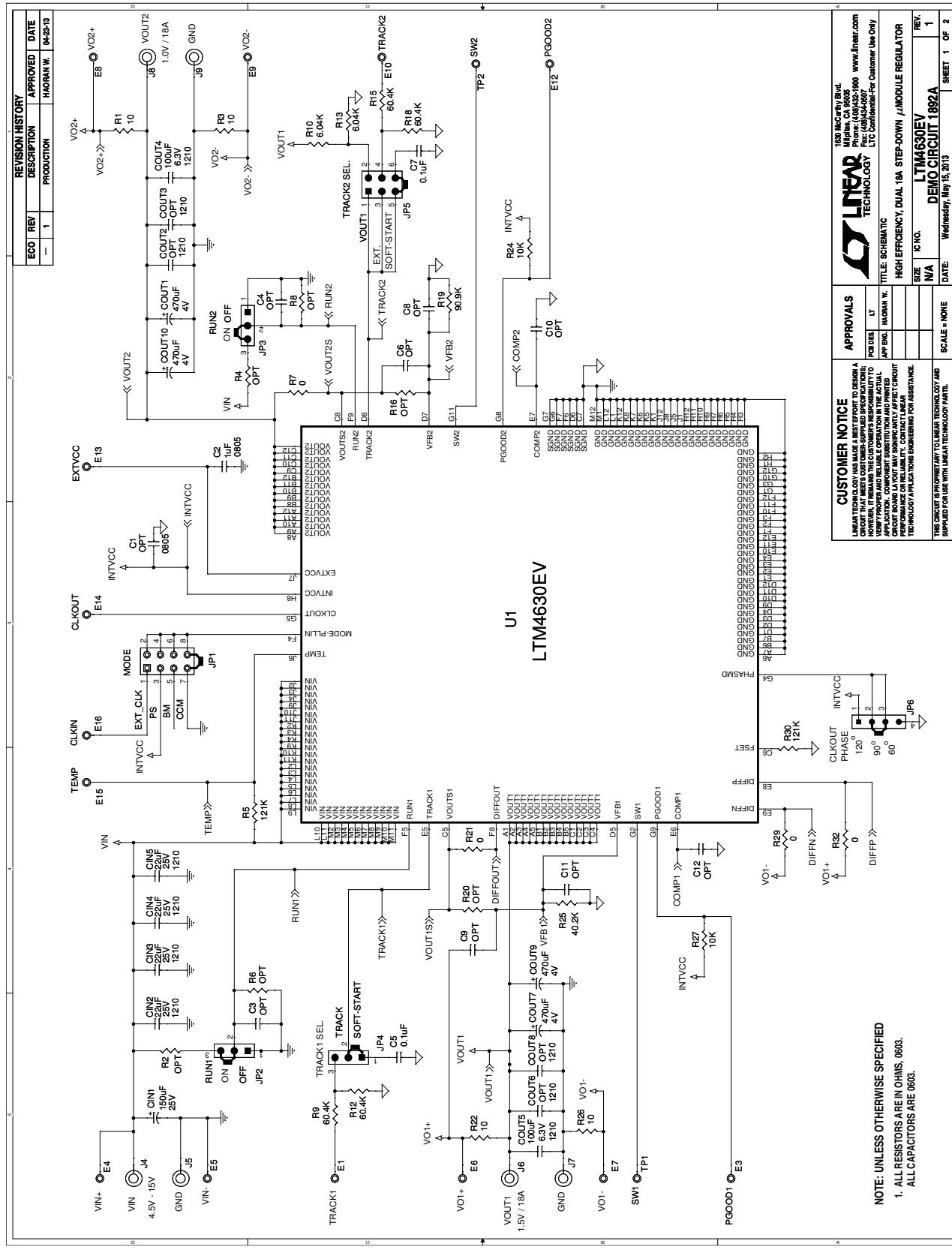
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PARTS LIST

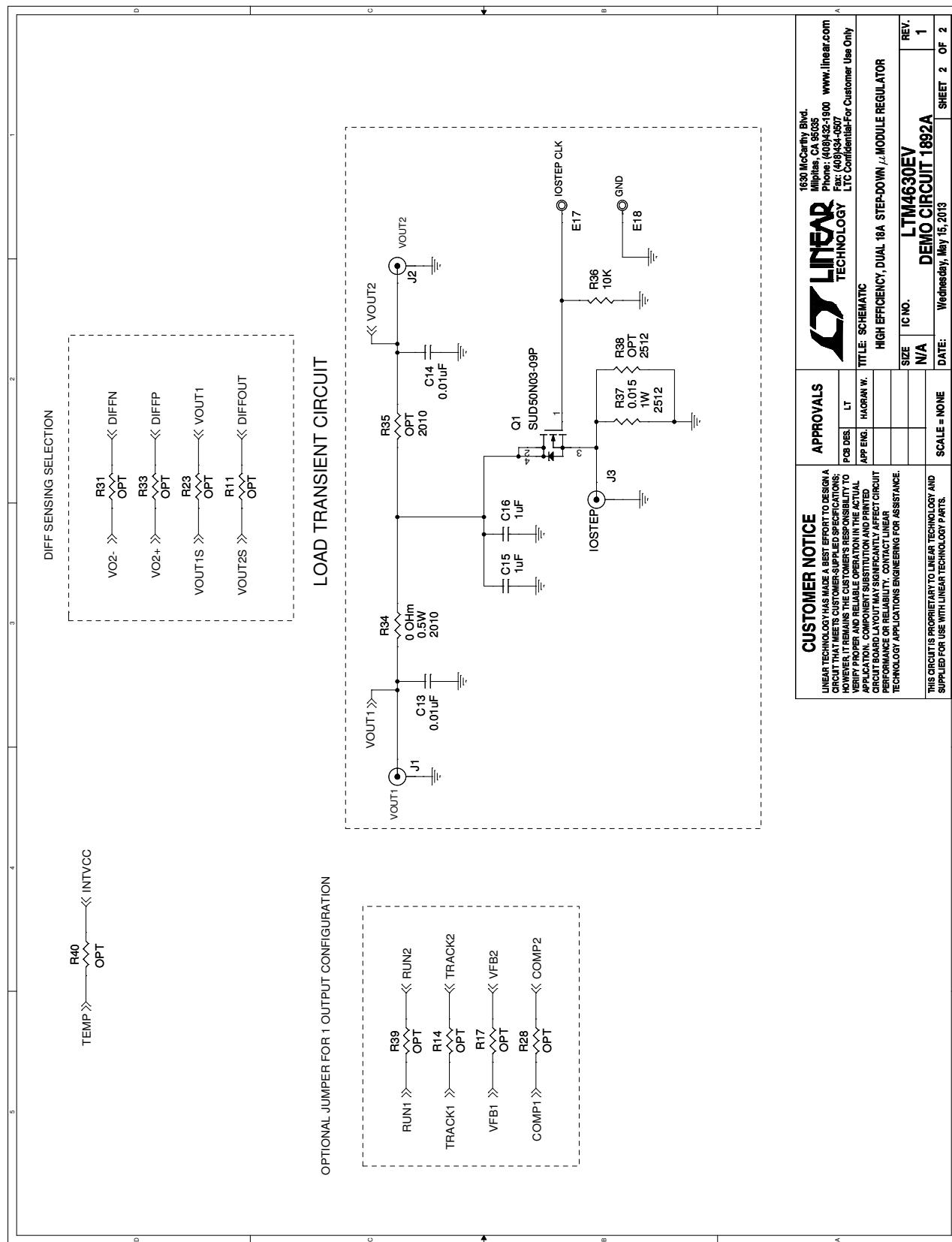
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	4	CIN2, CIN3, CIN4, CIN5	CAP., X5R, 22µF, 25V, 10%, 1210	MURATA, GRM32ER61E226KE15
2	2	COUT1, COUT7, COUT9, COUT10	CAP., 470µF, 4V, POSCAP, F8	SANYO, 4TPE470MCL
3	2	COUT4, COUT5	CAP., X5R, 100µF, 6.3V, 20%, 1210	AVX, 12106D107MAT2A
4	2	R22, R26	RES., CHIP, 10, 1%, 0603	VISHAY, CRCW060310R0FKEA
5	1	R19	RES., CHIP, 90.9k, 1%, 0603	VISHAY, CRCW060390K0FKEA
6	1	R25	RES., CHIP, 40.2k, 1%, 0603	VISHAY, CRCW060340K2FKEA
7	1	R5, R30	RES., CHIP, 121k, 1%, 0603	VISHAY, CRCW0603121KFKEA
8	1	U1	LTM4630EV, 16x16x4.41-LGA	LINEAR TECHNOLOGY, LTM4630EV
Additional Demo Board Circuit Components				
9	1	CIN1	CAP., 150µF, 25V, ALUMINUM ELECTR.,	SUN ELECT., 25CE150AX
10	0	COUT2, COUT3, COUT6, COUT8	OPT, 1210	
11	0	C1	OPT, 0805	
12	1	C2	CAP., X7R, 1µF, 25V, 10%, 0805	AVX, 08053C105KAT2A
13	2	C5, C7	CAP., X5R, 0.1µF, 25V, 10%, 0603	AVX, 06033D104KAT
14	0	C3, C4, C6, C8-C12	OPT, 0603	
15	2	C13, C14	CAP., X7R, 0.01µF, 50V, 10%, 0603	AVX, 06035C103KAT2A
16	2	C15, C16	CAP., X7R, 1µF, 10V, 10%, 0603	AVX, 0603ZC105KAT2A
17	1	Q1	N-CHANNEL 30V MOSFET	VISHAY, SUD50N03-09P
18	2	R1, R3,	RES., CHIP, 10, 1%, 0603	VISHAY, CRCW060310R0FKEA
19	0	R2, R4, R6, R8, R11, R14, R16, R17, R20, R23, R28, R31, R33, R39, R40	OPT, 0603	
20	4	R24, R27, R36	RES., CHIP, 10k, 1%, 0603	VISHAY, CRCW060310K0FKED
21	4	R7, R21, R29, R32	RES., CHIP, 0, 1%, 0603	VISHAY, CRCW06030000Z0ED
22	5	R9, R12, R15, R18	RES., CHIP, 60.4k, 1%, 0603	VISHAY, CRCW060360K4FKED
23	2	R10, R13	RES., CHIP, 6.04k, 1%, 0603	VISHAY, CRCW06036K04FKED
24	1	R34	RES., CHIP, 0Ω, 0.5W, 2010	VISHAY, CRCW20100000Z0EF
25	0	R35	OPT, 2010	
26	1	R37	RES., CHIP, 0.015Ω, 2W, 2512	VISHAY, WSL2512R0150FEA
27	0	R38	OPT, 2512	
Hardware: For Demo Board Only				
28	16	E1, E3-E10, E12-E16	TESTPOINT, TURRET, 0.094" PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
29	3	J1, J2, J3	CONN, BNC, 5 PINS	CONNEX 112404
30	6	J4-J9	JACK BANANA	KEYSTONE, 575-4
31	1	JP1	HEADER, 4-PIN, 0.079", DOUBLE ROW	SAMTEC, TMM104-02-L-D
32	1	JP6	HEADER, 4-PIN, 0.079", SINGLE ROW	SAMTEC, TMM104-02-L-S
33	3	JP2, JP3, JP4	HEADER, 3-PIN, 0.079", SINGLE ROW	SAMTEC, TMM103-02-L-S
34	1	JP5	HEADER, 3-PIN, 0.079", DOUBLE ROW	SAMTEC, TMM-103-02-L-D
35	6	XJP1-XJP6	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G
36	4	(STAND-OFF)	STAND-OFF, NYLON, 0.50"	KEYSTONE, 8833 (SNAP-ON)

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SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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