ULTRALOW-NOISE, HIGH-PSRR, FAST, RF, 1.5-A
LOW-DROPOUT LINEAR REGULATORS

FEATURES
- 1.5-A Low-Dropout Regulator With Enable
- Available in Fixed and Adjustable (1.2-V to 5.5-V) Output Versions
- High PSRR (49 dB at 10 kHz)
- Ultralow Noise (48 \( \mu \)VRMS, TPS78630)
- Fast Start-Up Time (50 \( \mu \)s)
- Stable With a 1-\( \mu \)F Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (390 mV at Full Load, TPS78630)
- 3 \times 3 \) SON PowerPAD™, 6-Pin SOT223 and
5-Pin DDPAK Package

APPLICATIONS
- RF: VCOs, Receivers, ADCs
- Audio
- Bluetooth®, Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

DESCRIPTION
The TPS786xx family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in small outline, SOT223-6 and DDPAK-5 packages. Each device in the family is stable, with a small 1-\( \mu \)F ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 390 mV at 1.5 A). Each device achieves fast start-up times (approximately 50 \( \mu \)s) while consuming very low quiescent current (265 \( \mu \)A, typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 \( \mu \)A. The TPS78630 exhibits approximately 48 \( \mu \)VRMS of output voltage at 3.0-V output noise with a 0.1-\( \mu \)F bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR, low noise features, and the fast response time.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

Copyright © 2002–2010, Texas Instruments Incorporated

PRODUCTION DATA information is current as of publication date.
Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS786xx yyy z</td>
<td>XX is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). YYY is package designator. Z is package quantity.</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Output voltages from 1.3 V to 5.0 V in 100-mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>OVER OPERATING TEMPERATURE (UNLESS OTHERWISE NOTED)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VALUE</strong></td>
</tr>
<tr>
<td>( V_{\text{IN}} ) range</td>
</tr>
<tr>
<td>( V_{\text{EN}} ) range</td>
</tr>
<tr>
<td>( V_{\text{OUT}} ) range</td>
</tr>
<tr>
<td>Peak output current</td>
</tr>
<tr>
<td>ESD rating, HBM</td>
</tr>
<tr>
<td>ESD rating, CDM</td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
</tr>
<tr>
<td>Junction temperature range, ( T_J )</td>
</tr>
<tr>
<td>Storage temperature range, ( T_{\text{stg}} )</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **absolute maximum ratings** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under **recommended operating conditions** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
## THERMAL INFORMATION

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)(2)</th>
<th>TPS786xx(3)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DRB</td>
<td>DCQ</td>
</tr>
<tr>
<td></td>
<td>8 PINS</td>
<td>6 PINS</td>
</tr>
<tr>
<td>$\theta_{JA}$</td>
<td>47.8</td>
<td>70.4</td>
</tr>
<tr>
<td>$\theta_{JCtop}$</td>
<td>83</td>
<td>70</td>
</tr>
<tr>
<td>$\theta_{JB}$</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>2.1</td>
<td>6.8</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>17.8</td>
<td>30.1</td>
</tr>
<tr>
<td>$\theta_{JCbot}$</td>
<td>12.1</td>
<td>6.3</td>
</tr>
</tbody>
</table>

### THERMAL METRIC DEFINITIONS:

1. For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report, SPRA953A.
2. For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
3. Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
   a. DRB: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
   b. DCQ: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.
   c. KTT: The exposed pad is connected to the PCB ground layer through a 5x4 thermal via array.
4. The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in the JESD51-7, in an environment described in JESD51-2a.
5. The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
6. The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
7. The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $\theta_{JA}$ using a procedure described in JESD51-2a (sections 6 and 7).
8. The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain $\theta_{JA}$ using a procedure described in JESD51-2a (sections 6 and 7).
9. The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range (T_J = −40°C to +125°C), V_EN = V_IN, V_IN = V_OUT(nom) + 1 V (1), I_OUT = 1 mA, C_OUT = 10 μF, and C_NR = 0.01 μF, unless otherwise noted. Typical values are at +25°C.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage, V_IN (1)</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal reference, V_FB (TPS78601)</td>
<td>1.200</td>
<td>1.225</td>
<td>1.250</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Continuous output current I_OUT</td>
<td>0</td>
<td>1.5</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage range TPS78601 (2)</td>
<td>0 μA ≤ I_OUT ≤ 1.5 A, V_OUT + 1 V ≤ V_IN ≤ 5.5 V (1)</td>
<td>1.225</td>
<td>5.5 – V.DO</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fixed V_OUT &lt; 5 V</td>
<td>(0.98)V_OUT</td>
<td>V_OUT</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fixed V_OUT = 5 V</td>
<td>–2.0</td>
<td>+2.0</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Output voltage line regulation (ΔV_OUT/V_IN) (1)</td>
<td>V_OUT + 1 V ≤ V_IN ≤ 5.5 V</td>
<td>0 μA ≤ I_OUT ≤ 1.5 A, V_OUT + 1 V ≤ V_IN ≤ 5.5 V (1)</td>
<td>–3.0</td>
<td>+3.0</td>
<td>%</td>
</tr>
<tr>
<td>Load regulation (ΔV_OUT/V_OUT)</td>
<td>0 μA ≤ I_OUT ≤ 1.5 A, V_OUT + 1 V ≤ V_IN ≤ 5.5 V (1)</td>
<td>0.07</td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Dropout voltage (3) V_IN = V_OUT(nom) − 0.1 V</td>
<td>TPS78628</td>
<td>I_OUT = 1.5 A</td>
<td>410</td>
<td>580</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>TPS78630</td>
<td>I_OUT = 1.5 A</td>
<td>390</td>
<td>550</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TPS78633</td>
<td>I_OUT = 1.5 A</td>
<td>340</td>
<td>510</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TPS78650</td>
<td>I_OUT = 1.5 A</td>
<td>310</td>
<td>470</td>
<td></td>
</tr>
<tr>
<td>Output current limit</td>
<td>V_OUT = 0 V</td>
<td>2.4</td>
<td>4.2</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Ground pin current</td>
<td>0 μA ≤ I_OUT ≤ 1.5 A</td>
<td>260</td>
<td>385</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Shutdown current (4)</td>
<td>V_EN = 0 V, 2.7 V ≤ V_IN ≤ 5.5 V</td>
<td>0.07</td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>FB pin current</td>
<td>V_FB = 1.225 V</td>
<td>1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-supply ripple rejection TPS78630</td>
<td>f = 100 Hz, I_OUT = 10 mA</td>
<td>59</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 100 Hz, I_OUT = 1.5 A</td>
<td>52</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>f = 10 kHz, I_OUT = 1.5 A</td>
<td>49</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output noise voltage (TPS78630) BW = 100 Hz to 100 kHz,</td>
<td>I_OUT = 1.5 A</td>
<td>C_NR = 0.001 μF</td>
<td>66</td>
<td>μV RMS</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_NR = 0.0047 μF</td>
<td>51</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_NR = 0.01 μF</td>
<td>49</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_NR = 0.1 μF</td>
<td>48</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time, start-up (TPS78630)</td>
<td>R_L = 2 Ω, C_OUT = 1 μF</td>
<td>C_NR = 0.001 μF</td>
<td>50</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_NR = 0.0047 μF</td>
<td>75</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_NR = 0.01 μF</td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-level enable input voltage</td>
<td>2.7 V ≤ V_IN ≤ 5.5 V</td>
<td>1.7</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-level enable input voltage</td>
<td>2.7 V ≤ V_IN ≤ 5.5 V</td>
<td>0</td>
<td>0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN pin current</td>
<td>V_EN = 0</td>
<td>–1</td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>UVLO threshold</td>
<td>V_OUT rising</td>
<td>2.25</td>
<td>2.65</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>UVLO hysteresis</td>
<td></td>
<td>100</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Minimum V_IN = V_OUT + V.DO or 2.7 V, whichever is greater. The TPS78650 is tested at V_IN = 5.5 V.
(2) Tolerance of external resistors not included in this specification.
(3) Dropout is not measured for TPS78618 or TPS78625 since minimum V_IN = 2.7 V.
(4) For adjustable version, this applies only after V_IN is applied; then V_EN transitions high to low.
**FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION**

**FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION**

**PIN CONFIGURATIONS**

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NAME</th>
<th>DCQ (SOT223)</th>
<th>KTT (DDPAK)</th>
<th>DRB (SON)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NR</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td></td>
<td>Noise-reduction pin for fixed versions only. An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.</td>
</tr>
<tr>
<td>EN</td>
<td>1</td>
<td>1</td>
<td>8</td>
<td></td>
<td>The EN terminal is an input that enables or shuts down the device. When EN is a logic high, the device is enabled. When the device is a logic low, the device is in shutdown mode.</td>
</tr>
<tr>
<td>FB</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td></td>
<td>Feedback input voltage for the adjustable device.</td>
</tr>
<tr>
<td>GND</td>
<td>3, 6</td>
<td>3, TAB</td>
<td>6</td>
<td></td>
<td>Regulator ground</td>
</tr>
<tr>
<td>IN</td>
<td>2</td>
<td>2</td>
<td>1, 2</td>
<td></td>
<td>Input supply</td>
</tr>
<tr>
<td>OUT</td>
<td>4</td>
<td>4</td>
<td>3, 4</td>
<td></td>
<td>Regulator output</td>
</tr>
</tbody>
</table>
TPS786xx

TYPICAL CHARACTERISTICS

TPS78630
OUTPUT VOLTAGE
VS
OUTPUT CURRENT

\[ V_{\text{IN}} = 4 \text{V} \]
\[ C_{\text{OUT}} = 10 \mu \text{F} \]
\[ T_{J} = 25^\circ \text{C} \]

\[ V_{\text{OUT}}(\text{V}) \]
\[ I_{\text{OUT}}(\text{A}) \]

Figure 1.

TPS78628
OUTPUT VOLTAGE
VS
JUNCTION TEMPERATURE

\[ V_{\text{IN}} = 3.8 \text{V} \]
\[ C_{\text{OUT}} = 10 \mu \text{F} \]
\[ I_{\text{OUT}} = 1 \text{mA} \]
\[ I_{\text{OUT}} = 1.5 \text{A} \]

\[ V_{\text{OUT}}(\text{V}) \]
\[ T_{J}(^\circ \text{C}) \]

Figure 2.

TPS78628
GROUND CURRENT
VS
JUNCTION TEMPERATURE

\[ V_{\text{IN}} = 3.8 \text{V} \]
\[ C_{\text{OUT}} = 10 \mu \text{F} \]
\[ I_{\text{OUT}} = 1 \text{mA} \]
\[ I_{\text{OUT}} = 1.5 \text{A} \]

\[ I_{\text{GND}}(\text{mA}) \]
\[ T_{J}(^\circ \text{C}) \]

Figure 3.

TPS78630
OUTPUT SPECTRAL
NOISE DENSITY
VS
FREQUENCY

\[ V_{\text{IN}} = 5.5 \text{V} \]
\[ C_{\text{OUT}} = 2.2 \mu \text{F} \]
\[ C_{\text{NR}} = 0.1 \mu \text{F} \]
\[ I_{\text{OUT}} = 1 \text{mA} \]
\[ I_{\text{OUT}} = 1.5 \text{A} \]

\[ \text{Output Spectral Noise Density} \ (\mu \text{V}/\sqrt{\text{Hz}}) \]
\[ \text{Frequency (Hz)} \]

Figure 4.

TPS78630
OUTPUT SPECTRAL
NOISE DENSITY
VS
FREQUENCY

\[ V_{\text{IN}} = 5.5 \text{V} \]
\[ C_{\text{OUT}} = 10 \mu \text{F} \]
\[ C_{\text{NR}} = 0.1 \mu \text{F} \]
\[ I_{\text{OUT}} = 1 \text{mA} \]
\[ I_{\text{OUT}} = 1.5 \text{A} \]

\[ \text{Output Spectral Noise Density} \ (\mu \text{V}/\sqrt{\text{Hz}}) \]
\[ \text{Frequency (Hz)} \]

Figure 5.

TPS78630
OUTPUT SPECTRAL
NOISE DENSITY
VS
FREQUENCY

\[ V_{\text{IN}} = 5.5 \text{V} \]
\[ C_{\text{OUT}} = 10 \mu \text{F} \]
\[ C_{\text{NR}} = 0.1 \mu \text{F} \]
\[ I_{\text{OUT}} = 1 \text{mA} \]
\[ I_{\text{OUT}} = 1.5 \text{A} \]
\[ C_{\text{NR}} = 0.01 \mu \text{F} \]
\[ C_{\text{NR}} = 0.0047 \mu \text{F} \]
\[ C_{\text{NR}} = 0.001 \mu \text{F} \]

\[ \text{Output Spectral Noise Density} \ (\mu \text{V}/\sqrt{\text{Hz}}) \]
\[ \text{Frequency (Hz)} \]

Figure 6.
TYPICAL CHARACTERISTICS (continued)

TPS78630
ROOT MEAN SQUARED OUTPUT NOISE
vs BYPASS CAPACITANCE

Figure 7.

TPS78630
RIPPLE REJECTION
vs FREQUENCY

Figure 10.

TPS78628
DROPOUT VOLTAGE
vs JUNCTION TEMPERATURE

Figure 8.

TPS78630
RIPPLE REJECTION
vs FREQUENCY

Figure 11.

TPS78630
RIPPLE REJECTION
vs FREQUENCY

Figure 12.

TPS78618
LINE TRANSIENT RESPONSE

Figure 13.

TPS78630
LINE TRANSIENT RESPONSE

Figure 14.

TPS78628
LOAD TRANSIENT RESPONSE

Figure 15.
TPS786xx

TYPICAL CHARACTERISTICS (continued)

**TPS78625**
**POWER-UP/POWER-DOWN**

- \( V_{\text{OUT}} = 2.5 \text{ V} \)
- \( R_L = 1.6 \text{ }\Omega \)
- \( C_{\text{NR}} = 0.01 \mu \text{F} \)

**Figure 16.**

**TPS78630**
**DROPOUT VOLTAGE vs OUTPUT CURRENT**

- \( V_{\text{IN}} \)
- \( V_{\text{OUT}} \)
- \( T_J = 25^\circ \text{C} \)
- \( T_J = -40^\circ \text{C} \)
- \( T_J = 125^\circ \text{C} \)

**Figure 17.**

**TPS78601**
**DROPOUT VOLTAGE vs INPUT VOLTAGE**

- \( I_{\text{OUT}} = 1.5 \text{ A} \)
- \( C_{\text{OUT}} = 10 \mu \text{F} \)
- \( C_{\text{NR}} = 0.01 \mu \text{F} \)

**Figure 18.**

**MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE**

- \( I_{\text{OUT}} = 1.5 \text{ A} \)
- \( T_J = 125^\circ \text{C} \)
- \( T_J = 25^\circ \text{C} \)

**Figure 19.**

**TPS78630**
**TYPICAL REGIONS OF STABILITY**
**EQUIVALENT SERIES RESISTANCE (ESR)**

- \( C_{\text{OUT}} = 1 \mu \text{F} \)
- \( C_{\text{OUT}} = 2.2 \mu \text{F} \)

**Figure 20.**

**Figure 21.**
TPS78630
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)

Figure 22.

START-UP

Figure 23.
APPLICATION INFORMATION

The TPS786xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265 μA, typically), and enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 24.

![Figure 24. Typical Application Circuit](image)

EXTERNAL CAPACITOR REQUIREMENTS

A 2.2-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS786xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS786xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitor is 1 μF. Any 1 μF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS786xx has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1-μF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the functional block diagram.

For example, the TPS78630 exhibits only 48 μV<sub>RMS</sub> of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 10-μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V<sub>IN</sub> and V<sub>OUT</sub>, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

REGULATOR MOUNTING

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

**PROGRAMMING THE TPS78601 ADJUSTABLE LDO REGULATOR**

The output voltage of the TPS78601 adjustable regulator is programmed using an external resistor divider as shown in Figure 25. The output voltage is calculated using Equation 1:

\[
V_{\text{OUT}} = V_{\text{REF}} \times \left(1 + \frac{R_1}{R_2}\right)
\]

where:

- \(V_{\text{REF}} = 1.2246 \, \text{V typ}\) (the internal reference voltage)

Resistors \(R_1\) and \(R_2\) should be chosen for approximately 40-μA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose \(R_2 = 30.1\, \text{kΩ}\) to set the divider current at 40 μA, \(C_1 = 15 \, \text{pF}\) for stability, and then calculate \(R_1\) using Equation 2:

\[
R_1 = \frac{V_{\text{OUT}}}{V_{\text{REF}}} \times R_2 - 1
\]

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB.

The approximate value of this capacitor can be calculated using Equation 3:

\[
C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)}
\]  

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2 μF instead of 1 μF.

**REGULATOR PROTECTION**

The TPS786xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS786xx features internal current limiting and thermal protection. During normal operation, the TPS786xx limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately +165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately +140°C, regulator operation resumes.

![Figure 25. TPS78601 Adjustable LDO Regulator Programming](image-url)
POWER DISSIPATION

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

\[ P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \]  \hspace{1cm} (4)

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the SON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On both SOT-223 (DCQ) and DDPAK (KTT) packages, the primary conduction path for heat is through the tab to the PCB. That tab should be connected to ground.

The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

\[ R_{JUA} = \frac{(+125^\circ C - T_A)}{P_D} \]  \hspace{1cm} (5)

Knowing the maximum \( R_{JUA} \), the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 26.

Figure 26 shows the variation of \( \theta_{JA} \) as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

**NOTE:** When the device is mounted on an application PCB, it is strongly recommended to use \( \Psi_{JT} \) and \( \Psi_{JB} \), as explained in the *Estimating Junction Temperature* section.
ESTIMATING JUNCTION TEMPERATURE

Using the thermal metrics $\Psi_{JT}$ and $\Psi_{JB}$, as shown in the Thermal Information table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $\theta_{JC, Top}$ parameter is listed as well.

\[ \Psi_{JT}: \quad T_{J} = T_{T} + \Psi_{JT} \cdot P_{D} \]
\[ \Psi_{JB}: \quad T_{J} = T_{B} + \Psi_{JB} \cdot P_{D} \]  

(6)

Where $P_{D}$ is the power dissipation shown by Equation 5, $T_{T}$ is the temperature at the center-top of the IC package, and $T_{B}$ is the PCB temperature measured 1mm away from the IC package on the PCB surface (as Figure 28 shows).

NOTE: Both $T_{T}$ and $T_{B}$ can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring $T_{T}$ and $T_{B}$, see the application note SBVA025, Using New Thermal Metrics, available for download at www.ti.com.

By looking at Figure 27, the new thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) have very little dependency on board size. That is, using $\Psi_{JT}$ or $\Psi_{JB}$ with Equation 6 is a good way to estimate $T_{J}$ by simply measuring $T_{T}$ or $T_{B}$, regardless of the application board size.

Figure 27. $\Psi_{JT}$ and $\Psi_{JB}$ vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC,top}$ to determine thermal characteristics, refer to application report SBVA025, Using New Thermal Metrics, available for download at www.ti.com. For further information, refer to application report SPRA953, IC Package Thermal Metrics, also available on the TI website.

Figure 28. Measuring Points for $T_{T}$ and $T_{B}$

(1) $T_{T}$ is measured at the center of both the X- and Y-dimensional axes.
(2) $T_{B}$ is measured below the package lead on the PCB surface.
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (August, 2010) to Revision L

| • Corrected typo in Figure 28 | ............................................................... 13 |

Changes from Revision J (May, 2009) to Revision K

| • Replaced the Dissipation Ratings table with the Thermal Information Table | ............................................................... 3 |
| • Revised Thermal Information section | ........................................................................ 12 |
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS78601DCQ</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>78</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78601</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78601DCQG4</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78601</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78601DCQR</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78601</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78601DCQRG4</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78601</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78601DRBR</td>
<td>ACTIVE</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OCI</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78601DRBT</td>
<td>ACTIVE</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OCI</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78601KTT</td>
<td>OBSOLETE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS78601KTTR</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>TPS78601</td>
<td>TPS78601</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78601KTTRG3</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>TPS78601</td>
<td>TPS78601</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78601KTTTT</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>TPS78601</td>
<td>TPS78601</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78618DCQ</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>78</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78618</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78618DCQR</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78618</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78618DCQRG4</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78618</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78618KTT</td>
<td>OBSOLETE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS78618KTTR</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>TPS78618</td>
<td>TPS78618</td>
<td>Samples</td>
</tr>
<tr>
<td>TPS78618KTTRE3</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>TPS78618</td>
<td>TPS78618</td>
<td>Samples</td>
</tr>
<tr>
<td>Orderable Device</td>
<td>Status</td>
<td>Package Type</td>
<td>Package Drawing</td>
<td>Pins</td>
<td>Package Qty</td>
<td>Eco Plan</td>
<td>MSL Peak Temp</td>
<td>Op Temp (°C)</td>
<td>Device Marking</td>
<td>Samples</td>
<td></td>
</tr>
<tr>
<td>------------------</td>
<td>--------</td>
<td>--------------</td>
<td>-----------------</td>
<td>------</td>
<td>-------------</td>
<td>----------</td>
<td>---------------</td>
<td>--------------</td>
<td>----------------</td>
<td>---------</td>
<td></td>
</tr>
<tr>
<td>TPS78618KTTRG3</td>
<td>ACTIVE</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>TPS 78618</td>
<td></td>
</tr>
<tr>
<td>TPS78618KTTRT</td>
<td>ACTIVE</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>TPS 78618</td>
<td></td>
</tr>
<tr>
<td>TPS78618KTTTGG3</td>
<td>ACTIVE</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>TPS 78618</td>
<td></td>
</tr>
<tr>
<td>TPS78625DCQ</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>78</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78625</td>
<td></td>
</tr>
<tr>
<td>TPS78625DCQG4</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>78</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78625</td>
<td></td>
</tr>
<tr>
<td>TPS78625DCQR</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78625</td>
<td></td>
</tr>
<tr>
<td>TPS78625DCQRG4</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78625</td>
<td></td>
</tr>
<tr>
<td>TPS78625KTT</td>
<td>OBSOLETE</td>
<td>DDPACK/ TO-263</td>
<td>KTT</td>
<td>5</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td>TPS 78625</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS78625KTTR</td>
<td>ACTIVE</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>TPS 78625</td>
<td></td>
</tr>
<tr>
<td>TPS78625KTTT</td>
<td>ACTIVE</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>TPS 78625</td>
<td></td>
</tr>
<tr>
<td>TPS78628DCQ</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>78</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78630</td>
<td></td>
</tr>
<tr>
<td>TPS78630DCQ</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78630</td>
<td></td>
</tr>
<tr>
<td>TPS78630DCQR</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78630</td>
<td></td>
</tr>
<tr>
<td>TPS78630KTT</td>
<td>OBSOLETE</td>
<td>DDPACK/ TO-263</td>
<td>KTT</td>
<td>5</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td>TPS 78630</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS78630KTTR</td>
<td>ACTIVE</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>TPS 78630</td>
<td></td>
</tr>
</tbody>
</table>

Addendum-Page 2
<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS78630KTTTG3</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>TPS 78630</td>
<td></td>
</tr>
<tr>
<td>TPS78633DCQ</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>78</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78633</td>
<td></td>
</tr>
<tr>
<td>TPS78633DCQG4</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>78</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78633</td>
<td></td>
</tr>
<tr>
<td>TPS78633DCQG4</td>
<td>ACTIVE</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>PS78633</td>
<td></td>
</tr>
<tr>
<td>TPS78633KTTT</td>
<td>OBSOLETE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS78633KTTTR</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>TPS 78633</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS78633KTTRE3</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>TPS 78633</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS78633KTRRG3</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>TPS 78633</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS78633KTTTT</td>
<td>ACTIVE</td>
<td>DDPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>TPS 78633</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

#### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width** (W1)

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **Pocket Quadrants**

#### PACKAGING INFORMATION

- **Device**
- **Package Type**
- **Drawing**
- **Pins**
- **SPQ**
- **Reel Diameter (mm)**
- **Reel Width W1 (mm)**
- **A0 (mm)**
- **B0 (mm)**
- **K0 (mm)**
- **P1 (mm)**
- **W (mm)**
- **Pin1 Quadrant**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Device Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS76601DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>7.1</td>
<td>7.45</td>
<td>1.88</td>
<td>8.0</td>
<td>12.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS76601DRB</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.3</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76601DRBT</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>3.3</td>
<td>3.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76601KTTR</td>
<td>DDPak/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76618KTTR</td>
<td>DDPak/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76618KTTT</td>
<td>DDPak/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76618KTTRE3</td>
<td>DDPak/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76618KTTT</td>
<td>DDPak/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76625DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>7.1</td>
<td>7.45</td>
<td>1.88</td>
<td>8.0</td>
<td>12.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS76625KTTR</td>
<td>DDPak/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76625KTTT</td>
<td>DDPak/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS76628DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>7.1</td>
<td>7.45</td>
<td>1.88</td>
<td>8.0</td>
<td>12.0</td>
<td>Q3</td>
</tr>
<tr>
<td>Device</td>
<td>Package Type</td>
<td>Package Drawing</td>
<td>Pins</td>
<td>SPQ</td>
<td>Reel Diameter (mm)</td>
<td>Reel Width W1 (mm)</td>
<td>A0 (mm)</td>
<td>B0 (mm)</td>
<td>K0 (mm)</td>
<td>P1 (mm)</td>
<td>W (mm)</td>
<td>Pin1 Quadrant</td>
</tr>
<tr>
<td>-----------------</td>
<td>--------------</td>
<td>----------------</td>
<td>------</td>
<td>-----</td>
<td>--------------------</td>
<td>--------------------</td>
<td>---------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------------</td>
</tr>
<tr>
<td>TPS78628KTTT</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS78630DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>7.1</td>
<td>7.45</td>
<td>1.88</td>
<td>8.0</td>
<td>12.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS78630KTTT</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS78633DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>7.1</td>
<td>7.45</td>
<td>1.88</td>
<td>8.0</td>
<td>12.0</td>
<td>Q3</td>
</tr>
<tr>
<td>TPS78633KTTTR</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS78633KTTRE3</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>TPS78633KTTT</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>15.6</td>
<td>4.9</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS78601DQQR4</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>358.0</td>
<td>335.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS78601DRBR</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS78601DRBT</td>
<td>SON</td>
<td>DRB</td>
<td>8</td>
<td>2500</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS78601KTTR</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78601KTTT</td>
<td>DDPACK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78618DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>358.0</td>
<td>335.0</td>
<td>35.0</td>
</tr>
<tr>
<td>Device</td>
<td>Package Type</td>
<td>Package Drawing</td>
<td>Pins</td>
<td>SPQ</td>
<td>Length (mm)</td>
<td>Width (mm)</td>
<td>Height (mm)</td>
</tr>
<tr>
<td>----------------</td>
<td>----------------</td>
<td>-----------------</td>
<td>------</td>
<td>-----</td>
<td>-------------</td>
<td>------------</td>
<td>-------------</td>
</tr>
<tr>
<td>TPS78618KTTTR</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78618KTTRE3</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78618KTTTT</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78625DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>358.0</td>
<td>335.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS78625KTTTR</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78625KTTT</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78628DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>358.0</td>
<td>335.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS78628KTTT</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78630DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>358.0</td>
<td>335.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS78630KTTT</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78633DCQR</td>
<td>SOT-223</td>
<td>DCQ</td>
<td>6</td>
<td>2500</td>
<td>358.0</td>
<td>335.0</td>
<td>35.0</td>
</tr>
<tr>
<td>TPS78633KTTT</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78633KTTRE3</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>500</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
<tr>
<td>TPS78633KTTTT</td>
<td>DPAK/TO-263</td>
<td>KTT</td>
<td>5</td>
<td>50</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
</tbody>
</table>
DCQ (R-PDSO-G6)  PLASTIC SMALL-OUTLINE

NOTES:  A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Controlling dimension in inches.
D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
E. Lead width dimension does not include dambar protrusion.

Lead width and thickness dimensions apply to solder plated leads.
F. Interlead flash allow 0.008 inch max.
G. Gate burr/protrusion max. 0.006 inch.
H. Datums A and B are to be determined at Datum H.

TEXAS INSTRUMENTS
www.ti.com
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-SM-782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Please refer to the product data sheet for specific via and thermal dissipation requirements.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

4203482–2/K 06/12
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions Diagram]

NOTE: All linear dimensions are in millimeters.
NOTEs: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com.<http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.
MECHANICAL DATA

KTT (R-PSFM-G5)  PLASTIC FLANGE-MOUNT PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0.13) per side.
⚠ Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

4200577-4/G 01/13

Texas Instruments
www.ti.com
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-SM-782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.
   Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.
Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products
- Audio: [www.ti.com/audio](http://www.ti.com/audio)
- Amplifiers: [amplifier.ti.com](http://amplifier.ti.com)
- Data Converters: [dataconverter.ti.com](http://dataconverter.ti.com)
- DLP® Products: [www.dlp.com](http://www.dlp.com)
- DSP: [dsp.ti.com](http://dsp.ti.com)
- Clocks and Timers: [www.ti.com/clocks](http://www.ti.com/clocks)
- Interface: [interface.ti.com](http://interface.ti.com)
- Logic: [logic.ti.com](http://logic.ti.com)
- Power Mgmt: [power.ti.com](http://power.ti.com)
- Microcontrollers: [microcontroller.ti.com](http://microcontroller.ti.com)
- RFID: [www.ti-rfid.com](http://www.ti-rfid.com)
- OMAP Applications Processors: [www.ti.com/omap](http://www.ti.com/omap)
- Wireless Connectivity: [www.ti.com/wirelessconnectivity](http://www.ti.com/wirelessconnectivity)

### Applications
- Automotive and Transportation: [www.ti.com/automotive](http://www.ti.com/automotive)
- Communications and Telecom: [www.ti.com/communications](http://www.ti.com/communications)
- Energy and Lighting: [www.ti.com/energy](http://www.ti.com/energy)
- Industrial: [www.ti.com/industrial](http://www.ti.com/industrial)
- Medical: [www.ti.com/medical](http://www.ti.com/medical)
- Video and Imaging: [www.ti.com/video](http://www.ti.com/video)
- TI E2E Community: [e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated