



# USB1T20 — Universal Serial Bus Transceiver

## Features

- Complies with Universal Serial Bus Specification 2.0 for FS/LS Applications
- Utilizes Digital Inputs and Outputs to Transmit and Receive USB Cable Data
- Supports 12Mbit/s Full Speed (FS) and 1.5Mbit/s Low Speed (LS) Serial Data Transmission
- Supports Single-ended and Differential Data Interface as Function of MODE
- Single 3.3 V Supply
- ESD Performance: Human Body Model
  - 9.5 kV on D-, D+ Pins Only
  - 4.0 kV on All Other Pins

## Description

USB1T20 is a generic USB 2.0 compliant transceiver. Using a single voltage supply, the USB1T20 provides an ideal USB interface solution for any electronic device able to supply 3.0 V to 3.6 V. It is designed to allow 5.0 V or 3.3 V programmable and standard logic to interface with the physical layer of the Universal Serial Bus (USB). It is capable of transmitting and receiving serial data at both full speed (12Mbit/s) and low speed (1.5Mbit/s) data rates.

Packaged in industry-standard TSSOP package. The USB1T20 is ideal for mobile electronics and other space-constrained applications.

## Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
USB1T20MTCX	-40° to +85°C	14-Lead, Thin-Shrink Small-Outline Package (TSSOP) JEDEC MO-153, 4.4mm Wide	Tape and Reel

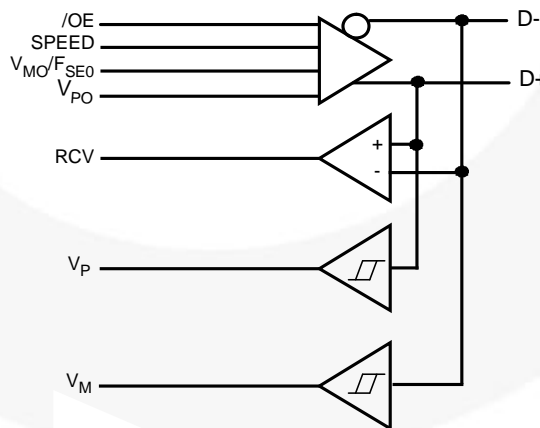


Figure 1. Logic Diagram

## Pin Configuration

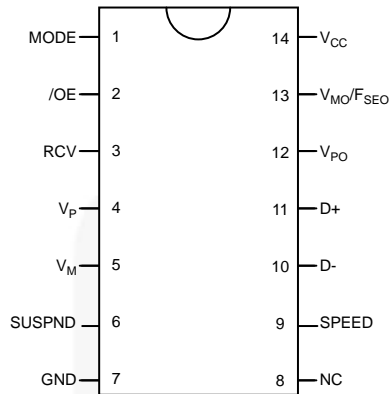


Figure 2. Pin Configuration (Top View)

## Pin Definitions

Pin #	Name	I/O	Description			
1	MODE	I	<b>Mode.</b> When left unconnected, a weak pull-up transistor pulls mode pin to $V_{CC}$ and, in this GND, the $V_{MO}/F_{SEO}$ pin takes the function of $F_{SEO}$ (force SEO).			
2	/OE	I	<b>Output Enable.</b> Active LOW; enables the transceiver to transmit data on the bus. When not active, the transceiver is in receive mode.			
3	RCV	O	<b>Receive Data.</b> CMOS-Level output for USB differential input.			
4, 5	$V_P, V_M$	O	Gated version of D- and D+. Outputs are logic "0" and logic "1." Used to detect single ended zero (/SEO), error conditions, and interconnected speed. (Input to SIE).			
			<b><math>V_P</math></b>	<b><math>V_M</math></b>	<b>RESULT</b>	
			0	0	/SEO	
			0	1	Low Speed	
			1	0	Full Speed	
6	SUSPND	I	<b>Suspend.</b> Enables a low-power state while the USB bus is inactive. While the suspend pin is active, it drives the RCV pin to a logic "0" state. Both D+ and D- are 3-state.			
7	GND		Ground reference.			
8	NC		No connect.			
9	SPEED	I	<b>Edge Rate Control.</b> Logic "1" operates at edge rates for full speed. Logic "0" operates edge rates for low speed.			
10, 11	D-, D+	AI/O	Data+, Data-. Differential data bus conforming to the Universal Serial Bus standard.			
12, 13	$V_{PO}, V_{MO}/F_{SEO}$	I	Inputs to differential driver. (Outputs from SIE.)			
			<b>Mode</b>	<b><math>V_{PO}</math></b>	<b><math>V_{MO}/F_{SEO}</math></b>	<b>RESULT</b>
			0	0	0	Logic "0"
				0	1	/SEO
				1	0	Logic "1"
				1	1	/SEO
			1	0	0	/SEO
				0	1	Logic "0"
				1	0	Logic "1"
1	1	1	Illegal Code			
14	$V_{CC}$		3.0 to 3.6 power supply.			

**Functional Truth Table**

Input					I/O		Outputs			
Mode	V <sub>PO</sub>	V <sub>MO</sub> /F <sub>SEO</sub>	/OE	SUSPND	D+	D-	RCV	V <sub>P</sub>	V <sub>M</sub>	Result
0	0	0	0	0	0	1	0	0	1	Logic "0"
0	0	1	0	0	0	0	Undefined State	0	0	/SEO
0	1	0	0	0	1	0	1	1	0	Logic "1"
0	1	1	0	0	0	0	Undefined State	0	0	/SEO
1	0	0	0	0	0	0	Undefined State	0	0	/SEO
1	0	1	0	0	0	1	0	0	1	Logic "0"
1	1	0	0	0	1	0	1	1	0	Logic "1"
1	1	1	0	0	1	1	Undefined State	Undefined State	Undefined State	Illegal Code
Don't Care	Don't Care	Don't Care	1	0	3-State	3-State	Undefined State	Undefined State	Undefined State	D+/D-Hi-Z
Don't Care	Don't Care	Don't Care	1	1	3-State	3-State	Undefined State	Undefined State	Undefined State	D+/D-Hi-Z

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
$V_{CC}$	DC Supply Voltage	-0.5	7.0	V	
$I_{IK}$	DC Input Diode Current, $V_{IN} < 0$ V		-50	mA	
$V_{IN}$	Input Voltage <sup>(1)</sup>	-0.5	5.5	V	
$V_{I/O}$	Input / Output Voltage	-0.5	$V_{CC} + 0.5$	V	
$I_{OK}$	Output Diode Current, $V_O > V_{CC}$ or $V_O < 0$ V		$\pm 50$	mA	
$V_O$	Output Voltage <sup>(1)</sup>	-0.5	$V_{CC} + 0.5$	V	
$I_O$	Output Source or Sink Current ( $V_O = 0$ to $V_{CC}$ )	$V_P, V_M, RCV$ Pins		$\pm 15$	mA
		D+/D- Pins		$\pm 50$	
$I_{CC} / I_{GND}$	$V_{CC} / GND$ Current		$\pm 100$	mA	
$T_{STG}$	Storage Temperature Range	-60	+150	°C	

### Note:

- The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	3.0	3.6	V
$V_{IN}$	Input Voltage	0	5.5	V
$V_{AI/O}$	Input Range for AI/O	0	$V_{CC}$	V
$V_O$	Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Ambient Temperature, Free Air	-40	+85	°C

## DC Electrical Characteristics Digital Pins

Over the recommended range of supply voltage and operating free air temperature unless otherwise noted.  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ .

Symbol	Parameter	Conditions	$T_A = -40\text{ to }+85^\circ\text{C}$			Units
			Min.	Typ.	Max.	
<b>Input Levels</b>						
$V_{IL}$	Low-Level Input Voltage				0.8	V
$V_{IH}$	High-Level Input Voltage		2			V
<b>Output Levels</b>						
$V_{OL}$	Low-Level Output Voltage	$I_{OL} = 4\text{ mA}$			0.4	V
		$I_{OL} = 20\text{ }\mu\text{A}$			0.1	
$V_{OH}$	High-Level Output Voltage	$I_{OH} = 4\text{ mA}$	2.4			V
		$I_{OH} = 20\text{ }\mu\text{A}$	$V_{CC}-0.1$			
<b>Leakage Current</b>						
$I_{IN}$	Input Leakage Current	$V_{CC} = 3.0\text{ to }3.6\text{ V}$			$\pm 5$	$\mu\text{A}$
$I_{CCFS}$	Supply Current, Full Speed	$V_{CC} = 3.0\text{ to }3.6\text{ V}$			5	mA
$I_{CCLS}$	Supply Current, Low Speed	$V_{CC} = 3.0\text{ to }3.6\text{ V}$			5	mA
$I_{CCQ}$	Quiescent Supply Current	$V_{CC} = 3.0\text{ to }3.6\text{ V}$ , $V_{IN} = V_{CC}\text{ or GND}$			5	mA
$I_{CCS}$	Supply Current in Suspend	$V_{CC} = 3.0\text{ to }3.6\text{ V}$ , Mode = $V_{CC}$			10	$\mu\text{A}$

## DC Electrical Characteristics D+/D- Pins

Over the recommended range of supply voltage and operating free air temperature unless otherwise noted.  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ .

Symbol	Parameter	Conditions	$T_A = -40\text{ to }+85^\circ\text{C}$			Units
			Min.	Typ.	Max.	
<b>Input Levels</b>						
$V_{DI}$	Differential Input Sensitivity	$ (D+) - (D-) $	0.2			V
$V_{CM}$	Differential Common-Mode Range	Includes $V_{DI}$ Range	0.8		2.5	V
$V_{SE}$	Single-Ended Receiver Threshold		0.8		2.0	V
<b>Output Levels</b>						
$V_{OL}$	Static Output Low-Voltage	$R_L$ of $1.5\text{ k}\Omega$ to $3.6\text{ V}$			0.3	V
$V_{OH}$	Static Output High-Voltage	$R_L$ of $1.5\text{ k}\Omega$ to GND	2.8		3.6	V
$V_{CR}$	Differential Crossover		1.3		2.0	V
<b>Leakage Current</b>						
$I_{OZ}$	High-Z State Data Line Leakage Current	$0\text{ V} < V_{IN} < 3.3\text{ V}$			$\pm 5$	$\mu\text{A}$
<b>Capacitance</b>						
$C_{IN}$	Transceiver Capacitance <sup>(2)</sup>	Pin to GND			10	pF
	Capacitance Match <sup>(2)</sup>				10	%
<b>Output Resistance</b>						
$Z_{DRV}$	Driver Output Resistance <sup>(3)</sup>	Steady-State Drive	4		20	$\Omega$
	Resistance Match <sup>(3)</sup>				10	%

### Notes:

- This specification is guaranteed by design and statistical process distribution.
- Excludes external resistor. To comply with USB specification 1.1, external series resistors of  $24\text{ }\Omega \pm 1\%$  each on D+ and D- are recommended.

## AC Electrical Characteristics D+/D- Pins, Full Speed

Over the recommended range of supply voltage and operating free air temperature unless otherwise noted.  
 $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 1.5\text{ k}\Omega$  on D+ to  $V_{CC}$ .

Symbol	Parameter	Conditions	$T_A = -40\text{ to }+85^\circ\text{C}$			Units
			Min.	Typ.	Max.	
<b>Driver Characteristics</b>						
$t_R, t_F$	Rise and Fall Time	10 and 90%, Figure 3	4		20	ns
$t_{RFM}$	Rise/Fall Time Matching	$t_r / t_f$	90		110	%
$V_{CRS}$	Output Signal Crossover Voltage		1.3		2.0	V
<b>Driver Timings</b>						
$t_{PLH}$	Driver Propagation Delay ( $V_{PO}, V_{MO}/F_{SEO}$ to D+/D-)	Figure 4			18	ns
$t_{PHZ}, t_{PLZ}$	Driver Disable Delay (/OE to D+/D-)	Figure 6			13	ns
$t_{PZH}, t_{PZL}$	Driver Enable Delay (/OE to D+/D-)	Figure 6			17	ns
<b>Receiver Timings</b>						
$t_{PLH}$	Receiver Propagation Delay D+/D- to RVC	Figure 5			16	ns
$t_{PHL}$					19	ns
$t_{PLH}, t_{PHL}$	Single-ended Receiver Delay (D+, D- to $V_P, V_M$ )	Figure 5			8	ns

## AC Electrical Characteristics D+/D- Pins, Low Speed

Over the recommended range of supply voltage and operating free air temperature unless otherwise noted.  
 $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ;  $C_L = 200\text{ pF to }600\text{ pF}$ ;  $R_L = 1.5\text{ k}\Omega$  on D- to  $V_{CC}$ .

Symbol	Parameter	Conditions	$T_A = -40\text{ to }+85^\circ\text{C}$			Units
			Min.	Typ.	Max.	
<b>Driver Characteristics</b>						
$t_{LR}, t_{LF}$	Rise and Fall Time	10 and 90%, Figure 3	75		300	ns
$t_{RFM}$	Rise/Fall Time Matching	$t_r / t_f$	80		120	%
$V_{CRS}$	Output Signal Crossover Voltage		1.3		2.0	V
<b>Driver Timings</b>						
$t_{PLH}, t_{PHL}$	Driver Propagation Delay ( $V_{PO}, V_{MO}/F_{SEO}$ to D+/D-)	Figure 4			300	ns
$t_{PHZ}, t_{PLZ}$	Driver Disable Delay (/OE to D+/D-)	Figure 6			13	ns
$t_{PZH}, t_{PZL}$	Driver Enable Delay (/OE to D+/D-)	Figure 6			205	ns
<b>Receiver Timings</b>						
$t_{PLH}, t_{PHL}$	Receiver Propagation Delay (D+/D- to RVC)	Figure 5			18	ns
$t_{PLH}, t_{PHL}$	Single-ended Receiver Delay (D+, D- to $V_P, V_M$ )	Figure 5			28	ns

### AC Loadings and Waveforms

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drops that occur with the output load.  $V_{CC}$  never goes below 3.0 V.

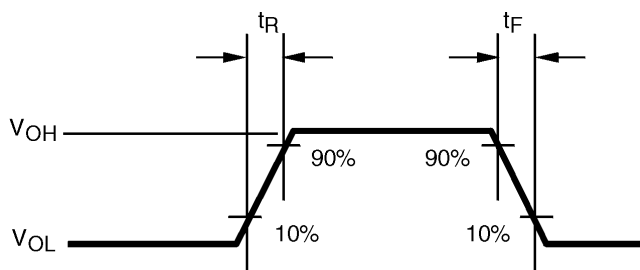


Figure 3. Rise and Fall Times

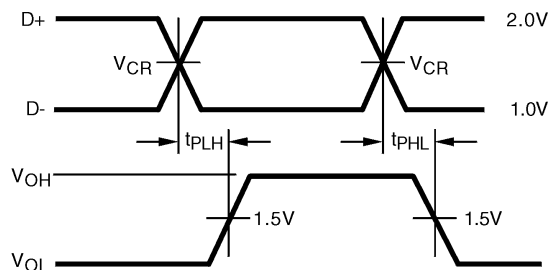


Figure 4.  $V_{PO}$ ,  $V_{MO}/F_{SEO}$  to D+/D-

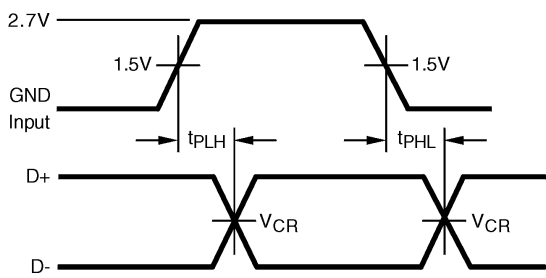


Figure 5. D+/D- to RCV,  $V_F/V_M$

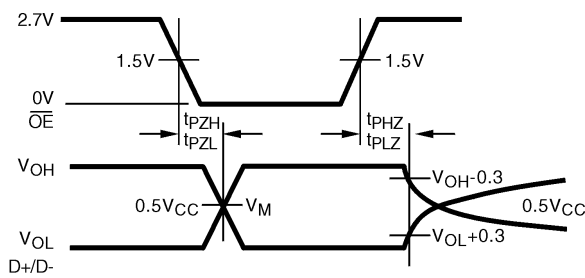


Figure 6. /OE to D+/D-

### Test Circuits and Waveforms

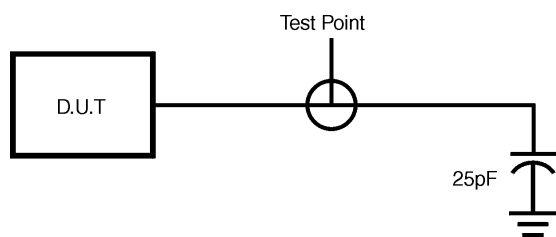


Figure 7. Load for  $V_M/V_P$  and RCV

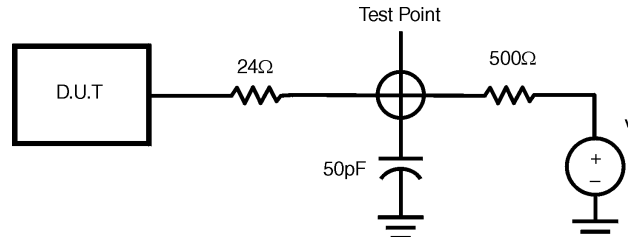
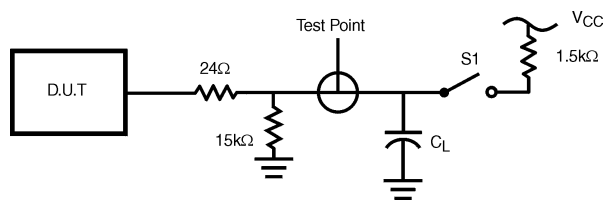


Figure 8. Load for Enable and Disable Times



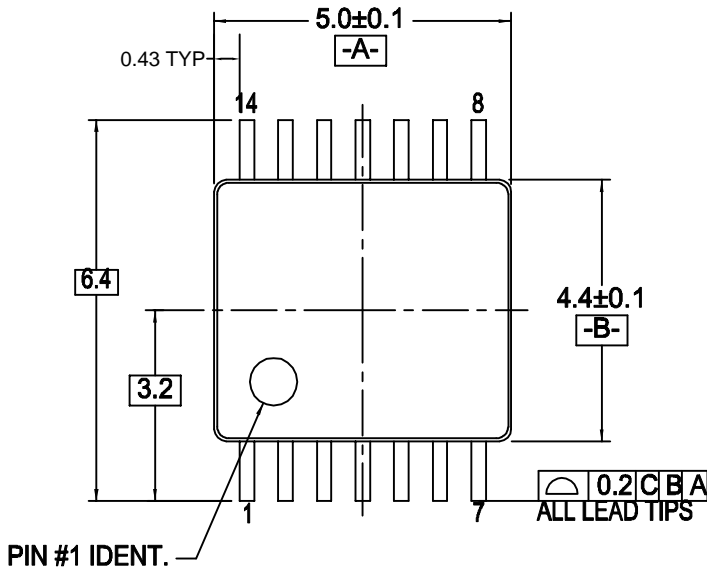
Test	S1
D-/LS	Close
D+/LS	Open
D-/FS	Open
D+/FS	Close

$C_L=50\text{pF}$ , Full Speed  
 $C_L=200\text{pF}$ , Low Speed (Minimum Timing)  
 $C_L=600\text{pF}$ , Low Speed (Maximum Timing)  
 1.5kΩ on D- (Low Speed) or D+ (Full Speed) only

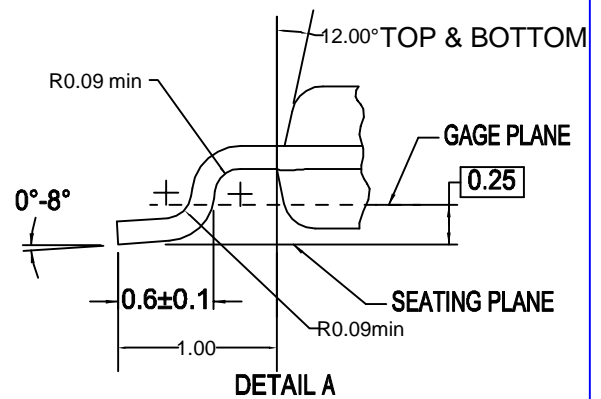
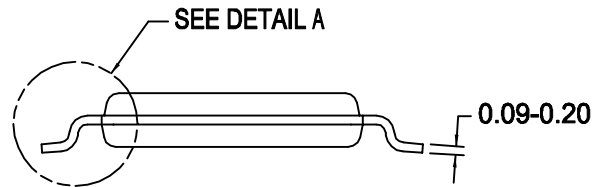
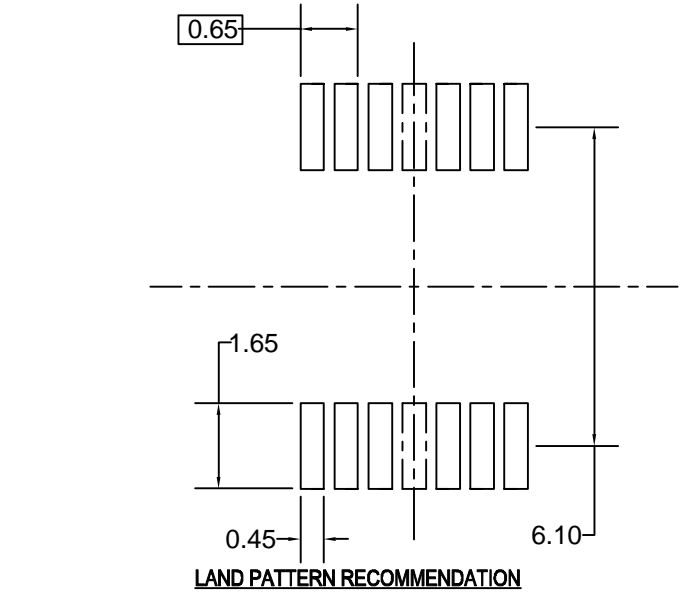
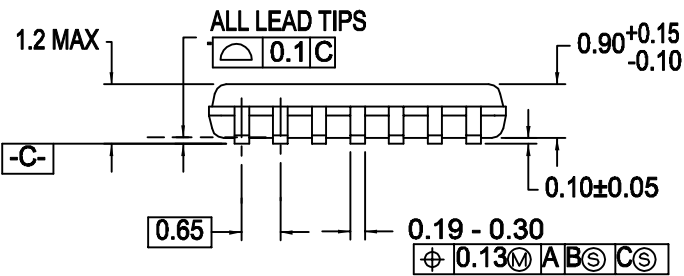
Figure 9. Load for D+/D-

**REVISIONS**

LTR	DESCRIPTION	E.C.N.	DATE	BY/APPD
C	REVISE & REDRAW ON PRO/E PER CURRENT STD; CORRECT DET CALLOUT FROM D TO A	11099	08/21/95	MS/
C1	CHANGE TO (FSPM) DRAWING		4-6-98	FEITAN
C2	ADDED NOTES SECTION, ADDED RADIUS DIMS, MOLDED BODY ANGLE DIMS, AND FILENAME		6-12-98	H.ALLEN
C3	CHANGED TITLE, ADDED TITLE		6-23-98	H.ALLEN
D	CHANGED REVISION LEVEL ONLY		11/12/04	H.ALLEN
6	UPDATED LAND PATTERN		9 JULY 07	L.HUEBENER



PIN #1 IDENT.



**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

<b>APPROVALS</b>	<b>DATE</b>	<b>FAIRCHILD</b> SEMICONDUCTOR™
DRAWN L.HUEBENER	9 JULY 07	
DFTG. CHK. H.ALLEN	31 JULY 07	14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE
ENGR. CHK.		
		SCALE N/A
		SIZE C
		DRAWING NUMBER MKT-MTC14
		REV 6
		DO NOT SCALE DRAWING
		SHEET 1 of 1





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SerDes®  
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**Definition of Terms**

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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