

TWR-LS1021A Getting Started

1 Introduction

This document explains how to connect the *QorIQ LS1021A Tower System Module (TWR-LS1021A)* board and verify its basic operations like, the switches, connectors, jumpers, push buttons and LED settings, and the instructions for connecting the peripheral devices.

NOTE

It is assumed that you are familiar with the LS1021A device and the content of the *TWR-LS1021A Reference Manual (TWR-LS1021ARM)*.

The following figures shows the main features of the secondary and primary side of the TWR-LS1021A board.

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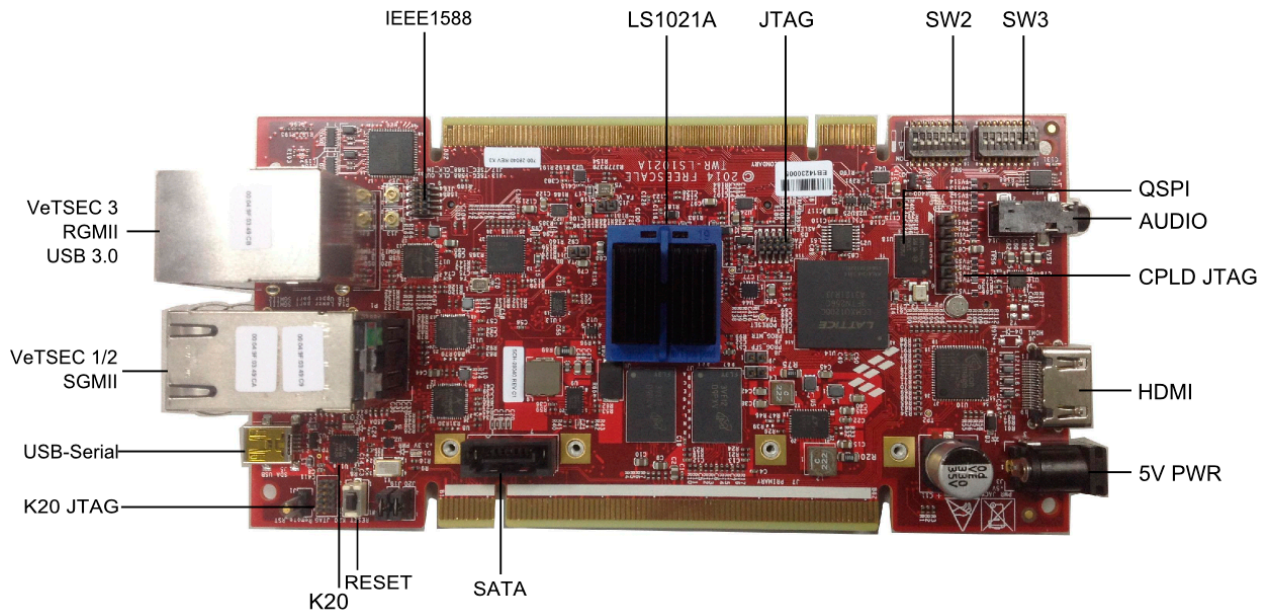


Figure 1. Primary side main features

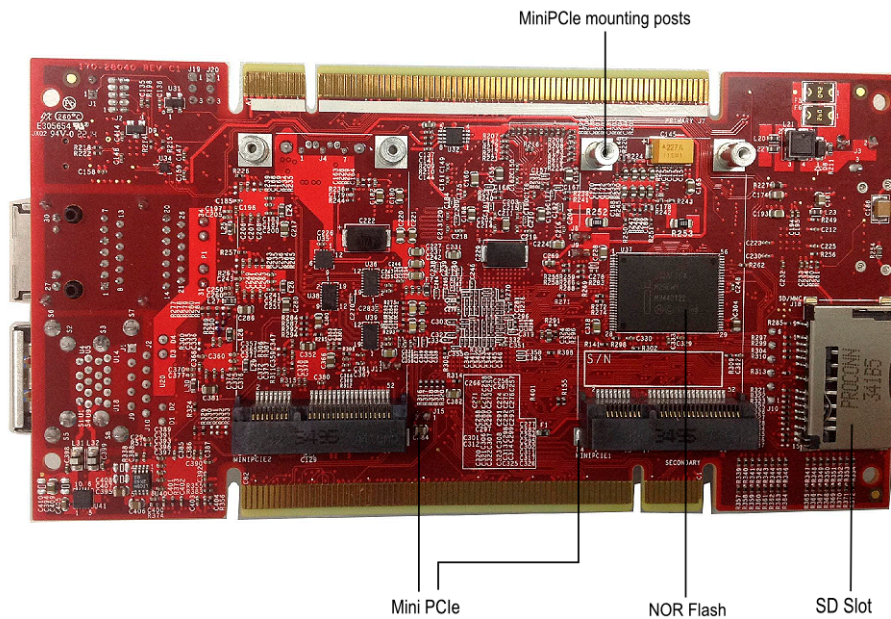


Figure 2. Secondary side main features

1.1 Related documentation

The following table lists and explains the additional documents and resources that you can refer, for more information on TWR-LS1021A board.

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1. Related documentation

Document	Description
LS1021A QorIQ Advanced Multicore Processor Data Sheet	Provides information about electrical characteristics, hardware design considerations, pin assignments, package information, and ordering information.
LS1021A QorIQ Integrated Multicore Processor Reference Manual (LS1021ARM)	Provides a detailed description about LS1021A QorIQ multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information.
The SystemID Format for Power Architecture™ Development Systems (AN3638)	Freescale Semiconductor Power Architecture™ technology-based evaluation and development platforms may optionally implement a “System ID” non-volatile memory device. This device stores important configuration data about the board.
TWR-LS1021A Reference Manual (TWR-LS1021ARM)	Provides a detailed description of the architecture, tower elevator connections, CPLD system controller architecture, board configuration and debug support for TWR-LS1021A QorIQ Tower System.

2 Switches and jumpers configuration

The TWR-LS1021A board have two 8-way dual in line package (DIP) switch. The default DIP switch positions provide working set up values for the board. Check the default positions and verify the board is operational before changing the switches. Figure 3 shows the settings for the switches with their default positions.

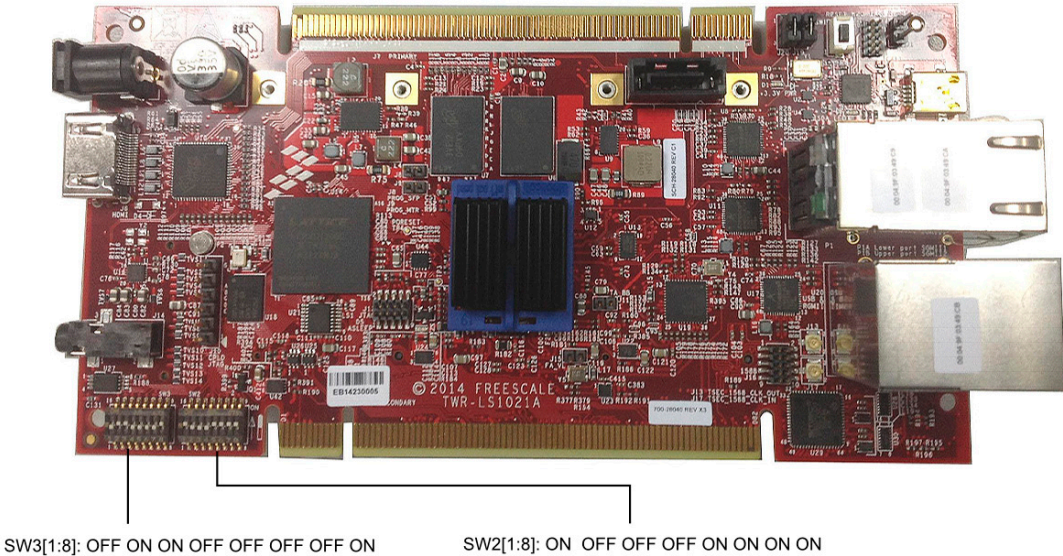


Figure 3. Default switch configuration

Table 2-2 lists and describes the default switch configuration for TWR-LS1021A board.

Table 2-2. Default switch settings

Feature	Settings [OFF=0 ON=1]	Option	Comments
S2.1	ON	RCW Source is NOR	NOR RCW_SEL 0 : NOR disabled »1 : NOR enabled(default)
S2.2	OFF	Reserved	Must be 0 [OFF]
S2.3	OFF	RCW Source is SDHC	SDHC RCW_SEL »0 : SDHC disabled (default) 1 : SDHC enabled
S2.4	OFF	RCW Source is QSPI	QSPI RCW_SEL »0 : QSPI disabled (default) 1 : QSPI enabled
S2.5	ON	Bus select is NOR or QSPI	IFC/QSPI Bus selection 0 : IFC disabled, QSPI enabled »1 : IFC enabled, QSPI disabled (default)
S2.6	ON	LVDD&L1VDD selection is 2.5V or 3.3V	LVDD&L1VDD Voltage Selection 0 : 3.3V »1 : 2.5V (default)
S2.7	ON	IFC_CS1 or SPI1_PCS0 selection	IFC_CS1/SPI1_PCS0 Selection 0 : IFC_CS1 disabled, SPI1_PCS0 enabled »1 : IFC_CS1 enabled, SPI1_PCS0 disabled (default)
S2.8	ON	DIPSW_IN1	SDA_SWD_EN Control 0 : use K20 IO pin to control SDA_SWD_EN »1 : tied to high to disable MBED connection (default)
S3.1	OFF	96MHz SYSCLK select or not	96MHz SYSCLK Selection »0 : Do not select 96MHz as SYSCLK(default) 1 : Select 96MHz as SYSCLK
S3.2	ON	TEST_SEL_DRV	Drive TEST_SEL signal 0 : non-compliant mode to support boundary scan. » 1 : JTAG compliant mode(default)
S3.3	ON	CLKGEN_FS0 System clock frequency setting	CLKGEN_FS[0:1] 00 = 66.66MHz 01 = 80.00MHz »10 = 100.00MHz (default) 11 = 83.33MHz
S3.4	OFF	CLKGEN_FS1 System clock frequency setting	
S3.5	OFF	NOR Bank Select BANK_SEL	BANK_SEL » 0 : Vbank0 (default) 1 : Vbank1

Table 2-2. Default switch settings

Feature	Settings [OFF=0 ON=1]	Option	Comments
S3.6	OFF	Signal multiplexed selection MUX_SEL	MUX_SEL » 0 : PCIE1,SGMII1,PCIE2,SGMII2, RGMII, CAN3&4, SAI1&2, LCD, LPUART1(default) 1 : PCIE1,SATA,PCIE2,SGMII2, RGMII, CAN3&4, CAN1&2, UCC1&3, SPI2
S3.7	OFF	Reserved	Must be 0 [OFF]
S3.8	ON	Reserved	Must be 1 [ON]

Table 2-3 lists the jumper settings.

Table 2-3. Jumper settings

Jumper	Setting	
	UART1 console (default)	LPUART1 console
J19	2-3	1-2
J20	2-3	1-2
Others Jumpers	Open	Open

Figure 4 shows the jumper settings.

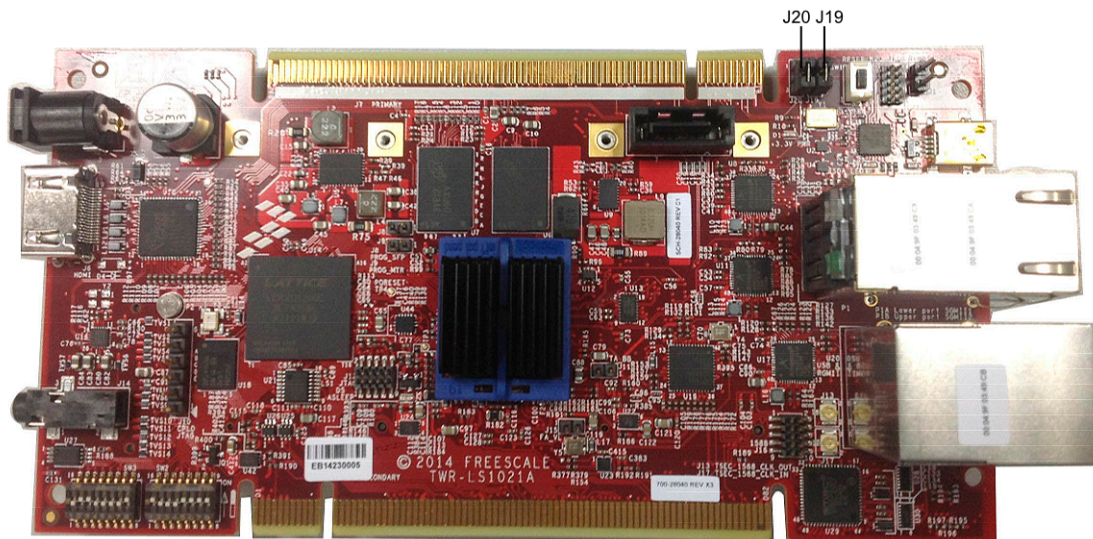


Figure 4. Jumper settings

3 Connecting USB UART

The TWR-LS1021A board comes preloaded with u-boot only. Serial connectivity for TWR-LS1021A board is provided through the mini type B USB connector.

NOTE

You need to install the USB drivers on the host PC before using the serial terminal. You can get the drivers from the USB memory stick available in the box, *or*, you can download these drivers from,

<https://mbed.org/handbook/Windows-serial-configuration>

After installing the drivers, set up a serial terminal using a PC communication program such as hyper terminal set to 115200-8-N-1. Then, select the first COM port assigned to the Virtual COM port.

4 Initial board power-up

The TWR-LS1021A board is powered through a barrel connector. This barrel should be supplied by a 5V @5A supply. See [Figure 2](#).

NOTE

It is normal for heatsink on the TWR-LS1021A board to become hot under standard operating conditions.

To perform initial board power-up and LED check, follow the steps listed below:

1. Power-up the board through barrel connector.
2. Check for the completion of the reset sequence indicated by the LEDs (see [Figure 2](#) for locations). [Table 4-4](#) lists a full description of the LED operation.
3. On powering up the board:
 - a) The LED D1 turns ON to indicate 3V3 power is present.
 - b) D5 turns ON then OFF.
 - c) Any Ethernet activity is indicated by the LEDs on the RJ45 connector.
 - d) D2 indicates MBED USB driver is loaded. If it is blinking, than the serial port is not available. You need to power up the board at J3, than insert the USB cable on board.

The following table lists the LED operations.

Table 4-4. LED operation

Description	Ref	Color	LED On	LED Off
3V3 Power	D1	Green	3V3 Power ON	3V3 Power OFF
LS1021A ASLEEP	D5	Green	ASLEEP	Out of asleep
MBED status	D2	Green	MBED driver is loaded	MBED driver is not loaded
Ethernet eTSEC1	P1 down	Green/Orange	ON – Link Blink - Activity	No Link

Table 4-4. LED operation

Description	Ref	Color	LED On	LED Off
Ethernet eTSEC2	P1 up	Green/Orange	ON – Link Blink - Activity	No Link
Ethernet eTSEC3	U20 up (above USB)	Green/Orange	ON – Link Blink - Activity	No Link

5 Board software configuration

The NOR flash on TWR-LS1021A board is divided into two banks. There are different images in each bank that supports different functionality.

The bank0 is programmed with RCW support for QE, and the bank1 is programmed with the RCW support for DCU. The default is bank0.

The board boots from bank0 by default with the following switch and jumper settings:

Table 5-5. Switch and jumper settings for bank0

Switch	Jumper	Configuration
SW3[5]=OFF	J19	Jumper in position 2-3: uart
	J20	Jumper in position 2-3: uart

To boot from bank1 to enable the DCU, use the following switch and jumper settings:

Table 5-6. Switch and jumper settings for bank1

Switch	Jumper	Configuration
SW3[5]=ON	J19	Jumper in position 1-2: Lpuart
	J20	Jumper in position 1-2: Lpuart

NOTE

If you enable the DCU, you have to use lpuart as console. The bootup information displays on lpuart console by default. For more information on how to enable the DCU output, refer to the *DCU Display Device Driver User Manual*, available in the following Yocto source ISO folder:

LS1021A-SDK-V1.2-ARM-SOURCE-20140829-yocto.iso\documents

The DCU boot log shows the DDR frequency as 528M and 1056MT/s, this is a known display error. On the board with 100M DDR clock, the actual frequency is 800M and 1600MT/s.

6 Connecting JTAG connectivity unit

The JTAG connectivity unit (CW TAP) enables the Freescale CodeWarrior software to work with the board.

1. Connect the JTAG connectivity unit to the LS1021A JTAG connector J12. Pin 1 is marked on the board.
2. Switch ON the power to the board.
3. Check for completion of the reset sequence (see [Initial board power-up](#)). Ensure D5 turns OFF.
4. Follow the on-screen instructions.

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