M24C64S-FCU

64-Kbit serial I²C bus EEPROM 4 balls CSP

Datasheet - preliminary data

Features

- Compatible with the 400 kHz I²C protocol
- Memory array:
  - 64 Kbits (8 Kbytes) of EEPROM
  - Page size: 32 bytes
- Supply voltage range:
  - 1.7 V to 5.5 V
- Operating temperature range
  - $V_{CC} = 1.7$ V: -40°C / +85°C
  - $V_{CC} = 1.6$ V: -40°C (Read) / 0°C (Write) / +85°C
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Random and sequential read modes
- Software Write protect
  - Upper quarter memory array
  - Upper half memory array
  - Upper 3/4 memory array
  - Whole memory array
- ESD protection
  - Human Body Model: 4 kV
- More than 1 million Write cycles
- More than 40-year data retention
- Package
  - WLCSP, RoHS and Halogen free compliant (ECOPACK®2)
Contents

1 Description ................................................................. 6

2 Signal description ....................................................... 7
   2.1 Serial Clock (SCL) ................................................. 7
   2.2 Serial Data (SDA) .................................................... 7
   2.3 VSS (ground) ........................................................ 7
   2.4 Supply voltage (VCC) .............................................. 7
      2.4.1 Operating supply voltage (VCC) ......................... 7
      2.4.2 Power-up conditions ........................................ 7
      2.4.3 Device reset .................................................. 7
      2.4.4 Power-down conditions ..................................... 8

3 Memory organization .................................................... 9

4 Device operation ........................................................ 10
   4.1 Start condition .................................................... 11
   4.2 Stop condition ..................................................... 11
   4.3 Data input .......................................................... 11
   4.4 Acknowledge bit (ACK) ........................................... 11
   4.5 Device addressing ................................................ 12

5 Instructions .............................................................. 13
   5.1 Write operations .................................................. 13
      5.1.1 Byte Write ................................................... 14
      5.1.2 Page Write ................................................... 15
      5.1.3 Write protection ............................................. 16
      5.1.4 Minimizing Write delays by polling on ACK ........... 17
   5.2 Read operations ................................................... 18
      5.2.1 Random Address Read ...................................... 18
      5.2.2 Current Address Read ....................................... 19
      5.2.3 Sequential Read ............................................. 19
      5.2.4 Read the Write Protect register ......................... 19

6 Initial delivery state .................................................. 19
<table>
<thead>
<tr>
<th>Page</th>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Maximum rating</td>
<td>20</td>
</tr>
<tr>
<td>8</td>
<td>DC and AC parameters</td>
<td>21</td>
</tr>
<tr>
<td>9</td>
<td>Package mechanical data</td>
<td>25</td>
</tr>
<tr>
<td>10</td>
<td>Part numbering</td>
<td>27</td>
</tr>
<tr>
<td>11</td>
<td>Revision history</td>
<td>28</td>
</tr>
</tbody>
</table>
List of tables

Table 1. Signal names ................................................................. 6
Table 2. Device select code ...................................................... 12
Table 3. Most significant address byte ....................................... 13
Table 4. Least significant address byte ................................. 13
Table 5. Write Protect register (Address = 1xxx.xxxx.xxxx.xxxx) ... 16
Table 6. Absolute maximum ratings .......................................... 20
Table 7. Test conditions ............................................................. 21
Table 8. Operating conditions .................................................. 21
Table 9. DC characteristics ....................................................... 22
Table 10. 400 kHz AC characteristics ....................................... 23
Table 11. WLCSP 4-bump wafer-level chip-scale package mechanical data .................................................. 26
Table 12. Ordering information scheme ..................................... 27
Table 13. Document revision history ........................................ 28
List of figures

Figure 1. Logic diagram ................................................................. 6
Figure 2. 4-bump WLCSP connections
           (top view, marking side, with balls on the underside) .................. 6
Figure 3. Block diagram ............................................................ 9
Figure 4. \textsuperscript{2}C bus protocol ........................................ 10
Figure 5. Write mode sequence (data write enabled) .......................... 14
Figure 6. Write mode sequence (data write inhibited) ........................ 15
Figure 7. Write cycle polling flowchart using ACK ............................ 17
Figure 8. Read mode sequences .................................................. 18
Figure 9. Maximum R\textsubscript{bus} value versus bus parasitic capacitance (C\textsubscript{bus}) for
           an \textsuperscript{2}C bus at maximum frequency f\textsubscript{C} = 400 kHz .......... 24
Figure 10. AC waveforms ......................................................... 24
Figure 11. WLCSP 4-bump wafer-level chip-scale package outline .......... 25
Figure 12. WLCSP 4-bump wafer-level chip-scale package recommended land pattern .... 26
1 Description

The M24C64S-FCU is a 64-Kbit I2C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 8 K × 8 bits.

The M24C64S-FCU can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C/+85 °C and with an extended supply voltage from 1.6 V to 5.5 V, over a reduced ambient temperature range.

The M24C64S-FCU is delivered in a 4-ball WLCSP package.

![Figure 1. Logic diagram](MS33355V1)

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Function</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDA</td>
<td>Serial Data</td>
<td>I/O</td>
</tr>
<tr>
<td>SCL</td>
<td>Serial Clock</td>
<td>Input</td>
</tr>
<tr>
<td>V_{CC}</td>
<td>Supply voltage</td>
<td></td>
</tr>
<tr>
<td>V_{SS}</td>
<td>Ground</td>
<td></td>
</tr>
</tbody>
</table>

![Figure 2. 4-bump WLCSP connections](MS30749V3)
2 Signal description

2.1 Serial Clock (SCL)
SCL is an input. The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial Data (SDA)
SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR’ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to VCC (Figure 9 indicates how to calculate the value of the pull-up resistor).

2.3 VSS (ground)
VSS is the reference for the VCC supply voltage.

2.4 Supply voltage (VCC)
2.4.1 Operating supply voltage (VCC)
Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified \([V_{CC}^{\text{min}}, V_{CC}^{\text{max}}]\) range must be applied (see Operating conditions in Section 8: DC and AC parameters). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually from 10 nF to 100 nF) close to the VCC/VSS package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle \(t_W\).

2.4.2 Power-up conditions
The VCC voltage has to rise continuously from 0 V up to the minimum VCC operating voltage (see Operating conditions in Section 8: DC and AC parameters) and the rise time must not vary faster than 1 V/µs.

2.4.3 Device reset
In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until VCC has reached the internal reset threshold voltage. This threshold is lower than the minimum VCC operating voltage (see Operating conditions in Section 8: DC and AC parameters). When VCC passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until VCC reaches a valid and stable DC voltage within the specified \([V_{CC}^{\text{min}}, V_{CC}^{\text{max}}]\) range (see Operating conditions in Section 8: DC and AC parameters).
In a similar way, during power-down (continuous decrease in $V_{CC}$), the device must not be accessed when $V_{CC}$ drops below $V_{CC}(\text{min})$. When $V_{CC}$ drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

2.4.4 Power-down conditions

During power-down (continuous decrease in $V_{CC}$), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).
3 Memory organization

The memory is organized as shown below.

**Figure 3. Block diagram**

![Block diagram of memory organization](image-url)
Device operation

The device supports the $I^2C$ protocol. This is summarized in Figure 4. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 4. $I^2C$ bus protocol
4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9\textsuperscript{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.
4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in Table 2 (on Serial Data (SDA), most significant bit first).

**Table 2. Device select code**

<table>
<thead>
<tr>
<th>Device type identifier(1)</th>
<th>Chip Enable address</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>b7</td>
<td>b6</td>
<td>b5</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

1. The most significant bit, b7, is sent first.

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time.

If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode (therefore will not acknowledge the device select code).
5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/W bit (R/W) reset to 0. The device acknowledges this, as shown in Figure 5, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

<table>
<thead>
<tr>
<th>A15</th>
<th>A14</th>
<th>A13</th>
<th>A12</th>
<th>A11</th>
<th>A10</th>
<th>A9</th>
<th>A8</th>
</tr>
</thead>
</table>

Table 3. Most significant address byte

<table>
<thead>
<tr>
<th>A7</th>
<th>A6</th>
<th>A5</th>
<th>A4</th>
<th>A3</th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
</tr>
</thead>
</table>

Table 4. Least significant address byte

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the “10th bit” time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle tW is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle (tW), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.
5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, the device replies with NoAck, and the location is not modified, as shown in Figure 6. If, instead, the addressed location is not Write-protected, the device replies with Ack, as shown in Figure 5. The bus master shall terminate the transfer by generating a Stop condition.

Figure 5. Write mode sequence (data write enabled)
5.1.2 Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A15/A5, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 32 bytes of data, each of which is acknowledged by the device if the page is not write-protected, as shown in Figure 5. If the page is write-protected, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in Figure 6. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 6. Write mode sequence (data write inhibited)
5.1.3 Write protection

By writing specific values in a register (Table 5) located at address 1xxx.xxxx.xxxx.xxxxb, the memory array can be write-protected by blocks, which size can be defined as:

- the upper quarter memory array
- the upper half memory array
- the upper 3/4 memory array
- the whole memory array

Table 5. Write Protect register (Address = 1xxx.xxxx.xxxx.xxxxb)

<table>
<thead>
<tr>
<th>b7</th>
<th>b6</th>
<th>b5</th>
<th>b4</th>
<th>b3</th>
<th>b2</th>
<th>b1</th>
<th>b0</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>Write protect activation</td>
<td>Size of write protected block</td>
<td>Size of write protected block</td>
<td>Write protect lock</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: Location 1xxx.xxxx.xxxx.xxxxb is outside of the addressing field of the EEPROM memory (16 Kbytes are addressed within the 00xx.xxxx.xxxx.xxxx range)

- Bit b3 enables or disables the Write protection
  - b3=0: the whole memory can be written (no Write protection)
  - b3=1: the concerned block is write-protected
- Bits b2 and b1 define the size of the memory block to be protected against write instructions
  - b2,b1=0,0: the upper quarter of memory is write-protected
  - b2,b1=0,1: the upper half memory is write-protected
  - b2,b1=1,0: the upper 3/4 of memory are write-protected
  - b2,b1=1,1: the whole memory is write-protected
- bit b0 locks the write protect status
  - b0=0: bits b3,b2,b1,b0 can be modified
  - b0=1: bits b3,b2,b1,b0 cannot be modified and therefore the memory write protection is frozen.
- b7, b6, b5, b4 bits are Don't Care bits.

Writing the Write Protect register

Writing in the Write protect register is performed with a Byte Write instruction at address 1xxx.xxxx.xxxx.xxxxb. Bits b7,b6,b5,b4 of the data byte are not significant (Don't Care).

Writing more than one byte will discard the write cycle (Write protect register content will not be changed).
5.1.4 Minimizing Write delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in AC characteristics tables in Section 8: DC and AC parameters, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 7, is:
- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 7. Write cycle polling flowchart using ACK

1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).
5.2 Read operations

Read operations are performed independently of the Write protection state.

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 8. Read mode sequences

5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 8) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.
5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 8, without acknowledging the byte.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 8.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

5.2.4 Read the Write Protect register

Reading the Write Protect register is performed with a Random Read instruction at address 1xxx.xxxx.xxxx.xxxxb. Bits b7, b6, b5, b4 of the Write Protect register content are read as 0, 0, 0, 0. The signification of the Protect Register lower bits b3, b2, b1, b0 are defined in Section 5.1.3: Write protection.

Reading more than one byte will loop on reading the Write Protect Register value.

The Write Protect register cannot be read while a write cycle (t_w) is ongoing.

6 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh) and the Write Protect register set to 0 (00h).
7 Maximum rating

Stressing the device outside the ratings listed in Table 6 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Ambient operating temperature</td>
<td>–40</td>
<td>130</td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage temperature</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TLEAD</td>
<td>Lead temperature during soldering</td>
<td>see</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>VIO Input or output range</td>
<td>–0.50</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>IOL</td>
<td>DC output current (SDA = 0)</td>
<td></td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>–0.50</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>VESD</td>
<td>Electrostatic pulse (Human Body model)</td>
<td></td>
<td>4000</td>
<td>V</td>
</tr>
</tbody>
</table>

1. Compliant with JEDEC standard J-STD-020D (for small-body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

### Table 7. Test conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data retention</td>
<td>TA = 55 °C</td>
<td>40</td>
<td>year</td>
</tr>
<tr>
<td>Cycling</td>
<td>TA = 25 °C</td>
<td>1 million</td>
<td>cycle</td>
</tr>
</tbody>
</table>

1. The data retention behavior is checked in production. The 40-year limit is defined from characterization and qualification results.

### Table 8. Operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Supply voltage</td>
<td>1.60</td>
<td>1.70</td>
<td>5.5 V</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>Ambient operating temperature: READ</td>
<td>–40</td>
<td>–40</td>
<td>85 °C</td>
</tr>
<tr>
<td></td>
<td>Ambient operating temperature: WRITE</td>
<td>0</td>
<td>–20</td>
<td>85 °C</td>
</tr>
<tr>
<td>f&lt;sub&gt;C&lt;/sub&gt;</td>
<td>Operating clock frequency</td>
<td>–</td>
<td>–</td>
<td>400 kHz</td>
</tr>
</tbody>
</table>
Table 9. DC characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{LI})</td>
<td>Input leakage current (SCL, SDA)</td>
<td>(V_{IN} = V_{SS} ) or (V_{CC}) device in Standby mode</td>
<td>-</td>
<td>(\pm 2)</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{LO})</td>
<td>Output leakage current</td>
<td>SDA in Hi-Z, external voltage applied on SDA: (V_{SS}) or (V_{CC})</td>
<td>-</td>
<td>(\pm 2)</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{CC})</td>
<td>Supply current (Read) (f_c = 400\ kHz)</td>
<td>-</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{CC0})</td>
<td>Supply current (Write)</td>
<td>During (t_W)</td>
<td>-</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{CC1})</td>
<td>Standby supply current</td>
<td>Device not selected (^{(1)}), (V_{IN} = V_{SS} ) or (V_{CC}), (V_{CC} = 1.8\ V)</td>
<td>-</td>
<td>1</td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Device not selected (^{(1)}), (V_{IN} = V_{SS} ) or (V_{CC}), (V_{CC} = 2.5\ V)</td>
<td>-</td>
<td>2</td>
<td>(\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Device not selected (^{(1)}), (V_{IN} = V_{SS} ) or (V_{CC}), (V_{CC} = 5.5\ V)</td>
<td>-</td>
<td>3</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Input low voltage (SCL, SDA)</td>
<td>(-0.45)</td>
<td>(0.25 V_{CC})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>Input high voltage (SCL, SDA)</td>
<td>(0.75 V_{CC})</td>
<td>(V_{CC} + 1)</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Output low voltage</td>
<td>(I_{OL} = 1\ mA, V_{CC} &lt; 1.8\ V)</td>
<td>-</td>
<td>(0.2 V_{CC})</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(I_{OL} = 2.1\ mA, V_{CC} = 2.5\ V)</td>
<td>-</td>
<td>(0.4 V_{CC})</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(I_{OL} = 3\ mA, V_{CC} = 5.5\ V)</td>
<td>-</td>
<td>(0.4 V_{CC})</td>
<td>V</td>
</tr>
</tbody>
</table>

1. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle \(t_W\) (\(t_W\) is triggered by the correct decoding of a Write instruction).
### Table 10. 400 kHz AC characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Alt.</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_C )</td>
<td>( f_{SCL} )</td>
<td>Clock frequency</td>
<td>-</td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>( t_{CHCL} )</td>
<td>( t_{HIGH} )</td>
<td>Clock pulse width high</td>
<td>600</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CLCH} )</td>
<td>( t_{LOW} )</td>
<td>Clock pulse width low</td>
<td>1300</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{QL1QL2} )</td>
<td>( t_F )</td>
<td>SDA (out) fall time</td>
<td>20</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{XH1XL2} )</td>
<td>( t_R )</td>
<td>Input signal rise time</td>
<td>(3)</td>
<td>(3)</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DXC} )</td>
<td>( t_{SU:DAT} )</td>
<td>Data in set up time</td>
<td>100</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CLD} )</td>
<td>( t_{HD:DAT} )</td>
<td>Data in hold time</td>
<td>0</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CLQX} )</td>
<td>( t_{DH} )</td>
<td>Data out hold time</td>
<td>50</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CLQV} )</td>
<td>( t_{AA} )</td>
<td>Clock low to next data valid (access time)</td>
<td>-</td>
<td>900</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CHDL} )</td>
<td>( t_{SU:STA} )</td>
<td>Start condition setup time</td>
<td>600</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DLCL} )</td>
<td>( t_{HD:STA} )</td>
<td>Start condition hold time</td>
<td>600</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CHDH} )</td>
<td>( t_{SU:STO} )</td>
<td>Stop condition set up time</td>
<td>600</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DHDL} )</td>
<td>( t_{BUF} )</td>
<td>Time between Stop condition and next Start condition</td>
<td>1300</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_W )</td>
<td>( t_{WR} )</td>
<td>Write time</td>
<td>-</td>
<td>5</td>
<td>ms</td>
</tr>
<tr>
<td>( t_{NS} )</td>
<td></td>
<td>Pulse width ignored (input filter on SCL and SDA) - single glitch</td>
<td>-</td>
<td>50</td>
<td>ns</td>
</tr>
</tbody>
</table>

1. Characterized only, not tested in production.
2. With \( C_L = 10 \) pF.
3. There is no min. or max. value for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when \( f_C < 400 \) kHz.
4. The min value for \( t_{CLQX} \) (Data out hold time) offers a safe timing to bridge the undefined region of the falling edge SCL.
5. \( t_{CLQV} \) is the time (from the falling edge of SCL) required by the SDA bus line to reach either \( 0.3V_{CC} \) or \( 0.7V_{CC} \), assuming that \( R_{bus} \times C_{bus} \) time constant is less than 400 ns.
Figure 9. Maximum $R_{bus}$ value versus bus parasitic capacitance ($C_{bus}$) for an I2C bus at maximum frequency $f_C = 400$ kHz

The $R_{bus} \times C_{bus}$ time constant must be below the 400 ns time constant line represented on the left.

Figure 10. AC waveforms

Start condition

Stop condition

Start condition

Write cycle

Start condition
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 11. WLCSP 4-bump wafer-level chip-scale package outline

1. Drawing is not to scale.
### Table 11. WLCSP 4-bump wafer-level chip-scale package mechanical data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>millimeters</th>
<th>inches⁽¹⁾</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.270</td>
<td>0.240</td>
</tr>
<tr>
<td>A1</td>
<td>0.095</td>
<td>-</td>
</tr>
<tr>
<td>A2</td>
<td>0.175</td>
<td>-</td>
</tr>
<tr>
<td>b</td>
<td>0.185</td>
<td>-</td>
</tr>
<tr>
<td>D</td>
<td>0.833</td>
<td>-</td>
</tr>
<tr>
<td>E</td>
<td>0.833</td>
<td>-</td>
</tr>
<tr>
<td>e</td>
<td>0.400</td>
<td>-</td>
</tr>
<tr>
<td>e1</td>
<td>0.500</td>
<td>-</td>
</tr>
<tr>
<td>F</td>
<td>0.217</td>
<td>-</td>
</tr>
<tr>
<td>G</td>
<td>0.167</td>
<td>-</td>
</tr>
<tr>
<td>N</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>aaa</td>
<td>0.110</td>
<td>-</td>
</tr>
<tr>
<td>bbb</td>
<td>0.110</td>
<td>-</td>
</tr>
<tr>
<td>ccc</td>
<td>0.110</td>
<td>-</td>
</tr>
<tr>
<td>ddd</td>
<td>0.060</td>
<td>-</td>
</tr>
<tr>
<td>eee</td>
<td>0.060</td>
<td>-</td>
</tr>
</tbody>
</table>

1. Values in inches are converted from mm and rounded to four decimal digits.

### Figure 12. WLCSP 4-bump wafer-level chip-scale package recommended land pattern

![Diagram](attachment:1CL_FP_V1)
### 10 Part numbering

**Table 12. Ordering information scheme**

Example: M24 C64S F CU 6 T /T

<table>
<thead>
<tr>
<th>Device type</th>
<th>M24 = I²C serial access EEPROM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device function</td>
<td>C64S = 64 Kbits (8 K x 8 bits)</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>$F = V_{CC} = 1.7 \text{ V} \text{ to } 5.5 \text{ V}$</td>
</tr>
<tr>
<td>Package</td>
<td>CU = ultra-thin 4-bump WLCSP</td>
</tr>
<tr>
<td>Device grade</td>
<td>6 = device tested with standard test flow over $-30$ to $85 \degree \text{C}$</td>
</tr>
<tr>
<td>Option</td>
<td>T = Tape and reel packing</td>
</tr>
<tr>
<td>Process technology</td>
<td>T = Process letter</td>
</tr>
</tbody>
</table>

*Note: The M24C64S-FCU6T/T is RoHS compliant (ECOPACK®2).*
## Revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>06-Dec-2013</td>
<td>1</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
| 21-Mar-2014 | 2        | Updated Supply voltage and Operating temperature ranges in *Features*
|             |          | Updated *Section 1: Description*                                         |
|             |          | Updated *Table 8: Operating conditions*                                   |
| 30-May-2014 | 3        | Added *Figure 12: WLCSP 4-bump wafer-level chip-scale package recommended land pattern.* |
Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale. Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com